A 10-bit, 100 MS/s Analog-to-Digital Converter in 1-µm CMOS

Final Report

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Applications such as high-end video signal processing, high performance digital communications, and medical imaging require ADCs with sample rates approaching 100 MS/s and a dynamic range at the Nyquist bandwidth close to 60 dB. In response to these needs, there is a continued search for architectures and circuit techniques enabling a monolithic ADC to meet these specifications with a reasonable chip area and power dissipation. It is of particular interest that if such an ADC is fabricated in a standard CMOS technology.
This work addresses some of the known problems inherent in time-interleaved, or parallel, pipeline ADCs with a new architecture. A prototype of this architecture demonstrates, for the first time, 10-bit operation at the maximum sampling rate up to 95 MHz in 1 µm CMOS technology. It attains 59.5 dB SNDR at a low conversion rate, and more than 50 dB SNDR at 50MHz input frequency with a 95 MHz conversion rate. By using a minor offset control to suppress the fs/2 tone, 65 dB spurious free dynamic range (SFDR) is achieved. The simulated bit error rate is less than $10^{-10}$. The ADC implemented in fully differential circuitry uses the 2-channel 3-stage pipeline architecture. Each stage converts 4-bits, and 2-bits from 12-bit are used for digital error correction. Because all the digital clock signals are generated from the on-chip clock buffer, it requires a single full speed clock signal. The active chip area is 50 mm$^2$ and the ADC dissipates 1.2 W from a single 5 V power supply.
Chapter 1

Introduction

The analog-to-digital converter (ADC) and digital-to-analog converter (DAC) are required between the analog signal and the digital processor to take advantage of digital signal processing, because most signals in use are analog in nature. The digital signal processor has developed rapidly due to integrated circuit technology over the past 20 years. There are several reasons why digital signal processing of an analog signal may be preferable to processing the signal directly in the analog domain. First, accuracy considerations play an important role in determining the form of the signal processor. Second, the digital signals are easily stored on magnetic media (tape or disk) without deterioration or loss of signal fidelity beyond that introduced in the ADC. As a consequence, the signals become transportable and can be processed off-line. The digital signal processing method also allows for the implementation of more sophisticated signal processing...
algorithms which is difficult to perform precise mathematical operations on analog signal form. And, in some case, a digital implementation of the signal processing system is cheaper than its analog counterparts. However, one of the practical limitations of digital implementation is the speed and accuracy of the operation of the ADC, which normally requires more power and complex circuitry than DACs.

Applications such as high-end video signal processing [65][96], high performance digital communications [78], and medical imaging require ADCs with sample rates approaching 100 MS/s and a dynamic range at the Nyquist bandwidth close to 60 dB. For instance, the conventional NTSC TV system requires 8-bit resolution and a 20 MHz sampling rate. However, recently proposed high definition television (HDTV) digital VTR in Japan requires 10-bit resolution and 75 MHz sampling for 1125 scanning lines, a 60Hz field rate with 30MHz bandwidth luminance signal, and two 15MHz bandwidth color-difference signals. The requirements of conventional and HDTV systems are summarized in Table 1.1. In

Table 1.1  ADC requirement in conventional and HDTV system

<table>
<thead>
<tr>
<th>Applications</th>
<th>Requirements</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Resolution</td>
</tr>
<tr>
<td>NTSC</td>
<td>8 bit</td>
</tr>
<tr>
<td>HDTV</td>
<td>10 bit</td>
</tr>
<tr>
<td></td>
<td>Sampling Rate</td>
</tr>
<tr>
<td>TV, VCR</td>
<td>20 MHz</td>
</tr>
<tr>
<td>HDTV ENCODER</td>
<td>50 MHz</td>
</tr>
<tr>
<td>HDTV STANDARD</td>
<td>75 MHz</td>
</tr>
</tbody>
</table>

response to these needs, there is a continued search for architectures and circuit
techniques enabling a monolithic ADC to meet these specifications with a reasonable chip area and power dissipation. It is of particular interest if such an ADC is fabricated in a standard CMOS technology.

Most published ADCs which come close to these specifications are 10-bit bipolar ADCs [9][34][72][87][99] as shown in Figure 1-1 and 12-bit bipolar ADC [59]. Their high speed and wide dynamic range owes to the use of open-loop precise building blocks, including low-offset comparators. A recent ADC attains up to a 70 dB dynamic range with this approach [59]. CMOS ADCs, by contrast, tend to use
closed-loop op-amp based circuits for precise analog signal processing and closed loop auto-zeroed comparators in quantizers resolving 4-bits or more. It is therefore difficult for these circuits to attain both the dynamic range and the speed of a bipolar ADC built with devices of comparable $f_t$. For instance, an open-loop folding and interpolation ADC in 0.8 mm CMOS clocks at up to 75 MHz, but is limited to about 45 dB in dynamic range [62]. Device layout and other averaging techniques yield limited improvements in the accuracy of the intrinsically poorly-matched MOSFET. Parallelism is one reliable way to obtain a high throughput while retaining wide dynamic range. For instance, an array of identical high-resolution but low-speed ADCs may be time-interleaved in parallel to increase overall throughput, proportional increase in hardware complexity and power dissipation [2].

This work addresses some of the known problems inherent in time-interleaved, or parallel, pipeline ADCs with a new architecture. A prototype of this architecture demonstrates, for the first time, 10-bits operation at 100 MS/s in a 1µm CMOS technology.

The thesis is organized as follows. In Chapter 2, the high speed ADC architectures are reviewed and limitations of each type have been analyzed. Chapter 3 describes the basic limitations and requirements to build a CMOS ADC, the methods to overcome or relax the limitations, and an analysis of speed limitations in amplifiers. A detailed explanation of our system blocks, circuit design and layout
issues are presented in Chapter 4. The test results of this prototype CMOS ADC are discussed in Chapter 5, followed by conclusions in Chapter 6.
Chapter 2

High Speed ADC architectures

2.1 Fully Parallel (Flash) A/D Converter

Parallel (Flash) A/D conversion is by far the fastest and conceptually simplest conversion process [1][19][27][36][54][68][84][100][105][108]. As shown in Figure 2-1, an analog input is applied to one side of a comparator circuit and the other side is connected to the proper level of reference from zero to full scale. For N-bit resolution, $2^{N-1}$ comparators simultaneously evaluate the analog input and generate the digital output as a thermometer code. All the output from the comparator is encoded to Binary or Gray code digital output by encoding circuitry.

Because the flash converter needs only one clock cycle per conversion, it is often the fastest converter as shown in Table 2.1. Moreover, since references are made by a resistor string, they are monotonic, resulting in low differential
nonlinearity. However, there are several drawbacks. One is that the hardware

![Flash(Parallel) A/D converter architecture](image)

**Figure 2-1** Flash(Parallel) A/D converter architecture

**Table 2.1** High speed Flash A/D converters

<table>
<thead>
<tr>
<th>Process</th>
<th>N-bits</th>
<th>Conversion rate</th>
<th>Affiliation</th>
<th>Year</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bipolar</td>
<td>6-bits</td>
<td>2 GHz</td>
<td>NTT[100]</td>
<td>1988</td>
</tr>
<tr>
<td></td>
<td>8-bits</td>
<td>500 MHz</td>
<td>Sony[19]</td>
<td>1991</td>
</tr>
<tr>
<td></td>
<td></td>
<td>400 MHz</td>
<td>NTT[1]</td>
<td>1987</td>
</tr>
<tr>
<td></td>
<td>10-bits</td>
<td>300 MHz</td>
<td>Matsushita[34]</td>
<td>1993</td>
</tr>
<tr>
<td>CMOS</td>
<td>6-bits</td>
<td>125 MHz</td>
<td>Micro Networks[54]</td>
<td>1992</td>
</tr>
<tr>
<td></td>
<td>8-bits</td>
<td>30 MHz</td>
<td>TI[84]</td>
<td>1991</td>
</tr>
</tbody>
</table>
complexity increases exponentially with the resolutions because it needs a $2^{N-1}$ comparator circuits. This also means that the power dissipation and the chip area increase exponentially with the resolution. The second drawback is that the analog input must drive the large nonlinear input capacitance of the comparators. Since this input capacitance for the 10-bit is typically 40-100pF and the driving current reaches 24-60mA for a 100 MHz, 2 $V_{p-p}$ input signal, large-signal distortion may occur, further aggravated by the nonlinearity of the input capacitance.

The third disadvantage is that the mismatch in the resistor reference ladder and the unequal input offset voltage of comparators limits the resolution to about 8-bit in CMOS technologies [84]. The mismatches in offset voltage can be represented by $V_{be}$ mismatches in bipolar process and $V_t$ mismatches in CMOS process. The $V_{be}$ mismatch of the self-aligned bipolar transistor is due to both emitter saturation current mismatch and emitter resistance mismatch of transistor pairs. $\Delta V_{be}$ can be written as

$$\Delta V_{be} = \frac{KT}{q} \ln \left( \frac{I_{s1}}{I_{s2}} \right) + (R_{e1} - R_{e2}) I_e$$

(2.1)

where $I_{s1}$ and $I_{s2}$ is a saturation current of two devices and $R_{e1}$ and $R_{e2}$ are the emitter resistance of two devices, respectively. In the low emitter current range, the first term of eq. (2.1), which has a linear dependency on the emitter perimeter-to-area ratio, is the dominant factor in the mismatch of $V_{be}$. In the high current range, the emitter contact resistance which is the second term of eq. (2.1), is the dominant
factor of the mismatch in $V_{be}$. In the self-aligned bipolar process, the standard deviation of a $V_{be}$ mismatch is 1–2 mV for medium emitter current ($\approx 200\mu$A) or less with the emitter area larger than 0.2x2.3$\mu$m$^2$ [79]. A 10-bit A/D converter has been reported by adding a preamplifier in front of the comparator and by choosing a proper emitter size transistor to reduce the comparator offset due to $V_{be}$ mismatch [34]. The threshold voltage, $V_t$, in the CMOS process can be represented as

\begin{equation}
V_t = V_{fb} + \sqrt{\frac{(2\varepsilon_{si}qN_A 2\phi_b)}{C_{ox}}} + 2\phi_b
\end{equation}

where $V_{fb}$ is a flatband voltage, $\varepsilon_{si}$ is a permittivity of silicon, and $N_A$ is a doping density. The local doping density variation causes a $V_t$ mismatch in a CMOS process, and the standard deviation of length of 1$\mu$m and width of 9$\mu$m device mismatch fabricated in 1$\mu$m process with 20nm thin oxide thickness is about 5 mV [69]. To obtain a 10-bit resolution with a 2.0 V$_{p-p}$ input signal, the comparator should resolve 2 mV, which is very difficult to obtain in bipolar and even more difficult in a CMOS process. Therefore, several schemes, such as adding a chopper amplifier [36] and auto-zero scheme to sample an offset in the capacitor in front of the latch, or inserting a preamplifier [108] in front of the latch, have been developed to decrease DNL of the ADC.

### 2.2 Subranging and two-step A/D Converter

The subrange and two-step architecture was developed to reduce hardware
complexity, reduce power dissipation and die area, and also to reduce input capacitance which loads the preceding circuit. Conceptually, these types of converter need $m \times 2^n$ comparator instead of $2^N$ comparators where $N = m \cdot n$ assuming $n_1, n_2, \ldots, n_m$ are all equal to $n$. For example, the 10-bit 2-stage subrange converter needs 64 ($2 \times 2^5$) comparators instead of 1024 ($2^{10}$) comparators in flash type. However, the conversion in subrange and two-step ADC does not occur instantaneously like a flash ADC, and the input has to be held constant until the sub-quantizer finishes as its conversion. Therefore, the sample-and-hold circuit is required to improve performance. Even though multi-stage (> 2) converters are possible, these types of ADC must be 2-stage because of delay in the sub-stage.

### 2.2.1 Subrange A/D converter

A subrange ADC which consists of $2^N$ resistors, $2^{N/2} - 1$ comparators, a switch bank, and a S/H [11][80] is illustrated in Figure 2-2. In the first step, the S/H samples the input signal and the sampled input is quantized by the first quantizer which consist of $2^{N/2} - 1$ comparator referenced on a resistor string every $2^{N/2}$ taps apart. In the second phase, the previous quantized result (MSB) determines the selected interval of a resistor string for the second quantization where the fine conversion (LSB) has to be made. One with $2^{N/2} - 1$ comparators can perform both the MSB and LSB quantization.
The simple holding capability has been added to the 2nd comparator circuit to increase a conversion speed, especially in CMOS ADC so that the S/H can acquire a new input signal after the MSB has been determined. The extra comparators were added to the 2nd quantizer, and a digital error correction scheme was used to increase conversion linearity [17][51][88].

### 2.2.2 Two-stage A/D converter

A two-stage converter consists of a sample-and-hold (S/H), two coarse quantizers, DAC, subtracter and gain block as shown in Figure 2-3. The S/H samples and holds the input signal. This sampled signal from the S/H circuit is
quantized by the first coarse quantizer. The first quantizer output selects the DAC output, and the residue is made from the difference between a sampled input signal and DAC output. The residue is amplified and is quantized by a 2nd coarse quantizer. The S/H output is held until the 2nd quantizer finishes the conversion. In a subrange architecture, the second quantizer can only tolerate a $\pm 1/2$ LSB of $N$-bit offset for the $N$-bit ADC, even though the precision of the first quantizer can be relaxed by adding some of the extra comparator at both ends of the second quantizer and by adapting an error correction scheme. But in a two-step architecture, both the first and second quantizers can tolerate more than a $\pm 1/2$ LSB of $N$-bit offset for the $N$-bit ADC because the residue amplifier can amplify the residue signal to the full input scale.

However, there are several disadvantages in the two-step architecture
changed to the flash architecture. The two-step ADC requires a DAC whose linearity should be better than \( N \)-bits for \( N \)-bit ADC, and also requires a subtracter (or a subtracter and residue amplifier) which can be the speed bottleneck. In addition, the conversion time is longer than a flash ADC because the two-step ADC has to wait until the residue signal is settled and quantized.

10-bit resolution has been reported in a two-step converter [12][58][83][72][89]. Furthermore, the 12-bit two-step ADC has been achieved with the supports of a self-calibration circuit and a trimming feature [30][31][40].

2.3 Multi-Stage Pipeline A/D Converters

The pipeline A/D architecture as shown in Figure 2-4 utilizes a sample-and-hold (S/H) in each stage to improve the conversion rate [9][42][46][47][50][87][90]. Each stage consists of a S/H, an \( N \)-bit flash ADC, a reconstruction DAC, a subtracter, and a residue amplifier. The conversion mechanism is similar to that of...
subranging conversion in each stage. Now the amplified residue is sampled by the next S/H, instead of being fed to the following stage. All the $N$-bit digital outputs emerging from the quantizer are combined as a final code by using the proper number of delay registers, combination logic and digital error correction logic.

Although this operation produces a latency corresponding to the sub-conversion stage before generating a valid output code, the conversion rate is determined by each stage’s conversion time, which is dependant on the reconstruction DAC and residue amplifier settling time. The multi-stage pipeline structure combines the advantages of high throughput by flash converters with the low complexity, power dissipation, and input capacitance of subranging converters. Furthermore, the T/H function can be obtained free if a switched capacitor amplifier is used in a residue amplifier circuit in CMOS technology.

One effective way to reduce power dissipation is by converting to one effective bit per each stage. When 2 effective bits have been digitized in each stage, the total number of the pipeline stage and the total number of the residue amplifier are reduce to half, but the residue amplifier gain increases by 2 times, which means the gain-bandwidth product has to be twice as large as the 1 effective bit per stage. Since the transconductance is

$$g_m = \sqrt{2\mu C_{ox} \frac{W}{L} I_d}$$  \hspace{1cm} (2.3)$$

$I_d$ has to be 4 times larger in an ADC converting 2 effective bits per stage than in 1 effective bit per stage. The number of comparators required to build the ADC is
larger in 1 effective bits per stage than that in 2 effective bits. The required residue amplifier gain and number of comparators are summarized in Table 2.2. However

Table 2.2  Effective bits vs. residue amplifier gain and number of comparator in 10-bit ADC

<table>
<thead>
<tr>
<th>Effective bits</th>
<th>Number of stage</th>
<th>Structure</th>
<th>Gain</th>
<th>Number of comparator</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>9</td>
<td>2bx9</td>
<td>2</td>
<td>3x9</td>
</tr>
<tr>
<td>2</td>
<td>5</td>
<td>3bx4+2b</td>
<td>G1-3=4</td>
<td>7x4+3</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>G3=2</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>3</td>
<td>4bx3</td>
<td>8</td>
<td>15x3</td>
</tr>
<tr>
<td>5</td>
<td>2</td>
<td>5b+6b</td>
<td>16</td>
<td>31+61</td>
</tr>
</tbody>
</table>

the number of comparators shown in Table 2.2 can be further reduced by using more sophisticated error correction scheme. For example, a 10-bit ADC which converts 1 effective bit per stage and consists of nine stages, nine op amps, and 19 comparators has been reported [42]. A power dissipation of 50 mW or less is obtained in 10-bit 20 MHz ADC using the 1 effective bit per stage concept [8][91]. However, the limitation of the low power approach in converting less bit per stage is that the gain accuracy of the first residue amplifier becomes more stringent, because the accuracy requirement is dependent on the remaining number of bits to be converted. For example, in 10-bit ADC using a one effective bit per conversion, the tolerable gain error in the first residue amplifier is less than \( \pm \frac{2^{-9}}{2} \). Since the capacitor matching is about 0.1%, the gain of the first several residue amplifiers
might need a gain adjustment.

### 2.4 Parallel Pipelined A/D Converters

The throughput rate can be increased further by using a parallel architecture as shown in Figure 2-5. The first channel samples the input while the other two channels are evaluating previously sampled input. Theoretically, the conversion rate can be increased by the number of parallel paths, at the cost of a linear increase in power and chip area.

However, this parallel pipeline architecture has three major sources of distortion. One error source is that a timing mismatch among the input samplers of
each channel can degrade spectrum purity. The timing mismatch among the channels is unavoidable because of asymmetry among the clock distribution in the layout, and also due to mismatch of devices such as clock buffer devices. With this fixed amount of timing mismatch, the signal-to-distortion ratio decreases at higher input signal frequency as shown in Table 2.3.

<table>
<thead>
<tr>
<th>Input signal frequency</th>
<th>SDR (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 MHz</td>
<td>70.1</td>
</tr>
<tr>
<td>20 MHz</td>
<td>64.0</td>
</tr>
<tr>
<td>50 MHz</td>
<td>56.1</td>
</tr>
</tbody>
</table>

The other sources of distortions are the input-referred offset mismatch, and the gain mismatch at the residue amplifiers among these channels. The inter channel input referred offset mismatch gives rise to fixed pattern noise. This can be found in the frequency domain as a tone at multiples of $f_s/N$ where $N$ is the number of channel and $n = 1, 2, \ldots, N$. The inter channel gain mismatch can generate a spurious tone at $f_s/N \pm f_{in}$, $2f_s/N \pm f_{in}$, $\ldots$, $Nf_s/N \pm f_{in}$. The input referred offset mismatch generates a tone at $lf_s/N$, $2f_s/N$, $\ldots$, $Nf_s/N$. In addition, the first S/H in each channel must have enough tracking bandwidth to acquire an input frequency up to the Nyquist frequency.

The effects of all three limitations can be dramatically reduced by adding a single sample-and-hold circuit in front of each channel, as shown in Figure 2-6. The
A parallel pipeline ADC with a single S/H

timing mismatch among the channels is not an issue when the parallel pipeline architecture has a single S/H, because S/H is distributing sampled signals instead of dynamic signals [74][106].
Chapter 3

General Considerations

3.1 Digital error correction

The digital error correction scheme is one way to overcome an offset of comparator in a data converter system using a coarse quantizer such as algorithmic ADCs [43][60][67][83] and pipelined ADCs. For example, we want to design a 8-bit algorithmic ADC with an ideal residue amplifier and an ideal DAC but with a comparator which has a 5-LSB input referred offset as shown in Figure 3-1. Because of the offset of the comparator, the Vin1 (which should be 10000001 in an ideal A/D converter) is quantized to 0 instead of 1 at the first conversion. The amplified (x 2) residue of Vin1 after the first quantization lands on an over-range scale, and the second through 8th quantized data are all quantized to 1 at sub-conversion, resulting in 01111111. The Vin2 (which should be 10000010 in an
ideal A/D converter) also converted to $01111111_2$ because after the first conversion, all the amplified residue landed on the over-range scale. Therefore, the requirement of the comparator is that the offset should be less than $1/2$LSB of the converter. To relax this requirement, the simple digital error correction scheme has been introduced[25][31][41].

As shown in Figure 3-2 (a), this offset at the comparator in the subconverter block which contains a coarse quantizer, a D/A converter and a residue amplifier
can be explained with a residue versus input plot. In Figure 3-2 (b), both the coarse quantizers and the D/A converter are assumed to be ideal. The residue can be expressed as

\[ \text{Residue} = \text{Vin} - \text{DACout} \tag{3.1} \]

where \( \text{DACout} \) is selected by a coarse quantizer. If the input (\( \text{Vin} \)) of a subconverter block is between two adjacent thresholds of the coarse quantizer, the residue is a linearly increasing function with the input. Once the Vin is increased over the coarse quantizer threshold, the residue abruptly changes by 1 LSB because the DAC input has increased by 1. Therefore the ideal residue waveform looks like a saw-tooth as shown in Figure 3-2 (a). Here, the residue is always between ±1/2 LSB and consists only of the part of the input that is not quantized by the first stage. With the interstage gain equal to 2, the maximum residue is amplified into a full-scale input to the next stage; therefore, the conversion range of the next stage is equal to the maximum residue out of the first stage.

Two similar curves are shown in Figure 3-2 (c) for a case when the coarse quantizer has some input referred offset, but the DAC is still ideal. In this example, two of the A/D subconverter decision levels are shifted, one by -1/4 LSB and the other by +1/4 LSB. If the decision levels are shifted by less than 1/4 LSB, the range of the residue increases 1/4 LSB on both ends of the ideal conversion range which is between -1/2 LSB and +1/2 LSB. Because the residue consists of the unquantized part of the input and the error caused by the offset of the coarse
Figure 3-2  (a) Block Diagram of N-bit/stage in a pipeline A/D converter. (b) Ideal residue versus input. (c) Residue versus input with quantizer nonlinearity when N=2
quantizer, these increased residues are accurate for the codes to which they correspond as long as the DAC output is ideal; therefore, at this point, no information is lost. Even though the interstage gain is 2, however, information can be lost when the larger residues saturate the next stage and produce overflow in the conversion. Therefore, if the conversion range of the second stage is increased to handle the larger residues, they can be encoded and the errors corrected. This process is called digital error correction.

A digital error correction scheme can be utilized with the 8-bit A/D converter shown in Figure 3-3, which illustrates the two conversion process with the non-ideal (vin1) and ideal (vin2) comparator, and with the underflow and overflow indication. The non-ideal comparator is modeled as a comparator with offset of more than 6 LSB of 8 bit and the ideal comparator is modeled as a comparator with zero offset. Because of the offset in a non-ideal comparator case, the output is 0 instead of 1. At the second conversion process, the residue input is larger than full scale and the comparator output indicates the 1 with the overflow. With the overflow indication, the second residue of the non-ideal comparator case becomes the same as that of the ideal comparator case. Once the conversion process is completed, the digital output with overflow and underflow indication should be recalculated such that a digital output 1⁺ has to add 1 to the upper digital data and set itself to 0 and a digital output 0⁻ has to subtract 1 from the upper digital data and set itself to 1. If the comparator has no offset, the overflow and underflow range are
not needed. Otherwise, these are used for generating extra information for digital error correction. The digital error correction scheme improves linearity by allowing the converter to postpone decisions on inputs that are near the first coarse quantizer threshold until the residue from these inputs are amplified to the point where similar coarse quantizer threshold offset in the later A/D converter block is insignificant. The penalty in using a digital error correction is that it requires a redundant

Figure 3-3  Effect of comparator offset in algorithmic A/D converter
comparator and correction logic.

Because in digital circuits the subtraction process, which consists of two’s complement and addition, is more complex than the addition process, digital error correction with only an addition process algorithm has been investigated [15][42][83]. One way to eliminate subtraction in the digital error correction by shifting a comparator offset by 1/2 LSB has been investigated [42], and the residue waveform of this method is illustrated in Figure 3-4. The correction range can be defined as the amount of offset shift at the coarse quantizer that can be tolerated without error. If the DAC and the residue amplifier is ideal with gain of 2, the amplified residue from Figure 3-4 (a) remains within the conversion range of the next stage when the coarse quantizer offsets are shifted no more than 1/2 LSB. Under this condition, errors caused by the coarse quantizer offsets can be corrected. Because the offset introduced into the coarse quantizer in Figure 3-4 (b) is 1/2 LSB, the digital output is always less than or equal to its ideal value if a coarse quantizer offset can shift the threshold back to the left by no more than 1/2 LSB. Thus, the correction requires no change or addition. While the ideal residue in Figure 3-4 (a) is always between $\pm V_r/4$, the range of ideal residues in Figure 3-4 (b) is $-V_r/2$ to $+V_r/4$. With identical stages and an interstage gain of 2, the minimum residue in Figure 3-4 (b) occurs on the left end of the plot and rests on the lower conversion-range boundary of the next stage. Although movement of the threshold of the coarse quantizer has no effect on the value of this left-end residue, interstage offset or gain
error may cause the left-end residue to lie below the conversion range of the next stage.

Figure 3-4  Ideal Residue vs. input of the ADC block (a) without a offset comparator (b) with 1/2 LSB comparator offset
3.2 Nonlinearity in interstage block of ADC

3.2.1 Offset of residue amplifier

As was discussed in the previous section, if the amplified residue does not exceed the full conversion range of the following coarse quantizer, the linearity of ADC is not affected by the digital error correction scheme. Therefore, the input referred offset of a residue amplifier must meet the following requirement:

$$\frac{1}{2} \cdot LSB \leq \text{offset}_{RA} + \text{offset}_{quant.} \leq \frac{1}{2} \cdot LSB$$  \hspace{1cm} (3.2)

with the conversion range as shown in Figure 3-4.

Even though the offset canceling scheme has been used to cancel out the offset of op amp, offsets still remains due to a limited op amp DC gain, mismatches in switches, and capacitors in the residue amplifier. An offset resulting from two different sources with a slightly mismatched capacitor is reviewed. For example, one of the four capacitors in Figure 3-5 is mismatched as follows:

$$C_{s1} = N \cdot C$$
$$C_{s2} = N \cdot C$$
$$C_{f1} = C$$
$$C_{f2} = (1 + \varepsilon) \cdot C$$  \hspace{1cm} (3.3)

Let’s assume the op amp has an infinite DC gain and zero input referred offset. From charge conservation, the charge stored at each node of the differential input of op amp can be described as follows
Assume $V_{boc} = V_{oc}$ for simplicity. Then, during the reset phase ($\phi_1 = “1”$), $V_{a1}$ and $V_{a2}$ become $V_{oc}$ because the residue amplifier is shorting its output to input of the op amp through switch $M_{f11}$ and $M_{f21}$ due to DC gain of the op amp. During the amplifying phase ($\phi_2 = “1”$), $V_{a1}$ and $V_{a2}$ become equal. Therefore, eq. (3.4) and
(3.5) becomes

\[ V_{o}(1 + \frac{N+2}{N+1} \cdot \frac{\varepsilon}{2}) = N \left( 1 - \frac{\varepsilon}{2(N+1)} \right) V_{in} - \frac{N\varepsilon}{N+1} (V_{bic} - V_{ic}). \]  

(3.6)

From eq. (3.6), we can find that

1. The offset is due to difference between the output common mode of the previous stage \(V_{ic}\) and the input common mode voltage \(V_{bic}\) when the amplifier is amplifying the residue. And the offset can be found due to the difference between the biasing voltage of \(C_f(V_{boc})\) and the op amp output common mode voltage \(V_{oc}\).

2. The other offset is due to the injected charge \(Q_{inj}\) from \(M_{f11}\) and \(M_{f21}\) to the node of input differential pair of the op amp at the end of \(\phi_f = 1\) which can be modeled as the input common mode difference \(Q_{inj} = C_{s1} \cdot \delta V = C_{s2} \cdot \delta V\).

### 3.2.2 Gain inaccuracy of residue amplifier

The gain deviation from the ideal gain in a residue amplifier increases the DNL of the A/D converter as shown in Figure 3-6. In order to avoid a missing code at the end of the transition, the tolerable gain error (\(\varepsilon\)) can be expressed as

\[ \left| (G_{ideal} - G_{actual}) \cdot \frac{1}{2} \cdot LSB \right| < \frac{1}{2} \cdot 2^{-r} \cdot V_r \]  

(3.7)

where \(G\) is interstage gain, a unit of 1 \(LSB\) is a resolution of coarse quantizer, \(V_r\) is input full scale, and \(r\) is the number of bits of resolution of the sum of the following subconverters. Since
Therefore, the gain accuracy required at the residue amplifier is determined by the sum of the following subconverters resolution. The gain inaccuracy arises from capacitor mismatch and the finite DC gain of the residue amplifier.

The gain of the op amp can be represented by the product of the

\[ 1\text{LSB} \cdot G_{\text{ideal}} = V_r, \]  

\[ (3.8) \]

\[ \varepsilon = 2^{-7} \]  

\[ (3.9) \]

Figure 3-6 Effects of interstage gain error
transconductance to the output and output impedance where the signal current generated from the differential pair flows through the cascode stage. As the impedance at the output goes high, not all the current generated from the differential pair can pass through the cascode stage. This means that the input impedance of the cascode stage is not low any more. Therefore, a voltage swing develops at the input of the cascode stage which is represented as $G_1$ in Figure 3-7. The output ($V_{out}$) of the amplifier can be represented as

$$V_o = \frac{C_i}{C_f \left(1 + \frac{1}{G} \left[1 + \frac{C_{ip} + G_1 C_{gd} + C_i}{C_f}\right]\right)} V_{in}$$

(3.10)

where $G(= G_1 \cdot G_2)$ is the overall DC gain of the op amp, and $C_{gd}$ is the gate to drain
capacitance in the input differential pair. The gain error should be less than $2^{-r}$, which is tolerable from eq. (3.9). Therefore, the overall DC gain, $G$, should be

$$G > 2^r \left(1 + \frac{C_{ip} + G_1 C_{gd} + C_s}{C_f}\right).$$  \hspace{1cm} (3.11)$$

This tolerable gain error is calculated from the static requirement which applies at low conversion rates, whereas the unavoidable gain error due to incomplete settling of the op amp in the ADC can be observed in the high conversion rate.

There are two major sources of static gain inaccuracy. The one gain inaccuracy occurs from the capacitor mismatch, and the other gain inaccuracy occurs from the finite DC gain of the OP amplifier as shown in eq (3.11).

### 3.3 Capacitor and resistor mismatch

#### 3.3.1 Capacitor mismatch

The matched capacitors or precision capacitor ratios have been used extensively for many years to make accurate A/D and D/A converters [55][93][104], filters, and precision amplifiers. Because the capacitor matching accuracy plays an important role in performance, many studies have been reported on this topic [37][39][56][85][86][95].

There are several mismatch error sources in MOS capacitors. The first error source consists of long-range, gradient related systematic errors, which are strongly correlated for all capacitors on the same chip. These can be kept to a minimum by
using unit-capacitor layout techniques with a common centroid geometry [55].

The second error type results from uncorrelated random effects of edge variations and deviations of oxide thickness and permittivity of MOS capacitors. These random errors decide the ultimate limitation on the achievable accuracy of MOS analog integrated circuits. The systematic and random capacitor mismatches are calibrated in the prototype ADC.

The voltage coefficients of small signal capacitance can limit the accuracy of the ADC. For MOS capacitors on heavily doped N+ back plates, about 30 ppm/V voltage coefficients have been reported[56]. And McCreary reported the temperature dependence of MOS capacitors measured approximately 25 ppm/C. Capacitor hysteresis and MOS threshold voltage hysteresis due to dielectric absorption in the capacitor has also been reported [39][95].

The 10-bit and 8-bit capacitor ratio mismatch was measured[55][93] in the early days of MOS ADCs. A 9-bit capacitor matching accuracy has been reported using a binary weighted capacitor array which is made of 25X25μm poly-N+ diffusion in NMOS technology[86] where the capacitor matching between two minimum unit capacitors was better than 10-bit. And the measured capacitor matching between 26 ~ 90 fF unit capacitor has been measured at 0.1~1% [37]. In addition, layout rules which makes it possible to achieve 0.1% accuracy for the individual systematic error sources with unit capacitor in the 20~40μm range has also been reported [57].
3.3.2 Resistor mismatch

The matching properties of the resistor is one of the limiting factors in ADC and DAC performance such as the reference voltage for comparators, DAC output of a subconverter block in ADC, and DAC output itself. The reference voltage for each comparator can be generated from one of the \(2^n\) resistor cells connected between two reference voltages at the end of the resistor string. The integral nonlinearity and differential nonlinearity of ADC are dependent upon that of the resistor string, especially in the flash and subrange type. In some of 8~10 bits subrange [11][12][53][83], two-step[72], and pipeline[41] ADC, the resistor has been used to generate a DAC output to form a residue for the following stage. The matching of resistor string and the operation speed was proven by the 10-bit 50 MHz DAC[4][70].

To find the resistor matching requirement for an \(n\)-bit resistor string with \(N\)-bit matching, assume that the resistor values are normally distributed with mean \(R\) and standard deviation \(\sigma_R\). Then, the mean and the variance of the \(m\)-bit resistor string (\(RS_m\)) which consists of \(2^m\) resistors connected in series, can be describe as:

\[
\text{mean} (RS_m) = 2^m \cdot R \\
\text{Var} (RS_m) = 2^m \cdot \sigma_R^2
\]

(3.12)

Since the worst deviation from the ideal value occurs at the mid-point of the resistor string as shown in Figure 3-8, we can model this as two big segments of resistors.
Eq. (3.12) can be written such that each segment matching of a resistor string can be represented as normal distribution with

\[
RS_{N/2} = \text{Normal} \left( 2^{N/2} R, 2^{N/2} \sigma^2 \right)
\]

The deviation must be less than \( \pm 1/2 \) LSB of \( N \)-bit ADC from the gain accuracy requirement. Assuming that the each segment of the resistor string can be represented as a mean value and a standard deviation, this resistor matching condition can be described as

\[
\begin{align*}
\text{mean} (RS_{n/2}) &= 2^{n/2} \cdot R \\
\text{Var} (RS_{n/2}) &= 2^{n/2} \cdot \sigma_R^2
\end{align*}
\]

Figure 3-8 Matching requirement in resistor string with n-bit precision and N-bit accuracy
To maximize the effect of mismatch, one part of the segment has a positive sign and the other has a negative sign in the variation. With this assumption, eq. (3.14) becomes

\[
\frac{1}{2}\left(1 - \frac{1}{2^N}\right) \leq \left| \frac{2^{n-1}R \pm 2^{(n-1)/2}\sigma_R}{2^{n-1}R + 2^{(n-1)/2}\sigma_R + 2^{n-1}R \pm 2^{(n-1)/2}\sigma_R} \right| \leq \frac{1}{2}\left(1 + \frac{1}{2^N}\right).
\]

(3.14)

where \( n \) is the resolution and \( N \) is the linearity in bits [12]. For example, if 4-bit resolution and 10-bit linearity is needed, \( \sigma_R/R \) should be < 0.27%.

In order to achieve good matching, all resistors in the DAC should be built of the same basic resistor element. Three effects are considered to have an impact on relative accuracy: geometry (which is determined by shape), width, and length, resulting in local mismatches, gradients of sheet resistance, and variations in the polysilicon-metal contacts. In hand-crafted analog design, it is not unusual to design well-matched resistors without any bends. In a flexible layout generator for different resolutions (\( 2^N \) resistors), the resistors must contain bends or the area requirement would become excessive. Effects that decrease matching due to deterministic errors caused by bends, lithography, and etching are minimized by using an identical basic resistor cell for all matched resistors. In addition, better matching can be obtained by increasing width and length of a resistor basic cell, because most of the randomness stems from the perimeter due to lithography. The
gradients of the sheet resistance can be eliminated in the first order by layout in the cross coupled manner[72]. Another matching problem stems from contacts interconnecting a string resistors. The widely varying contact resistant becomes important to get a good matching in a low resistor sting especially in high-resolution converters. Further, the contacts should be avoided in the current path because it can lead to contact alignment error by mask tolerance.

3.4 Amplifier design

3.4.1 Residue amplifier

Figure 3-9 shows the switched capacitor amplifier with offset compensation. At the sampling phase, the sampling behavior depends on the unit gain bandwidth and phase margin of the circuit. But at the amplify phase, the settling behavior mostly depends on the closed-loop time constant of the amplifier only. Because the feedback factor ($\beta$) is smaller than 1, the phase margin is not an issue at the amplifying phase.

The feedback factor ($\beta$) during the amplifying phase is

$$\beta = \frac{C_f}{C_f + C_{ip} + C_{in}}$$

(3.16)

and the time constant ($\tau$) is

$$\tau = R_{eq} \cdot C_{eq}.$$  

(3.17)

Since
Figure 3-9  (a) Schematic of residue amplifier with offset compensation  
(b) During sampling phase  
(c) During amplifying phase
\[ R_{eq} = \frac{1}{g_{m eff}} \]
\[ = \frac{1}{(\beta \cdot g_m)} \]
\[ = \frac{(C_f + C_{ip} + C_{in})}{C_f} \cdot \frac{1}{g_m} \]  \hspace{1cm} (3.18)

and

\[ C_{eq} = C_o + \frac{1}{\frac{1}{C_f} + \frac{1}{C_{in} + C_{ip}}} \]
\[ = C_{load} + C_{op} + \frac{1}{\frac{1}{C_f} + \frac{1}{C_{in} + C_{ip}}} \]  \hspace{1cm} (3.19)

where \( C_{sm} \) is an input sampling capacitor, \( C_f \) is a feedback capacitor, \( C_{ip} \) is an input differential pair capacitance including wiring, and \( C_{op} \) is a parasitic capacitance from an op-amp output device and from wiring. Then, the time constant \( (\tau) \) becomes

\[ \tau = \frac{\{C_{ip} + C_{in} + C_{load} + C_{op} + (C_{in} + C_{ip}) (C_{load} + C_{op}) \} / C_f \}}{g_m} \]  \hspace{1cm} (3.20)

Figure 3-10 plots time constant from eq. (3.20) with a varying sampling capacitor size \( (C_{sm}) \) where a gain of amplifier is 2 and with the following parameters: in the case where an amplifier gain is \( A \) \( (C_{sm} = A \cdot C_f) \), the optimum time constant can be retained when the optimum feedback capacitor \( (C_{fop}) \) and the optimum sample capacitor \( (C_{smop}) \) are
By choosing a following capacitive load equal to the input capacitor

\[ C_{load} = C_{sm}, \]  

(3.22)

the optimum feedback capacitor \( C_{fop} \) and the optimum input capacitor \( C_{smop} \) becomes

\[
C_{fop} = \frac{(C_{load} + C_{op}) \cdot C_{ip}}{A} \\
C_{smop} = \frac{A \cdot (C_{load} + C_{op}) \cdot C_{ip}}{A + 2}.
\]  

(3.21)
3.4.2 Effect of feedback switch size

Once the optimum capacitor sizes are chosen, the next step is to decide upon a size for the switches. All the switches (\(S_{\text{smpl}}\), \(S_{\text{amp}}\), \(S_{f2}\)) except \(S_{f1}\) in Figure 3-9 (a) should be sized such that the time constant of switch resistance and the associated capacitor is small enough so that it does not decrease the -3 dB bandwidth of the amplifier. But the size of the \(S_{f1}\) is selected differently. The optimum switch size of \(S_{f1}\) may increase the -3 dB bandwidth by introducing a zero to help position the closed-loop poles at a desired location. The transfer function from \(V_{\text{in}}\) to \(V_{\text{out}}\) is

\[
\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{C_{sm} \cdot (Y_f - g_m)}{s^2 \cdot C_L \cdot (C_{sm} + C_{\text{inp}}) + s \cdot Y_f \cdot (C_L + C_f + C_{\text{inp}}) + g_m \cdot Y_f}
\]

where \(Y_f\) is an admittance in the feedback path. Since \(Y_f = 1/(R_f + 1/(s \cdot C_f))\), the equation (3.24) becomes

\[
\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{C_{sm} \cdot (sC_f(1 - g_m R_f) - g_m)}{s^2 C_L C_f R_f (C_{sm} + C_{\text{inp}}) + s (C_L + C_f)(C_{sm} + C_{\text{inp}}) + C_f g_m} + \frac{C_{sm} + C_{\text{inp}} + C_f C_L + C_f g_m}{}
\]

The denominator of equation (3.25) can be expressed as
\[ \text{Den}(s) = g_m C_f \cdot \left( \frac{s^2 (C_{sm} + C_{inp}) C_L R_f}{g_m} \right) \]

\[ + \frac{s ((C_L + C_f) (C_{sm} + C_{inp}) + C_f C_L)}{g_m C_f} + 1 \right) \]

\[ = g_m C_f \cdot \left( \frac{s^2}{\omega_0^2} + \frac{s}{Q \omega_0} + 1 \right) \]

where

\[ \omega_0 = \sqrt{\frac{g_m}{C_L R_f (C_{sm} + C_{pin})}} \].

\[ Q = \frac{C_f}{(C_L + C_f) (C_{sm} + C_{pin}) + C_f C_L} \cdot \sqrt{g_m R_f C_L (C_s + C_{pin})} \]

The zero location can be easily estimated by equating a feedback current \((i_f)\)

with \(g_m\) current as shown in Figure 3-11

\[ g_m V_a = \frac{V_a}{(R_f + 1/(s \cdot C_f))} \],

or by using equation (3.25). Also, a closed loop pole location can be found from

Figure 3-10 if the sampling capacitor \((C_{sm})\) is determined by the time constant \((\tau)\)

requirement. The value of feedback resistor \((R_f)\) can be estimated from eq. (3.28)

by substitution of \(s\) with \(-1/\tau\).

The transient step input response of the corresponding \(R_f\) is shown in Figure

3-12. From the transient response in Figure 3-12, when the \(R_f\) is larger than the

optimum value, peaking can be observed in the frequency domain and the overshoot
appears in the step response. However, the step response of the system can not be exactly estimated from the $Q$ factor because the system has a zero. Therefore, the optimum step response can be found from the transient simulation. With more than one overshoot, ringing increases the settling time drastically. The optimum feedback resistor value is converted to the MOS switch size for $M_{f/2}$.

### 3.4.3 Non-resetting Sample-and-Hold Amplifier

The major advantage of using a non-resetting sample-and-hold amplifier is that the subsequent stage can sample the amplifier output during the full period, unlike the resetting amplifier which provides a valid output only during half of the clock period. If interchannel offset mismatch is the one of the major performance
Figure 3-12  Transient step response with different switch size
Figure 3-13  (a) Non-reset Track and Hold amplifier schematic (b) During sampling and holdingII period (c) During holdingI period
limitation in ADCs such as a parallel architecture, an offset cancellation scheme is required. However, the bandwidth of unity gain feedback is set up by the op amp, and this is usually much lower than that of the passive sampling. Therefore, the non-resetting amplifier is more important in a high speed ADC than offset cancellation.

The half circuit of a non-resetting sample-and-hold amplifier [64] is illustrated for simplicity in Figure 3-13. During a sampling period (Figure 3-13 (b)), the sampling bandwidth on the sampling capacitor \( C_1 \) is determined by the \( RC \) time constant of \( C_1 \) and associated resistance from the MOSFET switches \( S_1 \) and \( S_2 \). Therefore, the sampling bandwidth can be as large as 1GHz[6]. Meanwhile, the holding capacitor \( C_2 \) is holding a previously sampled value while \( C_1 \) is sampling a new input. During holdingI period (Figure 3-13 (c)), the sampling capacitor \( C_1 \) is inserted in the negative feedback path and the dummy holding capacitor \( C_{2d} \) is inserted in positive feedback. Even though there are two capacitor \( C_1, C_2 \) in the feedback path, the charge from the \( C_2 \) in the feedback path is cancelled out by \( C_{2d} \) which is the same size as \( C_2 \), and \( C_1 \) will be the only feedback capacitor to determine the output of the op amp. The feedback factors at the tracking period \( (\beta_{track}) \) and at the holding period \( (\beta_{hold}) \), are

\[
\beta_{track} = \frac{C_1 + C_2 - C_{2d}}{C_1 + C_2 + C_{2d} + C_{ip}}
\]
\[
\beta_{hold} = \frac{C_2}{C_1 + C_{ip}}
\]

(3.29)
where $C_{ip}$ is the capacitance of the wiring, diffusion of switches, and input differential pair. If $C_2 = C_{2d}$, eq. (3.29) can be simplified as

$$\beta_{track} = \frac{C_1}{C_1 + C_2 + C_{2d} + C_{ip}}$$

(3.30)

and

$$\beta_{hold} = \frac{C_2}{C_2 + C_{ip}}.$$  

The effective capacitive loading at the output at the holdingI period ($C_{o,holdI}$) and at the holding period ($C_{o,holdII}$), are

$$C_{o,holdI} = (1 - \beta_{track}) (C_1 + C_2) + C_{load} + (1 + \beta_{track}) C_{2d}$$

$$C_{o,holdII} = (1 - \beta_{hold}) C_2 + C_{load} + C_{2d}.$$  

(3.31)

Therefore, the time constants associated with each period are

$$\tau_{holdI} = \frac{C_{o,holdI}}{g_m \beta_{holdI}}$$

(3.32)

and

$$\tau_{holdII} = \frac{C_{o,holdII}}{g_m \beta_{holdII}}.$$

From eq. (3.32), in order to reduce the time constant ($\tau_{holdI}$) during holdingI period, the $C_d$ should be decreased, because not only does the effective $g_m$ decrease as $\beta$ decreases (eq. (3.29)), but $C_{o,holdI}$ also reduces the effective capacitive loading. As $C_d$ reduces, however, the time constant ($\tau_{holdII}$) during holdingII period reduces. Therefore, $C_d$ has to be larger than a certain value so that the sample-and-hold output can recover from injected charges due to capacitor switching during the holdingII period.
3.5 Analysis of clock jitter

A small clock jitter in the high speed Nyquist analog-to-digital converter is required so as not to reduce signal-to-noise ratio, especially at input frequencies near Nyquist input [2][29]. The average error power due to clock jitter is given by

\[
E_j = \sum_{i=1}^{m} \langle \left( \hat{x}_i - x_i \right)^2 \rangle
\]  

(3.33)

where \( m \) is the number of samples in one period and \( \hat{x}_i \) is the sampled value of \( x_i \).

For a sinusoidal input waveform, and ideal samplers which exhibit a timing skew,

\[
x_n = A \cdot \sin (\omega \cdot nT)
\]  

(3.34)

and

\[
\hat{x}_n = A \cdot \sin (\omega \cdot (nT - \delta))
\]  

(3.35)

where \( x_i \) is the value sampled at \( nT \) and \( \hat{x}_n \) is the value sampled at \( nT \) with the timing jitter noise \( \delta \). For the values of \( x_i \) and \( \hat{x}_n \), the error power, \( E_j \) in eq. (3.33) becomes

\[
E_j = \frac{A^2}{m} \cdot \sum_{n=1}^{m} \left( \sin (\omega \cdot (nT - \delta)) - \sin (\omega \cdot nT) \right)
\]

\[
= \frac{A^2}{m} \cdot \sum_{n=1}^{m} (1 - \cos (\omega \delta))
\]

\[
= A^2 \cdot \left( \frac{\omega^2 \delta^2}{2!} + \frac{\omega^4 \delta^4}{4!} + \ldots \right)
\]  

(3.36)

which for small values of timing jitter may be approximated by
Therefore, signal-to-noise due to clock jitter ($SNR_j$) is

$$SNR_j = 10 \cdot \log \frac{A^2/2}{A^2 \omega^2 \delta^2/2}$$

$$= -20 \cdot \log \left( \omega \delta \right)$$

where $\delta$ is the R.M.S. value of clock timing jitter. The $SNR_j$ vs. $\delta$ is plotted in Figure 3-14. This plot shows that the clock timing jitter should be less than 5 ps (rms) to avoid reducing the SNR by 3 dB from quantized noise at 50 MHz input frequency.

Figure 3-14  Signal to noise due to clock timing jitter at 10 MHz, 30 MHz, and 50 MHz input frequency
3.6 Analysis of non-linear effect at multi-channel

Multi-channel parallelism in an ADC can increase conversion speed by the number of channels, but there are well-known problems such as offset, gain and timing mismatches among the channels which do not arise in digital systems [2][10][29][71][74].

3.6.1 Timing mismatch in the channels

The effect of timing mismatch among the channels has been analyzed and documented[29]. The analysis can be summarized as follows. Let the original sampled data sequence \( S = [x(t_0), x(t_1), x(t_2), ..., x(t_m), ..., x(t_M), x(t_{M+1}), ...] \) be
divided into \( M \) subsequences \( S_0, S_1, S_2, \ldots, S_{M-1} \) as follows:

\[
S_0 = [x(t_0), x(t_M), x(t_{2M}), \ldots] \\
S_1 = [x(t_1), x(t_{M+1}), x(t_{2M+1}), \ldots] \\
S_2 = [x(t_2), x(t_{M+2}), x(t_{2M+2}), \ldots] \\
\vdots \\
S_m = [x(t_m), x(t_{M+m}), x(t_{2M+m}), \ldots] \\
\vdots \\
S_M = [x(t_{M-1}), x(t_{2M-1}), x(t_{3M-1}), \ldots].
\] (3.39)

The \( S_m \) is obtained by uniformly sampling the signal \( x(t+t_m) \) at the rate \( 1/MT \).

Assume

\[
\overline{S}_m = [x(t_m), 0, 0, \ldots (M-1\text{ zeros}), x(t_{M+m}), 0, 0, \ldots], \quad (3.40)
\]

we can represent the original sequence, \( S \), as

\[
S = \sum_{m=0}^{M-1} \overline{S}_m z^{-m}. \quad (3.41)
\]

Then, the digital spectrum, \( X(\omega) \), of \( S \) can be represented as

\[
X(\omega) = \frac{1}{MT} \cdot \sum_{m=1}^{M-1} \left[ \sum_{k=0}^{\infty} X_a^m(\omega - \frac{2\pi k}{MT}) e^{j[\omega - (2\pi k/MT)]t_m} \right] e^{-j\omega t_m} \] (3.42)

Let \( r_m \) be the ratio of \( mT - t_m \) to the average sampling period \( T \), which is

\[
t_m = mT - r_m T \quad (3.43)
\]

then we can rewrite eq. (3.42) as
Since the Fourier transform of the sinusoidal input with the frequency \( f_0 \), is

\[
X'(\omega) = 2\pi \delta(\omega - \omega_0) \text{ and } \omega_0 = 2\pi f_0
\]

eq. (3.44) becomes

\[
X(\omega) = \frac{1}{T} \cdot \sum_{k=-\infty}^{\infty} A(k) 2\pi \delta[\omega - \omega_0 - k\left(\frac{2\pi}{MT}\right)]
\]  
(3.46)

where

\[
A(k) = \sum_{m=0}^{M-1} \left[ \frac{1}{M} e^{-jr_m2\pi f_0 f_s} \right] e^{-jkm(2\pi/M)} .
\]  
(3.47)

From eq. (3.46) and (3.47), we can find some important consequences of timing offset in the multi-channel A/D converter with sinusoidal input. First, from (3.47), the sequence \( A(k) \) is periodic on \( k \) with the period \( M \), hence the spectrum \( X(\omega) \) given by eq. (3.46) is periodic on \( \omega \) with a period equal to \( 2\pi/T \) (= \( 2\pi f_s \)). The \( M \) line spectra uniformly spaced on the frequency is comprised in one period of the spectrum with neighboring spectra separated by the \( f_s/M \). The main signal is located at \( f_0 \) and the magnitude is \( A(0) \), while the \( m \)-th spectral line is located at \( f_0 + (m+M)f_s \) and with magnitude \( |A(m)| \) as shown in Figure 3-16. Since \( A(k) \) in eq.
(3.47) is a discrete Fourier transform of the sequence of \[ \{ 1 / M e^{-j \frac{2\pi f_0}{f_s} m}, \ m = 0, 1, 2, \ldots, m-1 \}, \] by Parseval’s theorem,

\[
\frac{1}{M-1} \sum_{k=0}^{M-1} |A(k)|^2 = 1.
\] (3.48)

Therefore, the signal-to-noise ratio \( S/N \), due to timing offset sampling in the multiple-channel [29], can be expressed as

\[
S/N = 10 \cdot \log_{10} \left( \frac{|A(0)|^2}{1 - |A(0)|^2} \right) \text{ dB}.
\] (3.49)

Let’s consider the A/D converter with two channels. By definition of \( r_m, r_0=0 \) and
\[ |A(0)|^2 = \cos^2(\pi r_1 f_0 / f_s) \]  
(3.50)

and from eq. (3.49), we have

\[ S/N = 20 \log_{10}(|\cot(\pi r_1 f_0 / f_s)|) \text{ dB} \]  
(3.51)

where \(-1/2 < r_1 f_0 / f_s < 1/2\) assuming that the average sampling frequency \(f_s\) is greater than the Nyquist frequency \((f_0 / f_s < 1/2)\).

### 3.6.2 Offset and gain mismatch between the channels

The gain and offset mismatches among the channels can be modeled as parallel ADC with different conversion gain and offset as shown in Figure 3-17.

---

Figure 3-17  Model for the ADC in \(i\) th channel with gain and offset mismatch

\[-1 < r_0 < 1, \text{ hence,} \]

\[ |A(0)|^2 = \cos^2(\pi r_1 f_0 / f_s) \]  

and from eq. (3.49), we have

\[ S/N = 20 \log_{10}(|\cot(\pi r_1 f_0 / f_s)|) \text{ dB} \]

where \(-1/2 < r_1 f_0 / f_s < 1/2\) assuming that the average sampling frequency \(f_s\) is greater than the Nyquist frequency \((f_0 / f_s < 1/2)\).
The transfer characteristics of two converters with offset and gain mismatch between two channels and the best fit line minimizing error power for each transfer curve is depicted in Figure 3-18. The error in ADC of $i$ th channel can be represented as

$$
\varepsilon_i(x) = \delta_i(x) + \Delta_i(x)
$$

(3.52)

where

$$
\delta_i(x) = \hat{x}_i + (a_i x + b_i)
$$

(3.53)

and

$$
\Delta_i(x) = (a_i + a_{\text{min}}) x + b_i - b_{\text{min}}
$$

(3.54)
in which \( \hat{x}_i \) is the quantized level of \( x \), and \( a_i \) and \( b_i \) are error minimization terms corresponding to the best fit converter gain and offset. In eq. (3.52), (3.53), and (3.54), \( \delta_i(x) \) indicates that the error would exist if the ADC in \( i \) th channel were used alone, while \( \Delta_i(x) \) indicates an additional error which exists when the ADC in \( i \) th channel is used as part of a parallel converter. The best fit gain and offset of the ADC in \( i \) th channel is represented by \( a_i \) and \( b_i \), while the best fit gain and offset of the whole parallel converter is given by \( a_{\text{min}} \) and \( b_{\text{min}} \). The average error power for an \( M \) channel converter[2] is represented as

\[
E_p = \frac{1}{m} \sum_{i=1}^{m} \left[ \langle \delta_i^2 \rangle + \langle \Delta_i^2 \rangle \right] .
\]  

(3.55)

From eq. (3.55), the distortion due to the gain mismatch \((a_i)\) and offset mismatch \((b_i)\) and the distortion due to each ADC can be calculated respectively. Therefore, the signal-to-distortion ratio of ADC [71] in Figure 3-17 is represented as

\[
SNR = -10 \log_{10} \left( \frac{\sigma_a^2}{\sigma_b^2} + \frac{2\sigma_b^2}{A^2} \right)
\]

(3.56)

where \( \sigma_a^2 \) is a variance of gain and \( \sigma_b^2 \) is a variance of offset in each channel of ADC, and \( A \) is an amplitude of sinusoidal input.

Figure 3-19 illustrates a reconstructed spectrum of sinusoidal input with offset mismatches and gain mismatch among the \( M \) channel of ADC. Assume that the sampling periods are uniform and the input sinusoidal magnitudes are different in each channel (Figure 3-17) such that the sequences of input sinusoids are \( a_i e^{j\omega_0 T} \),
Figure 3-19  Reconstructed spectrum of sinusoidal input (a) offset mismatch (b) gain mismatch

\[ a_2 e^{j\omega_0 (2T)} , ... , a_{M-1} e^{j\omega_0 (M-1) T} , a_M e^{j\omega_0 MT} , ... \] and \( r_m = 0 \), the \( A(k) \) in eq. (3.47) can be rewritten as

\[
A(k) = \sum_{m=0}^{M-1} a_m e^{-jkm (2\pi / M)}
\]  

(3.57)

for the gain mismatches in \( M \) channel case as shown in Figure 3-19 (a). Therefore,
from eq. (3.46) we can note that the frequency of spurious tones are the same as that of non-uniform sampling case such that the frequency of spurious tone is at \( f_s/M \pm f_{in}, 2f_s/M \pm f_{in}, \ldots, (M-1)f_s/M \pm f_{in} \).

The offset mismatch among the channel generates a fixed pattern noise. In the frequency domain this is manifested as frequency tone at multiples of \( f_s/M \) as shown in Figure 3-19 (b), because the offsets \((b_k)\) can be interpreted as a periodic signal with \( M/f_s \) period sampled at the frequency \( f_s \).

The simulated total distortions due to gain and offset mismatch in 2-channel with ideal ADC model are shown in Figure 3-20. The gain is matched to better than 0.1% and the offset is less than 0.5 mV in 1.0 V input full scale so that the total distortion from gain mismatch and the tone due to fixed pattern noise are less than -65 dBc, respectively.

### 3.7 Signal dependent clock feed through

The signal dependent charge feed through in analog MOS switches causes distortion. The analytic expression and characterization for the switch induced error voltage on a sampled capacitor has been studied in [81] and [103]. In order to avoid the problem from voltage dependent clock feed through, dummy switches[14] and the transmission gate[101] have been investigated. But using those methods can not cancel this effect perfectly due to mismatch and randomness in the device.

The systematic way to reduce voltage dependant clock feed through is by
Figure 3-20  (a) SFDR with gain mismatch in 2 channel ADC  (b) SFDR with offset mismatch in 2 channel ADC with ±1 V full scale input
using bottom-plate sampling [43][44][66][90]. The two different $\phi_1$ and $\phi_{1d}$ clock signals are used instead of single $\phi_I$ clock signals to cancel the voltage-dependent charge injection from the sampling switch ($S_{\text{smpl}}$), as shown in Figure 3-21. At the end of $\phi_I = “1”$, the unit gain feedback switch $S_s$ will inject the charge $Q_s$ to node
$V_e$. At the end of $\phi_{1d}$, the sampling switch $S_{\text{smpl}}$ injects the charge $Q_{\text{smpl}1}$ and $Q_{\text{smpl}2}$ which cause the signal voltage-dependent charge injection, to node $V_e$, and the injected charge $Q_{\text{smpl}1}$ and $Q_{\text{smpl}2}$ are stored at a parasitic capacitor $C_{ip}$ and $C_{sp}$. The sampling capacitor, $C_{\text{smpl}}$ memorizes the amount of charge ($Q_{\text{smpl}1}$) flowing through $C_{\text{smpl}}$ as a voltage difference on the sampling capacitor. Assuming the DC gain is infinite and the offset at the input is negligible, the injected charge due to $S_s$, $Q_s$, is constant all the time and is independent of the input voltage. During phase $\phi_2$= “1”, the input signal charge and the signal dependent injection charge ($Q_{\text{smpl}1}$) stored in $C_{ip}$ are removed through $C_{in}$ to ground. Since the charge due to the input signal voltage dependent injection does not come from the feedback capacitor ($C_f$) but from a stored charge at $C_{ip}$, the input signal voltage dependent charge injection from the sampling switch does not effect the output voltage. Also, the part of input signal voltage dependent injected charge ($Q_{s2}$) does not effect the output voltage because both terminals of the parasitic capacitor ($C_{sp}$) are connected to a low impedance node.

If this scheme is implemented in a fully differential circuit, differential injected charge due to $S_s$ ($Q_s$) is cancelled out by the opposite side injected charge due to $S_s$. Therefore, the differential output is not effected by the charge injected from the switches.
3.8 Metastability

Metastability is a phenomenon typically associated with binary digital logic system, particularly those using flip-flops for synchronization of signals. A latch is expected to store two distinct states, representing a logic 1 and a logic 0. All flip-flops are also capable of generating a third, indeterminate level between 1 and 0 levels. This can occur when setup and hold times are violated, causing a clock edge to occur while an input signal is still in transition. The intermediate state is described as being metastable because the condition will eventually decay, not necessarily in a monotonic fashion, to one of the valid logic levels. The metastability problem has been analyzed by theoretical approaches and measurement [24][26][77][98] to focus on the understanding of the phenomena and by ac small signal analysis to optimize a latch or flip-flop [33].

Metastability has long been understood as a limitation in the design of high-speed converters because the comparator occasionally could not have enough time to resolve a small differential input to a valid logic level in a short clock cycle. To reduce errors arising from comparator metastability, the comparator architecture with cascaded latches [45] and cascaded sub-comparators [109] have been reported. In addition, the latch with a series of connected M/S flip-flops has been analyzed [18].

The probability that a cascade of two latches as shown in Figure 3-22(a) is in a metastable state can be explained as follows. First, consider a single latch case.
Figure 3-22  (a) Comparator with preamplifier and cascade of two latch with time constant $\tau_1$ and $\tau_2$  (b) Latch schematic during regeneration  (c) Transient response of the latch during regeneration phase  (d) Metastability region in coarse quantizer with 15 comparator
When the latch is switched from reset mode to regenerative “latch” mode as shown in Figure 3-22(b), the output voltage can be approximated by a simple expression[98]:

\[ V_0 = AV_i \exp \left( \frac{t}{\tau} \right) \]  

(3.58)

where \( V_0 \) is the output of the latch, \( A \) is the gain in “reset” mode, \( V_i \) is the input voltage at the start of regeneration, \( t \) is the time since the onset of positive feedback, and \( \tau \) is the time constant of the latch in positive feedback. The output voltage roughly follows this exponential growth until it reaches the valid logic level as shown in Figure 3-22(c). During this period, we can consider the regenerative circuit to have an effective gain which is a function of time:

\[ A_{eff} = \frac{V_0}{V_i} = AV_i \exp \left( \frac{t}{\tau} \right). \]  

(3.59)

As the clock rate of the ADC is increased, the amount of time the latch spends in positive feedback is reduced and the effective gain reached at the end of half a clock cycle is lower. A lower effective gain makes it more likely that an input voltage will be too small to be amplified to a full logic level, and thus increases the chances for an error. The effective gain \( A_{comp} \) of a comparator in Figure 3-22 (a) is:

\[ A_{comp} = A_{preamp} \left[ A_1 \exp \left( 2T/\tau_1 \right) \right] \left[ A_2 \exp \left( 2T/\tau_2 \right) \right] \]  

(3.60)

where \( T \) is the period of clock (\( \phi \)), \( \tau_1 \) and \( \tau_2 \) are the time constant of each latches, \( A_1 \) and \( A_2 \) are the gains in “reset” mode and \( A_{preamp} \) is a preamplifier gain. Since the metastable state occurs around each threshold of the comparator as shown in Figure
3-22 (d), the probability ($P_{\text{metastable}}$) that the comparator output is at metastable condition depends on the number of thresholds in the quantizer. Therefore, $P_{\text{metastable}}$ can be calculated:

$$P_{\text{metastable}} = \frac{(\text{Valid digital level})}{A_{\text{comp}}} \cdot \frac{\text{(full scale)}}{2^N}. \quad (3.61)$$
Chapter 4

System and Circuit Design

This 10-bit 100 M Samples/sec ADC is focused on how to reconfigure the architecture of a paralleled, pipelined ADC to solve all three of the known limitations discussed in the previous chapter, that is the timing skew, the gain mismatch of residue amplifier, and the offset mismatch between the channels in paralleled ADC architecture. To achieve a 10-bit, 100 MS/s in 1.0 µm CMOS technology, a 2-channel, 3-stage ADC with a single non-resetting sample-and-hold amplifier and a reconstruction DAC at the front end has been used, as shown in Figure 4-1. The underlying rationale of this architecture are as follows. A non-resetting full-speed (100MHz) single sample-and-hold at the front-end generates a held output which is distributed to both channels, thus avoiding the problems of timing skew. The front S/H and reconstruction DAC are optimized to run at the full speed because these are the most sensitive parts of the ADC to gain and offset.
Figure 4-1  Block Diagram of Architecture
mismatches as shown in Figure 3-20. The S/H circuit, using passive sampling for large bandwidth, might face a larger offset than the active sampling using an offset cancellation (or auto-zero) scheme. The offset mismatch between the residue amplifier has been reduced by applying an offset canceling scheme to each residue amplifier. Since the offset canceling is an active sampling scheme which requires a unit gain feedback, it takes more time than passive sampling. The bandwidth of unit gain feedback is 300MHz and that of S/H is 250MHz. Since the resetting S/H amplifier allows 5ns for following amplifier to sample its output, the minimum bandwidth requirement of the cascade of S/H and sampling circuit is 200 MHz. Therefore, it is very difficult to implement in a single channel. However, it is possible to accomplish this using non-resetting S/H, because the S/H output does not reset between samples, allowing the full clock period (10ns) for the residue amplifier in two channels to operate on the held sample. The other source of the distortion in the parallel pipeline architecture is the gain mismatch between the residue amplifier. As shown in Figure 4-2, a pipeline consisting of 1~2 bit/stage will suffer from the gain mismatch because the capacitor can be matched up to 0.1%. Since our goal is to achieve a high conversion rate without extensive trimming, a conversion of 3-bits/stage has been chosen, even though the converting multi-bit/stage will dissipate more power than 1-bit/stage to obtain constant bandwidth with larger gain.

A full-speed 4-bit quantizer and reconstruction DAC follows the
non-resetting S/H, distributing the residue to time-interleaved channels. Subsequently, the residue amplifier output needs to be quantized only to 7-bits, which means that a of gain error of up to 1% can be tolerated. Since the capacitor mismatch is about 0.1~0.2%, the residue amplifier gain mismatch due to the capacitor in the 4-bits/stage conversion does not adversely effect accuracy. However, since a residue amplifier input-referred inter-channel offset mismatch is 1 mVrms from the measurement of various device mismatches, which can cause a
tone larger than 60 dBc at 2 Vp-p input full scale, a programmable inter-channel offset correction circuit has been added to keep the tone below -65dBc from the input signal. This offset correction circuit has been inserted at the second residue amplifier, where the sensitivity is the lowest to errors in this circuit.

Once the residue signal, which is the difference between S/H output and reconstruction DAC, is interleaved into two channels, then the residue signal is processed at half of the full speed, 50MHz in each channel. Since the ADC converts 4-bits/stage, the required residue amplifier gain is 8, which is impossible to achieve in 1µm CMOS at 50 MHz clock. This problem is overcome by using a cascade of gain-of-2 and gain-of-4 amplifiers where the each gain-of-2 amplifier output distributes its output to two gain-of-4. This breakdown will keep the gain-bandwidth constant, as shown in Table 4.1. However, the second bank of residue amplifiers prior to the third quantizer consists of a gain-of-2 amplifier cascaded with a gain-of-4 amplifier, both operating at 50MHz. Here, an incomplete settling is no longer a source of inaccuracy in the final 4b quantizer. And at the last gain-of-4 amplifier, a binary-weighted array of small capacitors injects programmable

<table>
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<th>Table 4.1 Gain-bandwidth of linear component</th>
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</tr>
<tr>
<td>S/H</td>
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<tr>
<td>Gain-of-2 RA</td>
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<tr>
<td>Gain-of-4 RA</td>
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...
correction charges derived from a DC reference into the input of gain-of-4 amplifiers for correction of inter-channel offset. Since the gain-of-4 amplifiers in the first residue amplifier bank operate at 25MHz, there will be one more tone at $f_s/4$ in addition to $f_s/2$. However, the offset mismatch between two gain-of-4-amplifiers in the first gain-of-8 residue amplifier bank is reduced by the gain of the gain-of-2 amplifier so that the input referred offset mismatch in the two gain-of-4-amplifiers is negligible. The tone at $f_s/4$ was less than -70 dBc from the measurements on a test chip, so an offset cancellation circuit is added only to reduce a $f_s/2$ tone.

Since the second and third 4-bit quantizers operate at half of the full speed, 50MHz, the bandwidth of the preamplifiers before the comparators may be reduced in principle. In general, if the output load is fixed, the bandwidth linearly depends on the size of the device. Unfortunately, this is not possible in practice. The random offsets of the comparators depend on the size of the input differential pair. Instead of scaling the preamplifier, the input capacitance of the quantizer can be reduced to almost half, and the power dissipation at the preamplifier can be reduced significantly, by utilizing an interpolation scheme in the first stage preamplifier output. In addition, the offset variation of the comparator with interpolation becomes less than that of the comparator without interpolation. However, since each preamplifier has to drive a larger capacitive load, the settling time of the preamplifier can be longer.
Each quantizer encodes its output as Gray code, and one bit of the output is dedicated to error-correction between quantizers. The 4-bit digital output obtained from the first quantizer is interleaved in the two digital paths. In each digital path, the two additional 4-bit digital outputs emerging from the second and third quantizers are merged into the error correction circuit (ECC), in addition to the 4-bits digital output obtained from the first quantizer. The digital error correction circuit uses information from the extra 2-bits and provides a digitally error-corrected 10-bit digital output. All the error-correction logic and pipeline delay registers are on-board.

The ADC digital outputs were provided outside of the chip with two complementary 10-bits two 50MHz channels to make it easy to acquire the data. Differential output buffers drive ECL logic levels into a remotely terminated logic analyzer, without producing large data-dependent current glitches on the chip power supply.

4.1 Timing and requirement of system

The operation of the ADC converter is best understood with a timing diagram. Figure 4-3 illustrates the timing diagram of the ADC front end referenced to a 100 MHz conversion rate. A capacitor and switch acquires a sample of the balanced input voltage $t = 5$ ns, and at $t = 10$ ns, the capacitor connects in feedback around the S/H op amp. The first 4-bit quantizer follows the S/H output from $t =10$
to 15 ns, and is then strobed. The quantizer output code, which is ready at about
\(t = 16\) ns, is stored in the master flip-flop and the slave flip-flop selects one tap from
a 4-bit resistor ladder DAC to reconstruct itself as an analog threshold at 20 ns.

Meanwhile, over \(t = 10\) to 20 ns, the gain-of-2 amplifier, for example, in channel 2 is
in reset mode while its input capacitor is following the S/H op amp output. At
\(t = 20\) ns, this capacitor connects to the reconstruction DAC output, and the op amp
goes into amplify mode, thus amplifying the different charges, which constitutes the
residue. Over this duration, the corresponding amplifier in channel 1 settle to 2

Figure 4-3  Timing Diagram of ADC front end
times the previous sample’s residue, and then starts to follow the next S/H output.

The 10-bit ADC requires that the output of input S/H be linear to better than 10-bit, and the 15 thresholds of the first reconstruction DAC should be at least 10-bit accurate. There is no strict requirement on gain accuracy of the input S/H, because a variable gain amplifier (not shown) located in front of the ADC would adjust its gain to fully load the ADC input. Similarly, a fixed input offset of the ADC is tolerable.

Figure 4-4 (a) illustrates the block diagram of the first residue amplifier bank. The residue signal amplified by the gain of 2 amplifiers is interleaved to the gain of 4 amplifiers, as shown in Figure 4-4 (b). Therefore, the clock period of the gain-of-4 amplifier can be two times longer than that of the gain-of-2 amplifier and 4 times longer than that of the S/H amplifier. Although each amplifier output returns to zero for offset cancellation, the multiplexed output of the gain-of-4 stages amplifier bank does not return to zero.

The gain of the first bank of residue amplifiers is sufficiently accurate to align its full-scale output voltage with the reference of the subsequent quantizer within ± 1/2 LSB at 7-bits. Although their input-referred offset may be any reasonable value, the difference in these offsets between the channels should be less than 1/2 LSB at 10-bits to avoid a noticeable fixed-pattern at the output. As mentioned before, there is a provision for programmable correction for an inter-channel offset difference at the last residue amplifier.
Figure 4-5 (a) illustrates the block diagram of the 7-bit pipeline subconverter block in each channel. The second and third 4-bit quantizers use interpolation to reduce their input capacitance. The quantizer input capacitance and the wiring capacitance are the only load to the previous gain-of-4 amplifier during the first half of 20 ns, from 0 ns to 10 ns, while the following amplifier is in amplify
mode during the first half of each 50 MHz clock cycle, as shown in Figure 4-5 (b). Therefore, the output of the first residue amplifier bank can settle quickly during the first half of the 20 ns period because the sampling capacitor of the gain-of-2

Figure 4-5  7 bit pipeline converter
(a) block diagram (b) timing diagram
amplifier in the third stage does not capacitively load the gain-of-4 amplifier in the second stage. During the second half of the period, the following gain-of-2 amplifier in the third stage is switched in and samples the output of the gain-of-r amplifier in the second stage. After the gain-of-4 amplifier in the first residue amplifier bank, the timing diagram of the second and subsequent quantizers are similar to that of the first quantizer except the clock is running at half of the full-speed, 50 MHz.

This chip requires only one 100 MHz clock from the externally-supplied clock generator, and it internally generates two non-overlapping phases at this frequency, as well as two phases at one-half and one-fourth this frequency.

4.2 Non-resetting Sample-and-Hold amplifier

The input sample-and-hold (S/H) must provide a balanced, non-reset output, and must be capable of acquiring a new sample every 10ns. Let’s assume that a resetting S/H is used with a 50% duty cycle. Within a 5 ns period, the S/H amplifier should settle to a sampled output. This sampled output has to drive a preamplifier of the comparator whose output should settle at least 4-bit resolution, and the latch has to regenerate a thermometer code from this preamplifier output, as shown in Figure 4-6 (a) [42][61]. This idle time (during sampling period) of the S/H amplifier is shortened by introducing an analog double sampled pipeline scheme by the cascading of two conventional resetting unity-gain S/H amplifiers where the
Figure 4.6 Block diagram and timing diagram of (a) resetting S/H (b) double resetting S/H (c) non-resetting S/H.
latter one is delayed by a half clock cycle as shown in Figure 4-6 (b) [50]. The output of the first S/H drives the first quantizer, while the output of the second one drives the residue amplifier.

These two resetting S/H amplifiers can be replaced by a non-resetting S/H circuit [64] which allows a full 10 ns period for the following amplifier to sample and cancel an offset from itself using an auto-zeroing scheme, as shown in Figure 4-6 (c). The fully differential non-resetting S/H amplifier is realized with 6 capacitors, unlike the 2 capacitors in the resetting amplifier shown in Figure 4-7. The capacitor values of C3(C4) should be equal to that of C5(C6), while the capacitor values of C1(C2) can be different from C3(C4) and C5(C6). The operation of the S/H amplifier can be explained in three different stages, even though its operation repeats every two clock phase.

Figure 4-7  Non-resetting sample and hold amplifier
Figure 4-8  Non-resetting sample and hold Amplifier: (a) at $\phi_1$, (b) at $\phi_2$
1. Sampling period (Figure 4-8 (a)): s1(s3) and s5(s7) are closed, s2(s4) and s6(s8) are open, and \( \text{Vin}^+ [nT] \) (\( \text{Vin}^- [nT] \)) is sampled in capacitor C1(C2).

2. Transfer period (Figure 4-8 (b)): C1(C2) is switched into a feedback path, C5(C6) is connected to the input of the amplifier. C5(C6) is used so that the sampled charge on C1(C2) can be transferred to the output without interference by the holding capacitor C3(C4). The charge from the holding capacitor C3(C4) will be cancelled by that of C5(C6), and C3(C4) will be charged up to the new value, \( \text{Vin}^+ [nT] \) (\( \text{Vin}^- [nT] \)).

3. Holding period (Figure 4-8 (a)): The C1(C2) and C5(C6) are disconnected from the feedback path of the amplifier and the C3(C4) is holding the charge from the last phase. Therefore, the output value of the amplifier will be the same as the last phase output \( \text{Vin}^+ [nT] \) (\( \text{Vin}^- [nT] \)). The C1(C2), which is disconnected from the amplifier, is sampling the next available input \( \text{Vin}^+ [(n+1)T] \) (\( \text{Vin}^- [(n+1)T] \)).

These operations can be explained by the following equation. During(\( \phi 2 \))

\[
(C1 + C3) \cdot V_{out}^+ \left[ \left( n + \frac{1}{2} \right) T \right] + C5 \cdot V_{out}^+ \left( \left[ \left( n + \frac{1}{2} \right) T \right] \right) = C1 \cdot V_{in}^+ [nT] + C3 \cdot V_{out}^+ [nT] + C5 \cdot V_{out}^- [nT]
\]

Since \( V_{out} = V_{out}^+ = -V_{out}^- \),

81
During $\phi_1$, 

$$V_{out}\left[\left(n + \frac{1}{2}\right)T\right] = \frac{C1}{C1 + C3 - C5} \cdot V_{in}[nT]$$

$$+ \frac{C3 - C5}{C1 + C3 - C5} \cdot V_{out}[nT]$$

and $C3 = C5,$

$$V_{out}\left[\left(n + \frac{1}{2}\right)T\right] = V_{in}[nT]$$

During $\phi_1$

$$V_{out}\left[\left(n + 1\right)T\right] = V_{out}\left[\left(n + \frac{1}{2}\right)T\right] = V_{out}[nT].$$

Therefore, the eq. (4.3) and (4.4) demonstrate that the output of the non-resetting S/H is held constant from $\phi_2$ to $\phi_1$, as shown in Figure 4-3.

A switch-capacitor passive circuit tracks and samples the input (passive sampling). Because the bandwidth is determined by the on-resistance of the switch and the sampling capacitor, the passive sampling circuit has been successfully demonstrated that it can sample the 900 MHz signal [6][7]. Here, the bandwidth of the passive sampling circuit has been chosen to be 300MHz, which is adequate to capture the 50 MHz Nyquist input signal.

The major disadvantage of a non-resetting S/H amplifier scheme is that the hold (C3, C4) and dummy (C5, C6) capacitors in Figure 4-7 not only lower the feedback factor ($\beta$), but also act as the capacitive loading at the output, as mentioned in section 3.4.3. Therefore, the non-resetting S/H amplifier has to have larger $g_m$ at the input differential pair than the conventional resetting S/H amplifier. Figure 4-9
illustrates the feedback configurations of non-resetting S/H and resetting S/H in Figure 4-6 (b) where two resetting S/H are used. Assume the resetting amplifier has been down scaled by half of the non-resetting amplifier so that total power dissipation in the front end are equal. Therefore, the following equation can be assumed:

\[
\tau_{NR} \equiv \beta_{NR} g_{mNR} / C_L
\]

\[
N_{NRO} \equiv N_{NI} / \beta_{NR}
\]

\[
\tau_{R} \equiv \beta_{R} g_{mR} / C_L
\]

\[
N_{NRO} \equiv N_{Ri} / \beta_{R}
\]
\[ g_{mNR} = 2 \cdot g_{mR} \]
\[ N_{NRi} = \frac{1}{\sqrt{2}} \cdot N_{Ri} \]  \hspace{1cm} (4.5)

where \( g_{mNR} \) and \( g_{mR} \) are the transconductance of differential pair of non-resetting S/H and resetting S/H, and \( N_{NRi} \) and \( N_{Ri} \) are the input referred noise in non-resetting S/H and resetting S/H, respectively. The feedback constant of non-resetting S/H and resetting S/H are represented as follows;

\[ \beta_{NR} = \frac{C_1}{C_1 + C_2 + C_{2d} + C_p} \]
\[ \beta_R = \frac{C_1}{C_1 + C_p} \]  \hspace{1cm} (4.6)

Assume the feedback capacitors \( C_1, C_2, C_{2d}, \) and \( C_p \) are equal value for simplicity, the eq. (4.6) becomes

\[ \beta_{NR} = \frac{1}{4} \]
\[ \beta_R = \frac{1}{2} \]  \hspace{1cm} (4.7)

The settling time constant of non-resetting S/H and resetting S/H, \( \tau_{NR} \) and \( \tau_R \), are

\[ \tau_{NR} = \beta_{NR} \cdot g_{mNR} / C_L = \frac{1}{4} \cdot g_{mNR} / C_L \]
\[ \tau_R = \beta_R \cdot g_{mR} / C_L = \frac{1}{2} \cdot g_{mR} / C_L \]  \hspace{1cm} (4.8)

From eq. (4.5), \( \tau_{NR} \) and \( \tau_R \) are equal if the load capacitor \( C_L \) is much greater than the feedback capacitors, which is true in most cases. The output noise of the non-
resetting S/H is given by $N_{NRo}$ while the output noise of the resetting S/H is given by $N_{Ro}$. Both values are calculated by taking the input referred noise and dividing it by the feedback factor of the amplifier, $\beta$. This is shown in eq. (4.9). As the feedback is decreased, the gain and the output referred noise of the amplifier increase.

$$N_{NRo} = N_{NRi} / \beta_{NR} = 4 \cdot N_{NRi}$$
$$N_{Ro} = N_{Ri} / \beta_{R} = 2 \cdot N_{Ri} \tag{4.9}$$

Using simple models of the two sample and hold circuits, it can be shown that the input referred noise of the resetting and the non-resetting S/H are equal. Since $N_{NRi} = \frac{1}{\sqrt{2}} \cdot N_{Ri}$, due to the $g_m$ argument in eq. (4.5), and $\beta_{NR}$ is smaller, as given in eq. (4.6), the S/H input referred noise of the non-resetting S/H is 40% more than that of the resetting S/H during the first half of the period. During the second half period, the feedback configurations are equal but once again $N_{NRi} = \frac{1}{\sqrt{2}} \cdot N_{Ri}$. Therefore, during the second half of period, the noise of the resetting S/H is 40% more than that of the non-resetting S/H. In the non-resetting S/H, the holding capacitor C3 (C4), shown in Figure 4-8, samples the output noise during the transfer period, and sums up the output noise during hold period in a rms fashion. Therefore, the total ADC input referred noise of the non-resetting S/H is similar to the total input referred noise of the resetting S/H. Additionally, the resetting S/H output is valid only for 5 ns with a 100 MHz conversion rate, it is very difficult for the following residue amplifier to sample the S/H output while it is
canceling the offset. A summary of the non-resetting S/H is given in Table 4.2.

Table 4.2  Simulation summary of non-resetting S/H amplifier at 70°C

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Differential input full scale</td>
<td>± 1.0 V_p-p</td>
</tr>
<tr>
<td>Input capacitance</td>
<td>2.2 pF</td>
</tr>
<tr>
<td>Single end output range</td>
<td>2.1 ~ 3.3 V</td>
</tr>
<tr>
<td>Sampling bandwidth</td>
<td>300 MHz</td>
</tr>
<tr>
<td>Power dissipation</td>
<td>140 mW</td>
</tr>
<tr>
<td>SDR</td>
<td>67.8 dB</td>
</tr>
<tr>
<td>3rd harmonic</td>
<td>-71.5 dBc</td>
</tr>
</tbody>
</table>

The on-resistance of S_1 and S_3 in Figure 4-7 can introduce a harmonic due to the variation of the input voltage. This distortion can be minimized by choosing a large switch size or by selecting a proper PMOS and NMOS switch size ratio so that the on-resistance of the CMOS switch is constant in the maximum input signal range. The other source of distortion is the voltage dependant clock feedthrough. This distortion is eliminated to the first order, providing a 2 phase clock with a delayed edge is used for bottom-plate sampling.

4.3 A 4-bit AD-DA

The 4-bit AD-DA block consists of a differential 4-bit quantizer, two resistor ladders, a bank of differential DAC switches, and a 4-bit Gray code encoder, as shown in Figure 4-10. The 4-bit quantizer is made of 15 comparators.
and a resistor ladder. Each comparator has a 4-input preamplifier, latch, and master-slave flip-flop (F/F). The DAC consists of a bank of NOR gates, switches and a resistor ladder.

The sampled signal from the non-resetting S/H output is latched to 15 comparators at the middle of each period. Then the comparator output is latched to the F/F and the latched data are converted to thermometer code. The NOR gate is arranged so that the NOR output can select one of the 16 DAC switches based on the thermometer code, and is fed to the input of the Gray encoder.

Figure 4-10  4 bit AD-DA Block Diagram
4.3.1 Comparator circuit

The fast, low latency quantizer used in all blocks comprises comparators to amplify the difference between the balanced analog input and differential taps from a resistor ladder. There are 3 major design issues in a comparator circuit in this ADC architecture. The first issue is high operation speed, because it should quantize data at full speed, 100 MHz, in the first ADDA block. The second is small kick-back to the reference ladder. The kick-back from the latch circuit during regeneration disturbs the resistor ladder and will cause a longer DAC output settling time. The last consideration is to minimize offset of comparator threshold voltage.

To address these issues, the 2-stage preamplifier followed by a latch has been designed, as shown in Figure 4-11. The advantages of using a 2-stage amplifier are as follows. First, the offset variation due to the random device mismatch and the asymmetry of layout in the latch circuit can be reduced by a preamplifier gain. Therefore, the preamplifier gain is determined so that the offset contribution from the latch is less than those from the preamplifier. The second reason is that a 2-stage preamplifier can reduce kick-back from the latch during a regeneration period more effectively than a single stage. A cascaded gain stage is one of the best ways to achieve a wide-band amplifier. The last reason is that a 2-stage preamplifier can be easily modified in layout to implement an interpolation scheme in second stage preamplifiers and latches.

The sampled input (Vin+) and the reference voltage (Vref+) are applied to
one side of the differential pair and the opposite pair of the sampled input (Vin⁻), and the reference voltage (Vref⁻) are applied to the other side of the differential pair, as shown in Figure 4-12. The preamplifier senses the difference between two balanced inputs by subtracting the output currents of two differential pairs, and amplifies it by 5 times prior to the latch input. If the S/H has a -3 dB bandwidth of 200 MHz, the preamplifier should also have a 160 MHz -3 dB bandwidth so that the

Figure 4-11 Comparator Circuit
preamplifier output can settle its output in ± 1/2 LSB of 4-bits in 5 ns. The cascade of two stages results in a 250 MHz preamplifier, which is sufficiently wideband to track a full-scale Nyquist frequency input.

There are two different ways to arrange the input differential pair. One way is by connecting balanced input, Vin+ and Vin-, in one differential pair and balanced reference, Vref+ and Vref-, in the other pair, as shown in Figure 4-13 (a). The other is by connecting Vin+ and Vref+ in one differential pair and Vin- and Vref- in the other pair, as shown in Figure 4-13 (b). The advantage of using the latter scheme is that the differential pairs in the critical comparator detecting the closest
threshold to the input are always biased close to maximum gain and bandwidth. The preamplifier at each end in the former scheme has to compare the largest reference difference with the input. The differential pair in that preamplifier is biased so that the only small part of the tail current flows to the one of differential pair, which decreases the transconductance ($g_{m}$) of the differential pair and the preamplifier gain. Therefore, the input referred offset from the latch circuit becomes unacceptably large.

The latter preamplifier is used. The output common-mode of the S/H is slaved to the common-mode voltage of the ladder (its center tap). Any error or noise in these common-mode values is, in any case, subtracted at the comparator output. However, the input common-mode range of the preamp first stage must be nominally equal to the reference full-scale.

Figure 4-13 First stage preamplifier schematic (a) applying differential input in one differential pair (b) applying differential input in each differential pair, respectively
The simulated characteristics of the comparator are summarized in Table 4.3. Two type of simulation has been performed to ensure that the quantizer has a 4-bit linearity. The one type of the offset is due to the device mismatch such as threshold (Vt), device parameter, \( \beta \) (= \( \mu \cdot C_{\text{ox}} \cdot W/L \)), in the MOSFET. The other type is dynamic offset to the recovery from the overdrive. With this gain and with careful latch design to avoid a large common-mode jump when it is strobed, the comparator offset due to device mismatch is determined by the input differential pairs. The Monte Carlo simulation to find a random threshold offset mismatch at the comparator input uses the parameters specified in Table 4.4 [69]. The dynamic offset is an overdrive value to get the correct latch output when the input is changing from maximum to minimum in one clock period. The simulated dynamic offset in

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \Delta \beta ) (%)</td>
<td>( \frac{2}{\sqrt{W \cdot L}} )</td>
</tr>
<tr>
<td>( \Delta V_t ) (mV)</td>
<td>( \frac{15}{\sqrt{W \cdot L}} )</td>
</tr>
</tbody>
</table>

Table 4.3 Comparator specification

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Designed Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>-3dB BW</td>
<td>&gt; 250 MHz</td>
</tr>
<tr>
<td>DC Gain at zero-crossing</td>
<td>&gt; 5</td>
</tr>
<tr>
<td>Input Offset(( \sigma ))</td>
<td>6.8 mV</td>
</tr>
<tr>
<td>Input Cap</td>
<td>55.7 fF</td>
</tr>
<tr>
<td>Power Diss</td>
<td>5.8 mW</td>
</tr>
</tbody>
</table>
this system is 40 mV with a full input swing of ±1.0 V.

### 4.3.2 Latch Circuit

The dynamic and static types of latch has been reviewed (Appendix A). The dynamic latch (Figure 4-14 [35]) does not dissipate static power, but only power momentarily during the phase transition. The input differential pair (M1, M2) of the dynamic latch, which is normally off, turns on for the comparison at the phase transition. The gate capacitance change in the differential pair will cause a kickback, which might disrupt the exact zero-crossing information. The kickback degrades the performance of ADC, especially for multi-bit/stage subquantizer and
interpolation subquantizer. However, in high speed ADC, the power dissipation between static and dynamic latch becomes negligible. In addition, the dynamic latch is slower in regeneration than the static one because there is time delay in dynamic latch until all the transistors become active and start to regenerate the output.

The static latch is used because the major concern in designing a latch circuit as the one shown in Figure 4-15, is operation speed. During reset($\phi_1$) period, switches S1, S2, and S3 are on, $V_{out^+}$ and $V_{out^-}$ are shorted together, and the latch samples the preamplified error voltage through switches on two common-source PFETs (M1, M2), which are the loads to a cross-coupled pair of NFETs (M3, M4).

During comparison mode, $\phi_1$ goes low to strobe the latch, and all the switch
S1, S2, and S3 are off. The difference of drain currents between M1 and M2 initiates regeneration at the node Vout\(^+\) and Vout\(^-\), and the cross coupled M3 and M4 accelerate the regeneration by forming a positive feedback until the output nodes (Vout\(^+\) and Vout\(^-\)) reach the Vdd and GND. Furthermore, the bootstrap capacitor C1 and C2 speed up regeneration. The operation speed of the latch can be determined by the regeneration time constant (\(\tau\)).

\[
\tau = \frac{C_{\text{total}}}{g_{mn} + \alpha \cdot g_{mp}},
\]

(4.10)

where \(\alpha = \frac{C_1}{C_1 + C_{1p}}, g_{mn}\) of M3 (or M4), \(g_{mp}\) of M1 (or M2) and \(C_{\text{total}}\) total capacitance at Vout\(^+\) or Vout\(^-\). The source follower buffer (M5, M6, M7, M8) reduces wiring capacitance and increases capacitance matching at the output node by placing M5, M6, M7, and M8 closer to the latch output, and prevents the kickback from the F/F. The simulated regeneration time constant of the loaded latch is 0.27 ns. The width of S1 should be as small as possible because it adds parasitic junction capacitances from itself to the latch output node, and can introduce undesirable gain (Vout\(^+\)/Vin\(^-\)), decreasing the bit-error rate at the latch. However, its width should be large enough to reset node Vout\(^+\) and Vout\(^-\) at the end of the reset phase, otherwise the latch will have hysteresis.

When the latch starts to reset its output, the master flip-flop (F/F) disconnects its input from the latch output and transfers its output to the slave F/F, as shown in Figure 4-16 (a). The master F/F not only holds the latch value while the
Figure 4-16 (a) timing diagram of latch and FF (b) hysteresis of the master slave FF (c) back-to-back inverter latch
latch is resetting itself for the next sampled input, but also decreases the bit-error rate. The master slave F/F has two meta-stable regions because it has a hysteresis due to back-to-back inverter latches as shown in Figure 4-16 (b) (c). Assume the master F/F output is at “0”. Even though the latch starts to build its output in a positive direction, the master F/F output does not cross zero by at t=5ns unless the latch output is sufficiently large that it can overcome and release the back-to-back inverter F/F. In addition, the slave F/F has two meta-stable regions like the master F/F. Therefore, there exists a certain initial latch input range that drives the slave F/F output into the invalid digital output range at the end of T3 (t= 15ns), causing the meta-stable output of the comparator. This can be estimated with the invalid digital range and the regeneration time constant of the slave latch, in the same way as the latch without hysteresis. During T2, the master F/F output is disconnected from the latch output, and continuously regenerate through the back-to-back inverter F/F, whose output derives the slave F/F. Because of a 4.5ns delay from the slave output to the delay F/F in the error correction circuit, the digital output from the comparator (slave F/F) has to be in a valid digital level at approximately the end of T2 period. From the simulation results shown in Figure 4-17, the initial differential voltage $\delta$ (0.01mV) of the master F/F output is large enough to develop the slave output in valid digital levels at the end of the T2 period.

Simple direct calculation of the latch input referred metastable region (LMR) by two cascaded exponential terms can be in error, since the latch output is
buffered by the source follower, there is some delay between latch out and the master reset state. The delay is not only from the latch buffer, but also from the master itself because it has to erase the previous data and enter the reset state. However, it is impossible to exactly estimate the delays caused by each component.

The input metastable region of \( \delta \) (0.01mV) may be obtained by indirect slope mapping from the master output to the latch output. This \( \delta \) in the master F/F range can be converted to the latch output range with a certain ratio depending on the slope of the master F/F output crossing the “0” and the slope of the latch output at the delay \( (t_d) \) before. The mapped metastable region \( (\Delta V_{out}) \) is estimated as

\[
\Delta V_{out} = \exp\left(-\frac{(T-t_d)}{\tau_1}\right)
\]

![Diagram](image_url)

**Figure 4-17** Simulation result of latch and F/F
follow

\[ \Delta V_{out} = \left( \frac{slope_{latch}}{slope_{master}} \right) \cdot \delta. \quad (4.11) \]

The latch input referred metastable region (LMR) is

\[ LMR = \Delta V_{out} \cdot \exp \left( -\frac{T/2 - t_d}{\tau_{latch}} \right). \quad (4.12) \]

Since the latch output (\( V_{out_{latch}} \)) and the slope of the latch at time = \( T-t_d \) are

\[
\begin{align*}
V_{out_{latch}} & = V_{initial} \cdot \exp \left( \frac{t}{\tau_{latch}} \right) \\
Slope_{latch} \bigg|_{t = T-t_d} & = \tau_{latch} \cdot V_{initial} \cdot \exp \left( \frac{(T-t_d)}{\tau_{latch}} \right)
\end{align*}
\quad (4.13)
\]

where \( V_{initial} \) is the initial value set for simulation of latch, the LMR becomes

\[
LMR = \delta \cdot \frac{\tau_{latch} \cdot V_{initial} \cdot \exp \left( \frac{(T-t_d)}{\tau_{latch}} \right)}{slope_{latch}} \cdot \exp \left( -\frac{T/2 - t_d}{\tau_{latch}} \right)
\quad (4.14)
\]

Therefore the latch input referred metastable region can be estimated. By indirect slope mapping between the master flip-flop and latch, time delay becomes an independent factor from metastable region calculation. As shown in eq.(4.14), time delay (\( t_d \)) cancels out to make LMR independent of \( t_d \). The only restriction in selecting \( t_d \) is to set the latch output less than 2.0 V, because the latch output develops exponentially when it is less than 2.0 V. The time constant of latch (\( \tau_{latch} \)) is designed to be 0.27ns.
The bit error rate (BER) can be calculated from the preamplifier gain, the latch input referred metastable region (LMR), and the 1 LSB of the quantizer as follows:

\[
BER = \frac{\text{LMR}}{(\text{Preamplifier Gain}) \times 1 \text{ LSB} / 2}
\]  

(4.15)

From eq. (4.15), the projected bit-error rate is lower than \(10^{-10}\) for the loaded time constants of this design.

4.3.3 Interpolated Quantizer

The input capacitance of the second and third quantizers are a large fraction of the total capacitive load on the respective residue amplifiers preceding them. As the second and third quantizers operate at only half of the full speed (50 MHz), an interpolation scheme has been used to reduce the input capacitance of the quantizer, while the input differential pair size remains constant so as not to increase the offset. The interpolation is performed by rewiring the second stage preamplifier as shown in Figure 4-18, which reduces the input capacitance by half with a simple modification from the first 4-bit AD-DA. As expected, the DNL of the interpolated comparators is less than that of the comparator without interpolation.

4.3.4 Reconstruction DAC

The reconstruction DAC consists of NOR gates, selection switches, and a
10-bit linear resistor ladder with 16 taps. NOR gates decode the 15 latch output in the thermometer code into a 1-of-16 selection from switches connected to a 10-bit linear resistor ladder, and the selected tap on the resistor ladder defines the reconstructed analog threshold.

One resistor ladder can be shared between the AD and the DA to provide references for the AD comparators, and also to provide a DA output as shown in Figure 4-19. The 4-bit AD-DA block can be implemented in two ways, either by placing the resistor ladder at the input or by placing it at the output. In the former case (Figure 4-19 (a)), each NOR output is routed back to select the corresponding tap from the resistor ladder which is used to provide references for the AD comparator.
Figure 4-19  Two possible layouts of AD-DA using single resistor ladder
comparators. The delay due to the wiring capacitance causes the gain-of-2 amplifier to momentarily develop its output in the wrong direction until the correct selection switch closes. After the correct switch is selected, the output starts to converge in the correct direction. Therefore, the wiring capacitance increases the amplifier settling time by 2 times the delay due to the wires. For the latter case (Figure 4-19 (b)) where the resistor ladder is placed at the output of the AD-DA block, the reference signals for the comparators are easily corrupted due to the coupling of the large digital signals traveling nearby, because the 1 LSB of the quantizer is 0.125 V while the digital output swing is 5 V.

With 2 separate resistor ladders, the signal flows unidirectionally from the quantizer, through the encoder, into the reconstruction DAC in Figure 4-10. A separate ladder for the DAC therefore eliminates the problems specified above.

The reference ladder for the DAC requires a total polysilicon resistance of 150 ohm, and is wider than that for the comparator to attain 10-bit accuracy in its tap voltages and settling time. As in the Elmore delay model for the RC ladder, which is

$$t_d = \sum_i R_i C_i$$  \hspace{1cm} (4.16)

where $R_i$ is the summed resistance from point to driving source and $C_i$ is the capacitance at the point $i$ (as shown in Figure 4-20), the first and second resistance is more important to shortening the settling time than the latter ones in first order estimation. The resistance of the reconstruction resistor ladder and the selection
switch have to be chosen so that the -3 dB bandwidth at the gain-of-2 residue input is wider than 200 MHz, where the required -3 dB bandwidth in the gain-of-2 amplifier during the amplifying phase is at least 100 MHz.

### 4.4 Residue Amplifier

The residue amplifiers must be designed to reduce interchannel offset and settling time, and to accurately align its full-scale output voltage with the reference of the subsequent quantizer within 1/2 LSB at 7-bit. Unlike the S/H, these amplifiers must be autozeroed to reduce their input offset and, therefore, the inter-channel offset. At a minimum capacitor size of about 0.25pF, the capacitor ratios are inherently accurate enough for 7-bit. The amplifier setting time is reduced by using pipeline and parallel architecture inside a gain-of-8 amplifier bank, as shown in Figure 4-1.

#### 4.4.1 Gain-of-2 Amplifier

Figure 4-21 illustrates a schematic of a gain-of-2 amplifier. During
sampling period($\phi_1$), the op-amp has its inverting input terminal shorted to its output voltage $V_{off}$ (offset voltage of op-amp) through M5(M6) and hence, the sampling capacitor $C_{s1}$ ($C_{s2}$) charges to $V_{in} - V_{off}$, while feedback capacitor $C_{f1}$ ($C_{f2}$) charges to $-V_{off}$. Since a large $g_m$ is required to overcome the small feedback factor during the amplifying phase, the output of the op-amp becomes underdamped in the presence of the output load during the resetting phase. A damping capacitor $C_{c1}$($C_{c2}$) is added at the output node. The resetting switch size(M5,M6) is carefully chosen to increase the phase margin. At the end of the sampling period($\phi_2$), M5(M6) should open first to cancel the voltage dependent
charge injection through M1(M3), and then open M1(M3), M9(M10). The opening of M5(M6) determines the sampling moment.

During the amplifying period(\(\phi_2\)), M1(M2) and M7(M8) are closed. The bottom plate of the sampling capacitor is connected to the DAC output and forms the residue. The residue is amplified by the ratio of Cs1 and Cf1.

### 4.4.2 Gain-of-4 amplifier

Figure 4-22 illustrates a schematic of a gain-of-4 amplifier. The gain of 4 amplifier works exactly the same as the gain-of-2 amplifier, except the feedback capacitor Cf1(Cf2) is connected to the input instead of to the bias during sampling.
period(\(\phi_1\)). The sampling capacitor \(C_{s1}(C_{s2})\) and feedback capacitor \(C_{f1}(C_{f2})\) are charged to \(V_{in} - V_{off}\) during sampling period(\(\phi_1\)). During amplifying period(\(\phi_2\)), the bottom plate of \(C_{s1}(C_{s2})\) is connected to bias voltage and the bottom plate of \(C_{f1}(C_{f2})\) is connected to output. Since the gain-of-4 amplifier does not need to form a residue, the ratio between a sampling capacitor and a feedback capacitor does not have to correspond to the gain of an amplifier. If a feedback capacitor is precharged to the input voltage, the ratio between the sampling capacitor and a feedback capacitor can be 1/3 instead of 1/4 in a gain-of-4 amplifier [42]. Therefore, the gain of 4 amplifier can have a same time constant as gain of 3 amplifier by increasing the feedback factor \((C_{fb}/(C_{fb}+C_{sm}))\) from 1/5 to 1/4.

### 4.5 Super cascode amplifier

The residue amplifiers must be designed to allow quantization of the residue to 7-bit accuracy. The op amps in these SC amplifiers must therefore have a large DC gain, and their output must settle to sufficient accuracy so that the amplified residue aligns with the full-scale of the subsequent quantizer. As shown in Figure 4-23, the fully differential super cascode amplifier architecture is used in all residue amplifiers in this ADC. In order to meet a requirement at a first residue amplifier bank, a dc gain of the opamp should be larger than 70 dB, because the accuracy of the closed loop gain of 8 should be better than 1\%. Since a dc gain of single cascode structure designed in 1.0 \(\mu\)m CMOS technology is less than 50 dB, a cascode
amplifier with an auxiliary amplifier attached to the cascode transistors (M3, M4, M5, and M6) is used to improve the DC gain without losing head room [5]. From the simulation, 76 dB DC gain is obtained. A switched capacitor common feedback is used, because it is linear under a wide dynamic range of differential output, and can have a different common mode output level between resetting and amplifying phase which maximizes the dynamic range of differential output [32].

4.5.1 Different common mode output level

The offset mismatch between 2 channels will appear as fs/2 and fs/4 tone in FFT and reduce SNDR. Therefore, an offset cancellation scheme is essential to
reduce a random offset mismatch. The offset should be sampled in the sampling node and feedback capacitors by applying unit gain feedback to the OP amp in resetting mode (autozero mode). Because of the unit gain feedback, the output of the op amp is shorted to the inputs, which means that the output is biased at in the input common-mode region. In amplify-mode, on the other hand, the maximum signal swing requires that the output be biased in the middle of the output common mode range. These two requirements are met at different common-mode points. Therefore, the reference in the common-mode feedback loop alternates the common mode level between 2.1V in autozero-mode and 2.7 V in amplify-mode, as shown in Figure 4-24. This common mode level alternation scheme is done by precharging two pairs of capacitors (Figure 4-25) [32]. During sampling phase, one
pair of capacitor are connected in a common mode feedback loop, while the other pair is precharged to the proper value used in amplifying the phase, and vice versa. The only requirement to this scheme is that the common-mode feedback loop must be almost as fast as the signal feedback loop around the op amp.

### 4.6 Error correction circuit and output buffer

#### 4.6.1 Error correction circuit

The error correction circuit (ECC) consists of 3 blocks as shown in Figure 4-26 (a). The 4-bit digital word coded in Gray code from each quantizer is converted to 4-bit binary code. The total 12-bit from three quantizer is fed into the
adder circuit. Because the threshold of the comparator has been shifted 1/4 LSB at 4-bit, only additions are required in this ECC. These additions do not require the full 4-bit to 4-bit adder. It is implemented into the circuit based on simplified

Figure 4-26  Error correction circuit (ECC) (a) Error correction circuit block diagram (b) Adder in ECC
version of the carry look ahead algorithm [102] because most of the inputs to the carry look ahead adder are zeros. The first three LSBs do not require any operation, the 4th, 5th, and 6th LSB are determined by the MSB from the binary decoded third quantizer output, and the remaining MSB (7th ~ 10th LSB) are determined by the results of a carry and MSB of the first addition output as shown in Figure 4-26 (b). The detail logic is illustrated in Figure 4-27. The 10-bit of the addition circuit output is feed into the OR gate so that the overflow can be represented as $2^{10} - 1$. 

\[
P = x \oplus y
\]
\[
g = xy
\]
\[
z_i = p_i \oplus c_i
\]
\[
c_{i+1} = g_i + p_i c_i
\]
\[
c_0 = 0
\]
\[
c_1 = 0
\]
\[
c_2 = 0
\]
\[
c_3 = 0
\]
\[
c_4 = x_3 x_4
\]
\[
c_5 = x_5 x_4 x_3
\]
\[
c_6 = x_6 x_5 x_4 x_3
\]
\[
c_7 = x_8 x_7 + [(x_8 \oplus x_7)c_6]
\]
\[
= x_8 x_7 + [(x_8 \oplus x_7)x_6 x_5 x_4 x_3]
\]
\[
c_8 = x_9 c_7
\]
\[
= x_9 x_7 + [(x_9 \oplus x_7)x_9 x_8 x_7 x_6 x_5 x_4 x_3]
\]
\[
c_9 = x_10 c_8 = x_10 x_9 c_7
\]
\[
= x_10 x_9 x_7 + [(x_10 \oplus x_7)x_10 x_9 x_8 x_7 x_6 x_5 x_4 x_3]
\]
\[
c_{out} = x_11 c_9 = x_11 x_10 x_9 c_7
\]
\[
= x_11 x_10 x_9 x_7 + [(x_11 \oplus x_7)x_11 x_10 x_9 x_8 x_7 x_6 x_5 x_4 x_3]
\]
4.6.2 Output buffer

The output levels of the output buffer are compatible to that of ECL logic where $V_{OH} > -0.8$ V and $V_{OL} < -1.70$ V. The differential output buffer is used to drive ECL logic levels into a remotely terminated logic analyzer, and does not produce large data-dependent current glitches on the chip power supplies. The schematic of the differential output buffer is shown in Figure 4-28.

4.7 Layout

The ADC was laid out by Led layout editor from Mentor Graphics. The layout extraction and DRC check were performed using Checkmate from Mentor
Graphics. The layout was checked using LVS from Tanner Research. The fully differential balanced signal is applied to the ADC from the bottom of the chip, and a single 100 MHz clock is applied from the top of the chip as the floor plan shown in Figure 4-29. The effect of the digital circuit noise [3][48][49][92] has been one of the major sources of degradation in performance in the ADC. To avoid the digital noise coupling, the analog signal is kept away from the digital area. All the noisy clock buffers which generate 50 MHz clock signals and 25 MHz clock signals, and
the output buffers, are located in the top part of the chip. The clock buffers are surrounded by p+ substrate contacts and the n-well guard ring, and the large p+ substrate contacts are added in-between the digital data output buffer and the core circuitry. To obtain the symmetry in the layout of 2-channel, the clock signals are distributed through the middle of the chip where the p+ substrate contacts and the n-well guard ring also surrounds them. The noise-sensitive analog circuits, such as the S/H and the gain-of-2 amplifier in the first residue amplifier bank, are laid out at the bottom of the chip and the digital and less noise sensitive circuits, such as the third quantizer, are laid at the top of the chip.

Since it is using a parallel architecture, symmetry between the layout of the two-channels was the next biggest concern. Except for the S/H and the first 4-bit AD-DA (which is common to both channels), all the other blocks are laid out as mirror images. For testability, there are the monitoring points at the outputs of the S/H, the first and second residue amplifier bank, and the reconstruction DAC, connected to the pad by transmission gates. For low-speed testing (< 5MHz sampling rate), the monitoring point can be turned on and the analog output can be observed. However, at the high clock conversion rate, since the capacitance loadings from pad, the offchip wiring, and the measuring instruments is more than 10pF, the transmission gate is turned off.

The S/H and the first 4-bit AD-DA have been laid out at the bottom of the other subconverter block. The capacitors of two gain-of-2 amplifiers are placed
close together to reduce an interchannel offset mismatch. The ADC is laid out in 10 x 10 mm², however, the core area of the chip is 50 mm², as show in Figure 4-30.

4.7.1 Gain-of-2 amplifier layout

Layout issues in the amplifier in the first residue amplifier bank are fast
settling time, settling accuracy, small offset, and decoupling of the digital noise from the residue signal to obtain better than 1 LSB of 10-bit accuracy. The amplifier has its own biasing circuit to make wiring complexity lower in the overall layout. The detailed layout is illustrated in Figure 4-31.

The S/H output signal and the reconstruction DAC output are applied to the
sampling switches and the amplifying switches (M3, M4 and M1,M2 in Figure 4-21) located left bottom. The S/H output signal is applied to the bottom plate of the linear capacitor. The top plate of the sampling capacitor is connected to the input differential pair of the amplifier. By this capacitor connection, the substrate noise is decoupled into the amplifier. The linear capacitor is made of poly and N+ diffusion, whose capacitance value is 1.3 fF/µm². The gain-of-2 amplifier in the first residue amplifier bank can only tolerate 0.5% gain inaccuracy because the first residue amplifier bank should have 7-bit gain accuracy. The sampling and feedback capacitors are laid out closely to each other to get better matching and the dummy capacitors are added at the top and bottom of the sampling and feedback capacitor bank to minimize the boundary effect and get better matching. In addition, this sampling and feedback capacitors are surrounded by the P+ and N- substrate contacts to reduce clock noise propagated through the surface of the substrate.

All the clock signal are located in the right bottom side of the corner to make a wide separation between the analog signals and the digital signals as the analog signals pass through the middle of the amplifier. The layout of the current source devices, the differential pair devices (M1, M2 and M7, M8 in Figure 4-23), and the reset switch (M5, M5 in Figure 4-21) use common centroid layout to minimize the offsets, so that it can also minimize the offset mismatch between the channels. In addition, the reset switches have been laid out so that the source and drain of the switch device face the same direction, to minimize the offset from threshold. Ions
are implanted in the silicon surface several degree off from right angle during P and N ion implantation. Therefore, the threshold is sensitive to the direction. The four auxiliary amplifiers for gain boosting are placed close to the cascode devices. The damping capacitor connecting to the output during reset phase is located at the right upper conner.

4.7.2 4-bit AD-DA

The 4-bit coarse quantizer and the reconstruction DAC can be separated as analog parts consisting of the first and second preamplifier, resistor ladders for comparator reference and the reconstruction DAC, the 15 DAC output selection switches, and the digital part consisting of the latch, master slave F/F and NOR gates, as shown in Figure 4-32. A common centroid layout is used in the first and the second preamplifier to minimize systematic offsets. One of the worst offset sources in the comparator might be the unbalanced coupling from the switches in the latch circuit. Because of the positive feedback during the regeneration phase in the latch circuit, the initial condition at the beginning of phase transition to regeneration determines the output. Therefore, the unbalanced charge injection at the phase transition will generate the systematic offset on top of the random offset. The measured mean and standard deviation of comparator threshold for the first prototype is shown in Figure 4-33. The means of the systematic comparator offset are about 18 mV which comes from the asymmetry layout. Since the complete cancellation of the charge injection due to switch clock is impossible, balanced
injection is the solution. Simply say that the preamplifier gain is large enough to
overcome this offset differential pair input in the preamplifier (See 4.3.1)

Figure 4-32  4-bit AD-DA layout
The 10-bit linearity of the first reconstruction DAC is essential to obtain 10-bit resolution in the pipeline ADC. The followings are the rules needed for our resistor ladder test chip to get 10-bit linearity, as shown in Figure 4-34. The first two taps at each end are discarded to eliminate edge effects and the width of 80 µm or larger poly-resistor ladder is used to decrease the nonlinearity. In addition, the poly-metal1 contacts to the DAC selection switch have to be kept out of the main resistor ladder so as not to interrupt the current flow. The variation of the contact resistance would not encounter any problems because there is no current flows through the SC.

Figure 4-33  Measured mean and standard deviation of comparator threshold offset from 1st quantizer in first version
amplifier when the DAC output settles.

4.8 Simulations

4.8.1 Input referred noise analysis

The input referred noise of ADC is simulated in Figure 4-35. The noise contributions from the wide-band S/H in both HoldI and HoldingII, gain-of-2 residue amplifier, are dominant than KT/C noise. The total noise referred to the input of ADC is about 280 µV (rms). This analysis was based on the second version and the schematic of the op amp (resize=1) is shown in Figure A-29.

4.8.2 Performance simulation

The circuit was verified with Hspice from the Meta-Software. The model used in the simulation was the MOS level 28 from HP. The SPICE netlists were generated by Powerview from Viewlogic. The input file for the simulation was prepared with extracted wiring capacitor at each block output. Digital data was
Sampling

60 $\mu$V (rms)

Hold I

165 $\mu$V (rms)

Hold II (non-reset)

150 $\mu$V (rms)

from gain of 2 RA

170 $\mu$V (rms)

from gain of 4 RA

44 $\mu$V (rms)

20_30 represents the switch NMOS 20$\mu$m, PMOS=30$\mu$m
resize1 represents op amp used in second stage RAs

Figure 4-35  Input referred Noise in ADC
obtain from the full-chip simulation for 32 points along a sinewave, which shows the -74 dBc noise floor.

The number of digital output from the simulation determine the extent of the observed spurious free dynamic range. Let’s assume $2^N$ number of digital data was obtained from the 1 period of sinusoid input. Since the SNR of the ideal 10-bit ADC is 62 dB, the magnitude of the noise floor $(x_n)$ is represented as

$$2^{N-1} \cdot x_n^2 = \frac{62}{10}$$  \hspace{1cm} (4.17)

Therefore

$$N = - \frac{10 \cdot \log_{10} x_n^2 + 62}{10 \cdot \log_{10} 2} + 1$$  \hspace{1cm} (4.18)

Since the Spurious Free Dynamic Range (SFDR) = $-10 \cdot \log_{10} x_n^2$,

$$N \approx - \frac{-SFDR + 62}{3} + 1$$  \hspace{1cm} (4.19)

and the number of point required in FFT is $2^N$. For example, to resolve the harmonic whose magnitude is 74 dBc, $N \approx - \frac{-74 + 62}{3} + 1 = 5$ from eq. (4.19). The minimum number of points required are $2^5=32$ as shown in Figure 4-36.
Figure 4-36  Noise floor in $2^N$ point FFT of ideal 10-bit ADC
Chapter 5

Testing Summary

Three prototypes of the ADC have been fabricated. In the first version, the measured resolution was only 8-bit with a low conversion rate. The poor resolution was traced to the 4-bit quantizer not having enough resolution (Figure 4-33). Furthermore, the slow conversion rate was due to excessive wiring capacitance at the output of most of the amplifiers. Finally, the effects of self-heating were not properly accounted for. In the second version, the resolution of the 4-bit quantizer was increased by first scaling the device sizes to reduce the random offset in the preamplifier. Second, the inputs to the differential pairs of the preamplifiers were re-arranged so that the preamplifier closest to the zero-crossing has the largest gain. The gain in the preamplifier suppresses the random offsets in the latch devices and the systematic offset due to asymmetric charge injection. In addition, the symmetric layout reduces the source of systematic offsets in the latch. To obtain the target
conversion speed, the extracted capacitance was used to estimate the loading capacitance instead of using an estimated capacitance. Also, the design was centered at 70°C instead of room temperature. The is the estimated junction temperature with an estimated power dissipation of 1.0 W and a package thermal resistance of 35°C/W. Finally, the preamplifier bandwidth was increased, and gain was reduced until the input referred random offsets of latch circuit were comparable to that of the preamplifier circuit.

In the second version, 10-bit resolution was achieved, and the maximum conversion rate is 50 MHz. The conversion rate was less than expected due to a seriously underestimated junction capacitance in the FET model. Most of the test results in this chapter are from the third version of the ADC with some results from the second version.

5.1 DC test using a monitoring pin

As mentioned in the layout, the monitoring pins are connected to the output of the S/H, reconstruction DACs, and the residue amplifiers through transmission gates. By turning on this monitoring transmission gate, the output of points can be measured using a high impedance probe and will provide very precise information at low conversion rates, typically less than 5MHz. Because the extra devices adds an unacceptable amount of capacitive loading to the output of the monitoring point, all the monitoring points are disconnected from these devices at high conversion
5.1.1 Resistor DAC test result

The linearity requirement at the first reconstruction DAC in pipeline ADC should be better than that of the ADC. The various shapes of the resistor DAC as shown in Figure 5-1 were fabricated to determine the shape of the resistor linearity. The 60-µm wide straight resistor ladder has the best linearity in four of the prototypes. In the ADC, the actual resistor linearity has been measured by turning on monitoring points. The input DC voltage is increased to read each threshold with DVM readout. Figure 5-2 illustrates the test setup for the reconstruction DAC linearity test. The resistor ladder used in this test is made of 120 µm X 1500 µm straight polysilicon. The worst resistor ladder INL measured from 17 chips is 0.6 LSB of 10-bits, which is linear enough to use as a reconstruction DAC in a 10-bit pipeline ADC, as shown in Figure 5-3. The 10-bit DAC with 0.3 INL using resistor ladder was reported by Brigati [4] and Pelgrom [70].
5.1.2 Comparator offset

The comparator offset has been measured using the same setup as used for measuring the reconstruction DAC output. The input voltage to the ADC is...
increased until the voltage of the reconstruction DAC is equal to the average of the two adjacent DAC levels. This voltage was measured with a DMV and is defined as $DACO_{\text{mean}}$.

$$DACO_{\text{mean}} = \frac{DAC_{n-1} + DAC_n}{2}$$  \hspace{1cm} (5.1)

where $n = -8, -7, \ldots, 6, \text{and } 7$

At this trigger point, the reconstruction DAC output is very sensitive to the input. The comparator offset is calculated from the input of ADC by eliminating the S/H amplifier’s effect. The x-axis in Figure 5-4 shows a comparator index which is numbered 0 at the middle where $V_{\text{ref}}^+ = V_{\text{ref}}^-$, is numbered positive where $V_{\text{ref}}^+ > V_{\text{ref}}^-$ and numbered negative where $V_{\text{ref}}^+ < V_{\text{ref}}^-$. The measurement summary\(^1\) from the 1st quantizer of the random input offsets of the 15 comparators illustrates a mean value of about 2.5 mV, with a standard

---

1. This measurement is performed on second version ADC
deviation of 9 mV for every comparator in the array under the ±0.75 V full scale reference voltage. At the third version of the ADC, the same circuit has been used for the comparator. The 6σ of each comparator offset in 4-bit quantizers satisfies requirements on an accuracy of ±1.0 V full scale. This means that the offsets within the quantizers in all the ADCs will be less than ±62.5 mV, which is ±0.5 LSB at 4-
bit of ± 1.0 V input full scale.

5.2 Testing Setup

The dynamic testing setup for A/D converter chips is illustrated in Figure 5-5. Two very low phase noise frequency synthesizers are locked to each other by a 10 MHz reference. One synthesizer is used to generate balanced fully differential analog inputs, and the other is used to generate a low jitter clock pulse. The first synthesizer output is connected to a low pass filter by a SMA cable and is low pass filtered by a 5th order Chebyshev filter\(^1\) to suppress 2nd and higher order harmonics.

---

1. The model numbers are LC5-(passband frequency)-50-613A from TTE, and passband frequencies are 100K, 200K, 500K, 1M, 2M,..., 50M, and 100 MHz.
to less than -80 dBc. The following 180° phase splitter can generate the fully differential outputs from the output of the low pass filter. These outputs directly drive the input pins of the ADC. The input matching is performed by 50 Ω termination resistor between input pad and the GND pad inside the chip. The 50 Ω termination resistor is made of polysilicon (25 Ω/□). The pads have no ESD protection. The common mode of the input differential signal is set to GND to provide the clean input signal. Therefore, the prototype ADC is biased with +2.2 V and -2.8 V instead of 5 and 0 V. The other synthesizer output is fed to a very low phase jitter pulse generator (Colby PG 1000A) to generate a short rise and fall time and a 50% duty cycle to drive a clock for the ADC. The synthesizer output is also fed to a general purpose clock pulse generator to add a proper delay between a clock input to the ADC and a digital logic analyzer, so that the digital logic analyzer\(^1\) can be strobbed to collect converted data. Furthermore, the Colby pulse generator can provide variable duty cycle. To decouple the digital noise from the analog signal and to make clean Vdd, Vss, and GND, an 8 layer PCB board has been used. In addition, the isolation transformer supplies clean power to the synthesizer for analog input to the power supply providing an analog Vdd and Vss, and programmable power supply for reference generation. The 20 digital outputs at 50 MHz from the ADC are not multiplexed, so the logic analyzer comfortably collects and stores the converted digital data into its memory. The stored data are down

\(^1\) HP 1663A logic analyzer: 2 channel, 4K/channel memory depth and 100 MHz state analysis capability
loaded using GPIB to a PC for post processing. GPIB is controlled by the PC program written in Visual Basic. Matlab in PC analyzed the data up to 1K, and Matlab in a SUN workstation analyzed the 4K data.

The detailed description of an 8 layer PCB board now follows. The analog input signal lines are drawn on the top of the first layer and the digital output lines are drawn at the bottom of the 1st and 8th layer to minimized the digital signal coupling into the analog input signal line. The types of each layer are summarized in Table 5.1. The components and the signal line layout is illustrated in Figure 5-6.

<table>
<thead>
<tr>
<th>Layer number</th>
<th>Signal type</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Signals</td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
</tr>
<tr>
<td>3</td>
<td>Analog VDD</td>
</tr>
<tr>
<td>4</td>
<td>Digital VDD</td>
</tr>
<tr>
<td>5</td>
<td>Analog VSS</td>
</tr>
<tr>
<td>6</td>
<td>Digital VSS</td>
</tr>
<tr>
<td>7</td>
<td>GND</td>
</tr>
<tr>
<td>8</td>
<td>Signals</td>
</tr>
</tbody>
</table>

The signal-to-distortion and noise ratio (SNDR), the total harmonic distortion (THD), and the spurious free dynamic range (SFDR) have been measured by performing the Fast Fourier Transform (FFT) on digitized waveforms generated from the ADC’s digital output [23]. In addition, the histogram test was used to obtain the integral nonlinearity (INL) and the differential nonlinearity (DNL) for
Figure 5-6 PCB board (a) component location (b) signal line layout
at top plate
the different input and sampling frequencies [13].

5.3 DC performance

5.3.1 Input referred interchannel offset

Figure 5-7 illustrates the histogram of the offset mismatch among the channels extracted from the digitized data, when a 421 KHz input is sampled at a 4 MHz clock. The data are generated from the each channel in sequence such as channel 1-a, channel 2-a, channel 1-b, channel 2-b, channel 1-a, channel 2-a,….

After data are downloaded, and statistics are calculated on the interleaved set of data.

The spreads of offset mismatches between channel 1a-2a and 1a-2b are larger than that between 1a-1b and 2a-2b. Because the offset mismatch from the gain-of-4 amplifier is decreased by gain of the gain-of-2 amplifier, the offset mismatch between the gain-of-2 amplifier is the dominant factor for the tone in the spectrum rather than gain-of-4 offsets.

Figure 5-8 illustrates histograms of the amplitude of $fs/2$ tone in (a) and the histogram of sum of combined $fs/2$ and $fs/4$ tone in (b). These $fs/2$ and $fs/4$ tones are extracted from the FFT spectrum with measured digitized data at the ± 0.5V input full scale. The measurement is performed on the first version ADC allowing only ± 0.5V input full scale due to the comparator architecture (Figure 4-13 (a)). With ±1.0 V input full scale, the $fs/2$ and $fs/4$ tones will be decreased by 6 dB. As
Figure 5-7  Histogram of measured input referred inter-channel offset mismatch
Figure 5-8  (a) Histogram of fs/2 tone
(b) histogram of RMS sum of fs/2 and fs/4 tone referred to ± 1 V, measured in ± 0.5 V input full scale
shown in Figure 5-7 and Figure 5-8, fs/2 is one of the major sources of lower the signal-to-distortion ratio (SDR), and this fs/2 will be suppressed later to -65 dBc by an offset cancelling circuit. The tones at fs/2 are consistent with measured offsets.

5.3.2 Reconstructed spectrum at low input frequency

The fine details of the output spectrum are best understood from digitizing a low input frequency (421 KHz) at a modest sampling rate (4 MHz) as shown in Figure 5-9. This reconstructed spectrum results from 4K point FFT. The 4K points
are the maximum memory depth of the logic analyzer we have. The SNDR of the
ADC at this frequency is 59.5 dB and the THD is -69 dB. As expected, the tone
appears at half the conversion rate (fs/2) due to offset mismatches between the two
residue amplifier channels following the input sample-and-hold (S/H), and the tone
at 1/4th of the conversion rate (fs/4) due to offset mismatches among the four
gain-of-4 amplifiers. In general, the fs/2 tone can be as large as 55 dBC from the
previous test result, but in this case the fs/2 tone is negligible. Harmonics of the
input signal are below -74 dBC.

5.4 Dynamic Performance

The SNDR measured while varying the conversion rate at low input
frequency (500 KHz) is illustrated in Figure 5-10 (a). The SNDR of 59.5 dB is
obtained at the 4 MHz conversion rate. This test result shows that the SNDR at the
low input frequency is above 9-effective bits up to a maximum conversion rate of
95MHz. The total harmonic distortion (THD) is calculated by power summation
from the second to the 20th harmonic. The THD and spurious free dynamic range
(SFDR) is illustrated in Figure 5-10 (b). Normally, the SFDR is determined by fs/2
tone. However, in this particular chip, the fs/2 tone and fs/4 tone are much lower
than -70 dBC, and the offset calibration designed to suppress fs/2 below -65 dBC was
not necessary. The largest distortion is the 3rd harmonic in this chip and the
magnitude of the 3rd harmonic is illustrated at SFDR plot in Figure 5-10 (b).
Figure 5-10 (a) Measured signal-to-distortion ratio (b) measured total harmonic distortion (THD) and spurious free dynamic range (SFDR) where input signal frequency is fixed 500 KHz.
The SNDR at 4 MHz, 50 MHz, and 95 MHz conversion rates with various input frequencies are plotted in Figure 5-11. The SNDR of a 95 MHz conversion rate is reduced by 3 dB below that of 4 MHz conversion rate at low input frequency. The SNDR at a 95 MHz sampling rate is better than effective 8-bits up to a Nyquist input frequency.

One method to test the performance of the sampling circuit is by subsampling. An input signal whose frequency is higher than a Nyquist is applied to the ADC while it is converting samples at low or moderate frequency. Because ADC is operated in a low sampling rate, all components settle completely, except

Figure 5-11  Measured signal-to-distortion and noise ratio at 4 MHz, 50 MHz and 95 MHz conversion rate
possibly the sampling circuit. Therefore, the distortions in converted data are a result from the sampling circuit. Timing jitter in the sampling point degrades the performance of ADC. The total distortion ($E_p$) [3] due to the jitter is represented as follows;

$$E_p = \frac{A^2 \omega^2 \sigma_t^2}{2}$$

(5.2)

where $A$ is amplitude of input signal and $\omega$ is input frequency, and $\sigma_t$ is a phase noise. In high frequency input signal, phase noise is one of the major source of distortion.

At a 4 MHz conversion rate, another measurement without the pulse generator for chip clock input (Figure 5-5) result in SNDR of 55.4 dB at 50MHz input frequency and 4 MHz sampling frequency which is more than 4 dB better than the one with a pulse generator for chip clock input. At a 4 MHz sampling rate with 50 MHz input frequency, all the components settle, except the sampling capacitor which might introduce a third harmonic due to ON resistance variation of the sampling switch. Therefore, after accounting for the harmonic distortion due to the sampling switch, we can extract the additive phase noise from the pulse generator by the SNDR difference of this two experiment. The SNDR plot of the 4 MHz conversion rate with the pulse generator can be reproduced by power sum of the following factors: the measured noise and distortion power at low input and low sampling frequency, the measured 3rd harmonic, and the 8 ps of phase noise at the
chip clock input. The projected SNDR without this phase noise is illustrated in Figure 5-12. The major improvement in SNDR is at high input frequencies, especially at 50MHz, because the noise power due to phase jitter increases with input frequency as shown in eq. (3.37).

The reconstructed spectrum from 4 K point FFT of 2 MHz input frequency at 95.2 MHz conversion rate is illustrated at Figure 5-12. All harmonics are still lower than -60 dBC, and the fs/2 tone due to the interchannel offset mismatch remains at a low level.

Plots of DNL and INL calculated from the histogram technique [13] at a 2 MHz input frequency and a 90 MHz conversion rate are shown in Figure 5-14 and
Figure 5-15. The DNL is between +0.6 LSB and -0.33 LSB and the INL is worse than 1 LSB in some codes higher than 900.

5.5 Power dissipation and test summary

Figure 5-16 illustrates the power dissipation vs. sampling frequency. The analog circuit dissipates 850 mW and the digital circuit dissipates 250 mW at 95 MHz. The average power dissipation of the chip at 95 MHz is about 1.1 W from the single 5 V power supply, excluding the power dissipation from the off chip logic driver. The breakdown of the power dissipation of each block is illustrated in the
pie-chart in Figure 5-17. The largest portion of power dissipation is the residue amplifiers. This is the price of converting 3-bits/stage over 1-bit/stage.

The tested A/D converter characteristics are summarized in Table 5.2.
Figure 5-15  Integral nonlinearity from 2 MHz input frequency at 90 MHz conversion rate
Figure 5-16  Power dissipation vs. sampling frequency

Figure 5-17  Power dissipation at 95 MHz sampling rate
Table 5.2 Summary of ADC characteristic

<table>
<thead>
<tr>
<th>Parameter</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>10 bit</td>
<td></td>
</tr>
<tr>
<td>Max Sampling Rate</td>
<td>95 MHz</td>
<td></td>
</tr>
<tr>
<td>Input Range</td>
<td>± 1.0 V</td>
<td></td>
</tr>
<tr>
<td>Signal/(Noise+Distortion)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>sampling freq</td>
<td></td>
<td></td>
</tr>
<tr>
<td>at f_{in} = 0.5 MHz</td>
<td>57.7 dB</td>
<td>56.5 dB</td>
</tr>
<tr>
<td>at f_{in} = 20 MHz</td>
<td>56.7 dB</td>
<td>54.3 dB</td>
</tr>
<tr>
<td>Thermal Noise</td>
<td>0.4 mV(rms)</td>
<td></td>
</tr>
<tr>
<td>fs/2 tone</td>
<td>&lt; 65 dBc^a</td>
<td></td>
</tr>
<tr>
<td>Power supply</td>
<td>+ 5V</td>
<td></td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>1.1 W</td>
<td></td>
</tr>
<tr>
<td>Active Area</td>
<td>50 mm^2</td>
<td></td>
</tr>
<tr>
<td>Technology</td>
<td>1.0 µm CMOS (N-Well) with linear Cap.</td>
<td></td>
</tr>
</tbody>
</table>

a. After on-chip offset cancellation
Chapter 6

Conclusions

6.1 Summary of research

The research successfully demonstrated the 1 µm CMOS 10-bit ADC with the maximum sampling rate of up to 95 MHz. It attains 59.5 dB SNDR at a low conversion rate, and more than 50 dB SNDR at a 50 MHz input frequency with 95 MHz conversion rate. By using a simple offset calibration, the fs/2 tone can be suppressed below -65 dBc. The simulated bit-error rate is less than $10^{-10}$. The ADC is implemented in fully differential circuits using a 2-channel 3-stage pipeline architecture. Each stage converts 4-bits, and 1-bit in the first and second stages is used for digital error correction. Because all the digital clock signals are generated from the on-chip clock buffer, the circuit requires only a single external full speed clock signal. The active chip area is 50 mm$^2$ and the ADC dissipates 1.2 W from a
single 5 V power supply.

Several architectural and circuits which enabled the ADC are described in this report. The techniques used to obtain the performance are listed below.

- Two channels pipelined ADC are utilized to increase the throughput from the single pipeline ADC.
- A single sample-and-hold amplifier operating at full speed provides held outputs to the ADC. Therefore, the nonuniform sampling of the analog input into the two channels is not an issue.
- Two channels share a single reconstruction resistor DAC, which meets stringent requirement of 10-bit accuracy and matching. Therefore, the gain mismatch due to IR drop in the metal line connecting to the ends of the resistor ladder is not an issue.
- The 4-bit/stage conversion (effective 3-bit/stage) relaxes the gain requirement of the residue amplifier and eliminates the effects of the gain mismatch between the channels.
- The residue signal is amplified by one gain-of-2 amplifier operating at half of the clock speed and the amplified residue signal is interleaved to the two gain-of-4 amplifiers at 1/4th of the full clock speed. This breakdown is based on equal gain-bandwidth products to increase throughput rate.
- A simple offset cancellation circuit is inserted at the last residue
amplifier.

- A single full speed external clock is required and all the clocks, i.e. complementary clock with delay for one 100 MHz, one 50 MHz, and two 25 MHz, are generated on chip for proper synchronization and testability.

A non-resetting sample-and-hold amplifier has been optimized so that it can operate at full speed. The rationale to design the non-resetting functions are:

- The conversion time at the front-end of the ADC is determined by the sum of the S/H delay, coarse quantizer delay, and delay of the latch. This delay has been reduced by utilizing a double-sampled pipeline scheme using two cascaded resetting S/Hs.

- The non-resetting S/H output provides a full clock period for the following residue amplifier to perform autozero.

The required linearity and settling speed in the reconstruction resistor ladder DAC are achieved by the following techniques:

- Dummy cells at both ends of the resistor ladder improve a resistor DAC linearity to more than 10-bit.

- Optimizing a selection switch size and a resistor ladder size can obtain the required time constant for DAC settling.

The 4-bit quantizer consists of a preamplifier, a latch, and a master slave F/F. It has been laid out for the signal to flow in one direction using two resistor ladders. The
comparator circuit has been selected and designed with the following criteria:

- The 2-stage preamplifier provides a wide dynamic range with proper gain to reduce an offset from the latch circuit and prevents a kickback from the latch to the input reference resistor ladder and reconstruction resistor DAC.

- The differential inputs and references have been arranged so that they can maximize the $g_m$ of differential pairs detecting the closest threshold to input.

- The feed forward latch architecture and boosting capacitors in the latch have been used to maximize the conversion speed.

- Since the second and third quantizers operate at half speed, the interpolation scheme (which is a simple elimination of half of the first preamplifier) was utilized to reduce input capacitance. And further reduction of input capacitance can be done at the second preamplifier if settling time allows.

### 6.2 Performance Analysis

There are some limiting factors that do not allow the prototype ADC to reach or exceed a 100 MHz conversion rate.

The first reason is that the S/H requires a longer settling time when the
capacitive loading from the extracted layout is taken into account, compared to earlier simulations with an estimated load. Therefore, at high conversion rate, the noise floor increases due to the first quantizer error. The conversion rate can be improved by re-optimizing the clock driver circuitry, or by re-sizing the hold non-resetting S/H.

Another performance limiting factor is residue amplifier gain errors. Another is the DC-type gain error at the low conversion rate where all the blocks in the ADC fully settle. When a single reference voltage is applied to the first, second and third reference ladders, and the metal line connecting the ladder end points off-chip been carefully sized to avoid any significant IR drops, only a 57 dB of SNDR is achieved. The external reference voltage must be tapered down by 1% per stage to obtain the best SNDR at a low sampling rate. It also must be tapered down by an additional 1% to compensate for the incomplete settling in the first residue amplifier bank at 95MHz conversion rate.

The active area may be reduced by more aggressively scaling down some of the later quantizers, or better yet, by using a more efficient implementation such as folding architecture [20][21][62][63][73] in the two channels following the full speed front-end. The folding architecture demonstrates 8-bit resolution up to 80 MHz conversion rate[63]. However, the primary goal of this work was to demonstrate the viability of an architecture, and therefore the high performance, but large, front-end blocks are re-used in the subsequent stages.
Appendix A

Comparators

A.1 Bipolar comparator

One common method of implementing the comparator latch is to make a dual connection of two transistors by cross connecting a base of one transistor to the collector of the other, as illustrated in Figure A-1. The first stage, consisting of \( Q_1 \), \( Q_2 \), and \( Q_5 \), amplifies the input signal to node \( V_{outp} \) and \( V_{outn} \) with a gain of \( g_{mQ1(Q2)} \times R_L \), when the latch signal goes high (amplifying period). When the latch signal goes low (regeneration period), the current flowing through \( Q_5 \) switches to \( Q_6 \), and this current is steered to \( Q_3 \) and \( Q_4 \) where positive feedback results in a latch function disabling the input signal from effecting the differential output voltage. An advantage of this current steering technique is that no additional bias current is necessary to implement the latch function. However, the input transistor
The comparator with “high-level” clocking (as shown in Figure A-2) can reduce a kickback substantially by cascoding the clock switches such as Q3, Q4, Q5, and Q6 [73]. Because the input differential pairs are on all the time, there is no instantaneous base charge current. In addition, the input capacitance is reduced because there is no miller capacitance due to the cascode of the clock switch. However, this comparator requires a greater number of transistors.
A.2 CMOS comparators

The comparators consist of a preamplifier and a latch stage. Several types of comparators have been reviewed and the schematic of comparators with static latches are illustrated in Figure A-3, A-4, A-5, A-6, and A-7, and the schematic of comparators with dynamic latches in Figure A-8, A-9, and A-10. In general, the dynamic latch has a larger amount of kickback than the static latch to preceding circuits such as preamplifier output and input to the comparator or the reference ladder in worse case. The dynamic latch, however, dissipates less power than the
static latch, even though the difference is negligible at high clock rates, because the dynamic latch does not dissipate any power during the resetting period.

The schematic of the comparator reported by Nauta is illustrated in Figure A-3. With a low latch signal, the comparator is in its pre-amplification period (reset period). The gain of the comparator at this period is determined by the transconductance of M1,2 and resistors R\textsubscript{L}. At the rising edge of the latch signal, the cross-coupled transistors M7 and M8 make a positive feedback latch. Since M7 and M8 are at the its threshold during pre-amplification period, the latch start to regenerate the output right after the latch signal goes high, compared with other latch whose output is reset to either Vdd or ground. The regeneration time constant is decided only by the transconductance of M7,8 and output capacitance. The major

Figure A-3   Comparator schematic from Nauta, 1996 [63]
advantages of the comparator are compactness (preamplifier & latch combined) and low kickback. M1 and M2 are always on, and kickback from output resetting is reduced by M3 and M4 by fixing the gate nodes to either low or high latch signal. However, the comparator cannot deliver standard CMOS logic levels and it requires the following full swing latch, which makes it improper to be used as a inter-stage sub-quantizer in a pipeline architecture due to timing. Another disadvantage is slow resetting time, compared to a latch with output reset to either Vdd or ground.

The schematic of the comparator reported by Fiedler is illustrated in Figure A-4. When the latch signal is high, M10 and M11 discharge the latch output nodes. When the latch signal goes low, the drain current difference between M8 and M9 appears as the output voltage difference. The cross-connected M12 and M13 form

![Comparator schematic from Fiedler, 1981](image)
a positive feedback and results in a latch. There are two disadvantages in this scheme. One is that there is some delay because M11 and M12 has to wait until either side of the output voltage becomes larger than Vt. The other is that there is a static current in the comparators which are close to the threshold after the output is fully developed. Assume the potential of Voutp node is higher than that of Voutn node. After the short period, M11 turns off and the potential of Voutp becomes Vdd, however, since M12 is in a linear region, the static current from M8 will drain during the regeneration period.

Figure A-5 illustrates the schematic of the comparator designed by Song. When the latch signal is high (resetting period), the diode-connected transistors M10 and M11 are fully turned on to reset the output. In addition, it works as a gain
amplifier with the gain approximately

$$A_{reset} = \frac{g_{m1,2}}{g_{m9,10} - g_{m10,11}}$$

(A.1)

where $g_m$ of M8 and M9 acts as the negative transconductance. However, this gain has to be optimized so that the latch output can be reset at the given clock rate. Once the latch signal goes low, the diode-connected transistors M10 and M11 are turned off and the amplifier becomes a positive feedback latch due to the cross-coupled transistors M8 and M9. The disadvantage of this comparator is that it dissipates power at the latch circuits where the input of the comparator is close to the threshold after the latch output is fully developed. The output of the latch seems to reach its full-scale output faster than that of the previous latch [16] because the cross-coupled transistors, M8 and M9, are in an active region at the moment when the latch signal goes off and starts the regeneration with initial amplified output voltage from the end of the resetting period.

Figure A-6 illustrates the schematic of the comparator designed by Lewis [42]. The circuit consists of a folded-cascode amplifier (M1-M7) where the load has been replaced by a current-triggered latch (M8-M10). When the latch signal is high (resetting period), M10 shorts both the latch outputs. In addition, the on-resistance, $R$, of M10 can give an extra gain ($A_{reset}$) at the latch output, approximately

$$A_{reset} = \frac{g_{m1,2} \cdot R}{2 - g_{m9,8} \cdot R}$$

(A.2)
which speed up the regeneration process. However, the on-resistance, $R$, should be chosen such that it can meet the following,

$$g_{m8} \cdot R < 2$$  \hspace{1cm} (A.3)

in all process corner and should be small enough to reset the output at the clock rate. Since all transistors are in active region, the latch can start regenerating right after the latch signal goes low. The one disadvantage of this scheme is the large kickback. Either node A or B has to jump up to Vdd in every clock cycle since the latch output does the full swing. Because of this, there are substantial amounts of kickback into the inputs through the gate-drain capacitor of M1 and M2 ($C_{gd1}$, $C_{gd2}$). To reduce kickback, the clamping diode has been inserted at the output nodes [62].
disadvantage is that the static power is dissipated after the regeneration is completed, similar to the previous CMOS comparator in Figure A-4 and A-5.

Figure A-7 illustrates the schematic of the comparator designed by Robert. When the latch signal is low (resetting period), the amplified input signal is stored at node A and B (gate of M8, M9) and M12 shorts both Voutp and Voutn. The extra gain can be obtained by sizing M12 as shown in eq. (A.2). When the latch signal goes high, the cross-coupled transistors M10 and M11 make a positive feedback latch. In addition, the positive feedback capacitors, C1 and C2, boost up the regeneration speed by switching M8 and M9 from an input dependant current source during resetting period to a cross-coupled latch during the regeneration period. Because of C1 and C2, the M8~ M11 work like a cross-coupled inverter so that the latch does
not dissipate the static power once it completes the regeneration period. However, there is a large amount of kickback through the positive feedback capacitors, C1 and C2. The switches (M6, M7, M13) have been added to isolate the preamplifier from the latch. Therefore, the relatively large chip area is required due to the positive feedback capacitors (C1, C2), isolation switches (M7, M8, M13), and complementary latch signals.

Figure A-8 illustrates the schematic of the comparator modified from the comparator designed by Yukawa. The NMOS and PMOS transistors have been swapped for the various performance comparisons. The dynamic latch consists of discharge transistors (M6, M7), a PMOS flip-flop (M8, M9) with PMOS transfer gates (M10, M11) for strobing, NMOS discharging transistors (M12, M13), and
NMOS flip-flop (M14, M15). When the latch signal is high (resetting period), the node A and B voltage go to Vdd and the output nodes are discharged to GND. Therefore, no static currents are flowing though these transistors (M6~M15). Once the latch signal goes high, the cross-coupled transistors M8, M9 and M14, M15 start regenerating the output. Because the node A and B have to discharge to Vdd-V\(_t\) to activate the M8 and M9 and the node V\(_{outp}\) and V\(_{outn}\) have charge up to V\(_t\) to activate the M14 and M15, there will be a small delay between the latch signal and the time that the four cross-coupled transistors start to develop the latch output. However, both transconductance (g\(_m\)) of NMOS and PMOS in the cross-coupled four transistors are added so that the regeneration time constant is fairly short. During the regeneration period, there is a static current in the latch where the input is close to the threshold, but there is no static current where the input difference is large so that one of the input differential pair is turned off.

Figure A-9 illustrates the schematic of the comparator designed by Sutarja. When the latch signal is low (resetting period), M6 and M7 turn off so that no static current flows through the latch and the bias voltage V\(_b\) and V\(_{b1}\) are set so that PMOS M4 and M5 are in the linear region. At the end of resetting period, the voltage of node D becomes V\(_t\) less than that of node A and B. Therefore, the NMOS M9 and M10 immediately go into the active region and start regenerating the latch outputs right after the latch signal goes high. The disadvantages of this scheme are that the latch dissipates a large amount of power after the latch output is fully
developed, and the fully developed latch outputs do not swing rail-to-rail so that the inverter buffers are required to obtain a rail-to-rail swing. In addition, since the output of the latch is connected to the drain of the input differential pair of the comparator, there is a large kickback.

Figure A-10 illustrates the schematic of the dynamic latch designed by Kobayashi. The dynamic latch consists of precharge transistors M12 and M13, cross-coupled inverter M6~M9, differential pair M10 and M11, and switch M14 which prevent the static current flow at the resetting period. When the latch signal is low (resetting period), the A and B node voltages are Vdd-V_t and the C node voltage is V_t below the latch input common mode voltage. Therefore, once the latch signal goes high, the NMOS transistors M7, M9, M10, and M11 immediately go
into the active region. Because each transistor in one of the cross-coupled inverters turns off, there is no static power dissipation from the latch once the latch outputs are fully developed.

The summary of the comparator schematics is tabulated in Table A.1 [38].
Table A.1 Summary of comparator performance

<table>
<thead>
<tr>
<th>Latch type</th>
<th>Speed</th>
<th>Kickback</th>
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<tbody>
<tr>
<td>Nauta</td>
<td>static</td>
<td>fair</td>
</tr>
<tr>
<td>Fiedler [16]</td>
<td>static</td>
<td>fair</td>
</tr>
<tr>
<td>Song [88]</td>
<td>static</td>
<td>good</td>
</tr>
<tr>
<td>Lewis [42]</td>
<td>static</td>
<td>fair</td>
</tr>
<tr>
<td>Yukawa (^b) [108]</td>
<td>dynamic</td>
<td>fair</td>
</tr>
<tr>
<td>Sutarja [94]</td>
<td>dynamic</td>
<td>fair</td>
</tr>
<tr>
<td>Robert [75]</td>
<td>static</td>
<td>excellent</td>
</tr>
<tr>
<td>Kobayashi [35]</td>
<td>dynamic</td>
<td>excellent</td>
</tr>
</tbody>
</table>

\(^a\) These results may not be fully optimized from the author’s design point.
\(^b\) The latch is modified.
# Appendix B

## Glossary

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
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<tr>
<td>ADC</td>
<td>Analog-to-digital converter</td>
</tr>
<tr>
<td>BER</td>
<td>Bit error rate</td>
</tr>
<tr>
<td>Bi-CMOS</td>
<td>Bipolar and CMOS combined (technology)</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complementary Metal Oxide Silicon (technology)</td>
</tr>
<tr>
<td>$C_{ox}$</td>
<td>Oxide capacitance</td>
</tr>
<tr>
<td>DAC</td>
<td>Digital-to-analog converter</td>
</tr>
<tr>
<td>DNL</td>
<td>Differential non-linearity</td>
</tr>
<tr>
<td>DUT</td>
<td>Device under test</td>
</tr>
<tr>
<td>FFT</td>
<td>Fast Fourier transform</td>
</tr>
<tr>
<td>ECL</td>
<td>Emitter-coupled logic</td>
</tr>
<tr>
<td>HDTV</td>
<td>High definition television</td>
</tr>
<tr>
<td>INL</td>
<td>Integral non-linearity</td>
</tr>
<tr>
<td>Abbreviation</td>
<td>Description</td>
</tr>
<tr>
<td>--------------</td>
<td>------------------------------------</td>
</tr>
<tr>
<td>MOS</td>
<td>Metal-oxide semiconductor</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal-oxide semiconductor field effect transistor</td>
</tr>
<tr>
<td>NTSC</td>
<td>National Television systems committee</td>
</tr>
<tr>
<td>RA</td>
<td>Residue amplifier</td>
</tr>
<tr>
<td>S/H</td>
<td>Sample-and-hold</td>
</tr>
<tr>
<td>SNR</td>
<td>Signal-to-noise ratio</td>
</tr>
<tr>
<td>SFDR</td>
<td>Spurious-free dynamic range</td>
</tr>
<tr>
<td>SNDR</td>
<td>Signal-to-noise-plus-distortion</td>
</tr>
<tr>
<td>THD</td>
<td>Total harmonic distortion</td>
</tr>
<tr>
<td>$V_t$</td>
<td>Threshold voltage</td>
</tr>
</tbody>
</table>
Appendix C

Distortion in RC sampling circuit

The passive sampling with MOSFET and driving capacitor is modeled as an RC network (Figure A-11). The differential equation for the RC network is:

\[ \frac{1}{1 + (\omega \tau)^2} \]

Figure A-11  Steady state response of RC network
represented as follows,

\[ RC \frac{d}{dt} V_o(t) + V_o(t) = V_i(t) \]  \hspace{1cm} (A.4)

If input signal \( V_i(t) \) is

\[ V_i(t) = \cos \omega t \]  \hspace{1cm} (A.5)

then

\[ V_o(t) = Ae^{-t/\tau} + \frac{\cos (\omega t - \phi)}{\sqrt{1 + (\omega \tau)^2}} \]  \hspace{1cm} (A.6)

where

\[
RC = \tau \\
\phi = \text{atan}(\omega \tau) \\
A = \text{initial value}
\]

Therefore, the steady state output, \( V_{os}(t) \), is represented as

\[ V_{os}(t) = \frac{\cos (\omega t - \phi)}{\sqrt{1 + (\omega \tau)^2}} \]  \hspace{1cm} (1.8)

which is pure sinewave.

Now, let find out the magnitude of error (\( \Delta V \)) between the sample-and-hold output, \( V_{SHo} \), and the steady state output as shown in Figure A-12. Because,

\[ V_{SHo}(t_0) = V_{os}\left(t_0 - \frac{T}{2}\right) + \varepsilon \]  \hspace{1cm} (A.9)

where \( \varepsilon \) is the error between S/H output and the steady state output (\( V_{os} \)) at the
sampling time, which is negligible to the amplitude of $V_{os}$ with reasonable $\tau$. The distortions added to the steady state output are dependent upon the difference between the sample-and-hold output, $V_{SHo}$, and the steady state output, $\Delta V$,

$$\Delta V\left(t_0 + \frac{T}{2}\right) = \left| \frac{\cos \omega \left( \left(t_0 - \frac{T}{2}\right) + \phi \right) - \cos (\omega t_0 - \phi) e^{-T/2\tau}}{\sqrt{1 + (\omega \tau)^2}} \right| e^{T/2\tau}$$

\[ \leq 2 \cdot \frac{e^{-T/2\tau}}{\sqrt{1 + (\omega \tau)^2}} \tag{A.10} \]
The relative error \((R_{error})\) 0.01% in each sampling is sufficient to obtain total distortion less than -62 dB, where

\[
R_{error} = \frac{\Delta V(t_0 + \frac{T}{2})}{\text{Amplitude of steady state output}} \leq 10^{-4}
\]

(A.11)

For 100 MHz sampling rate, \(T=10\text{ns}\), the required RC time constant \((\tau)\) is about 0.5ns, equivalent to \(f_{3db} = 300\text{ MHz}\).

In contrast to a typical single pole role-off response of a RC network, the modulation of the MOS resistance due to the sampling clock, causes the \(\sin x/x\) effect. This can intuitively be seen as follows. During the time\((\tau)\) when the gate of the MOS resistor start to turn off until the gate level reaches \(V_{cm}+V_t\), the frequency response is dependent on the input frequency. Since a RC network can be viewed as an integrator, we can integrate the input wave form up to the time\((\tau)\) in order to characterize the response in the frequency domain. The frequency over 50 MHz doesn’t need to be considered. The input sinusoid whose frequency corresponds to \(1/\tau\) is blocked, and thus appears as a null in the frequency domain. The resistance modulation doesn’t introduce distortion. Diode bridge track and hold does have distortion. [9]
Appendix D

Detail schematic of ADC

D.1 Schematic of top

1. Figure A-13 illustrates the non-resetting S/H and 4-bit ADDA.
2. Figure A-14 illustrates the block diagram of one of 2 channel

D.2 Schematic of non-resetting S/H

3. Figure A-15 illustrates the schematic of S/H
4. Figure A-16 illustrates the schematic of S/H op amp
5. Figure A-17 illustrates the schematic of auxiliary amplifier for PMOS cascade device
6. Figure A-18 illustrates the schematic of auxiliary amplifier for NMOS cascade device
7. Figure A-19 illustrates the schematic of CMFB of non-resetting S/H
Figure A-13  Non-resetting S/H and 4-bit ADDA
Figure A-14  Block diagram of one of 2 channel
Figure A-15  Schematic of non-resetting S/H
Figure A-16  Schematic of non-resetting S/H op amp
Figure A-17  Auxiliary amplifier for PMOS cascode device in non-resetting S/H
Figure A-18  Auxiliary amplifier for NMOS cascode device in non-resetting S/H
Figure A-19  Schematic of CMFB of non-resetting S/H
D.3 First ADDA

1. Figure A-20 illustrates the block diagram of first ADDA (100 MHz)
2. Figure A-21 illustrates the block diagram of comparator circuit in first 4-bit quantizer
3. Figure A-22 illustrates the schematic of pre-amplifier in first 4-bit quantize
4. Figure A-23 illustrates the schematic of latch in first 4-bit quantize

D.4 First residue amplifier

1. Figure A-24 illustrates the block diagram of first residue amplifier
2. Figure A-25 illustrates the schematic of gain-of-2 residue amplifier in first residue amplifier bank
3. Figure A-26 illustrates the schematic of gain-of-2 residue amplifier in first residue amplifier bank

D.5 Second residue amplifier

1. Figure A-27 illustrates schematic of gain-of-2 in second residue amplifier
2. Figure A-28 illustrates the schematic of gain-of-4 in second residue amplifier
3. Figure A-29 illustrates the schematic of gain-of-4 in second residue amplifier
Figure A-20  Block diagram of first ADDA (100 MHz)
Figure A-21  Block diagram of comparator circuit in first 4-bit quantizer
Figure A-22  Schematic of pre-amplifier in first 4-bit quantizer
Figure A-23  Schematic of latch in first 4-bit quantize
Figure A-24  Block diagram of first residue amplifier
Figure A-25  Schematic of gain-of-2 residue amplifier in first residue amplifier bank
Figure A-26  Schematic of gain-of-2 residue amplifier in first residue amplifier bank
Figure A-27  Schematic of gain-of-2 in second residue amplifier
Figure A-28  Schematic of gain-of-4 in second residue amplifier with simple offset control switch
Figure A-29  Schematic of op amp in second residue amplifier bank
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