Trend of Analog Circuits and Low-Voltage Design

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Many analog circuits in a cell phone

- Human interface
  - Display, microphone, speaker

- Transceiver
  - LNA, MIX, LPF, PA, etc.

- Mixed signal circuits
  - DAC, ADC

- Camera

- Sensor for authentication

Analog circuits are essential for human interfaces and communications.

What analog circuit technology will be needed?
Number of analog-related sessions in ISSCC

<table>
<thead>
<tr>
<th>Year</th>
<th>Number of analog-related sessions</th>
</tr>
</thead>
<tbody>
<tr>
<td>1985</td>
<td>7</td>
</tr>
<tr>
<td>1995</td>
<td>11</td>
</tr>
<tr>
<td>2005</td>
<td>19</td>
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</tbody>
</table>
Number of analog-related sessions in ISSCC

- Applications were mainly audio, video, and TV.
- Supply voltage was **5V**.
- Supply voltage of 2-3V was the challenge and discussed in the evening session.
- CMOS and bipolar were used.
Number of analog-related sessions in ISSCC

- Higher fT was available.
- Some wireless applications such as cellular phone, DECT, and PHS.
- RX, TX, even TRX were integrated in a single chip.
- Data converters were implemented by CMOS, and RF circuits in wireless applications by bipolar process.
- Supply voltage was 2.7 - 5V.
Number of analog-related sessions in ISSCC

- More wireless applications including WLAN, BT, UWB, and TV were reported.
- GHz-order circuits were no longer special. Even CMOS GHz-circuits appeared.
- Supply voltage is 2.7 - 3.3V in bip. process and 1.2 – 1.8V in CMOS process.
- CMOS process has been widely used.
- Wireless applications were the driving force.
High integration has been realized
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Filtering function has been integrated in a single chip.
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Filtering function has been integrated in a single chip.
Trend of supply voltage in cellular phone ICs

From ISSCC

Bipolar

RF+BB

CMOS

Only LNA+MIX

CDMA

GSM

Supply voltage [V]

Year
Trend of supply voltage in WLAN ICs

From ISSCC

0.18um CMOS

0.25um CMOS

90nm CMOS
For PA, Vdd=3.3V

For PA, Vdd=3.3V
Trend of supply voltage in GPS ICs

From ISSCC
Trend of process used in cellular and WLAN applications

From ISSCC
Trends of analog circuits in ISSCC

• System on a single chip
  - RF, BB analog circuits, A/D, and D/A have been integrated in digital baseband LSI.
  - Supply voltage has become very low.

• Process
  - Process has been shifted from bipolar to CMOS.

• Higher frequency applications
  - Signal frequencies have become higher, kHz - MHz in audio and video to GHz in wireless.

• Driving force
  - Driving force of analog circuit technology was wireless applications
Future wireless systems

**Coverage area**
- **Cellular**: 3G: W-CDMA, CDMA2000 1X, 3.5G, 3GPP-LTE
- **MAN**: FWA (IEEE 802.16a 16e)
- **LAN**: IEEE 802.11, 802.11b, 802.11a/g, 802.11n
- **PAN**: Bluetooth, UWB, ZigBee

**Data rate (bps)**
- **NOW**: 100k, 1M
- **2007**: 100M
- **2010 - 2015**: 1Gbps
- **4G (IMT-Advanced)**: 100Mbps - 1Gbps

**Technologies**
- **UWB**: Giga LAN
- **IEEE 802.20**: 100 Mbps - 1 Gbps
Future wireless systems

- Cell phones are replaced every 2 to 3 years.
- Driving force for analog circuits will still be wireless applications.
Future terminals

Software-defined radio (SDR)  Multi-band & Multi-mode terminal

LNA  ADC  DSP

Easy?  Power?

2 GSPS, 20 bit

WCDMA  BT
GSM  GPS
WLAN  UWB
TV(DVB-H)
2GSPS, 20bit A/D converter is estimated to dissipate 1kW.
RF signal cannot be easily A-to-D converted.
Frequency conversion is necessary. Direct conversion architecture is one of candidates.
Trend of supply voltage from ITRS

![Graph showing the trend of supply voltage from ITRS with years 2005 to 2020 and voltage levels for 65nm, 45nm, 32nm, and 22nm technologies. The graph illustrates the decreasing voltage trend over time.]

- Performance RF/Analog
- Precision analog/RF
Architecture of future terminals

Low-voltage implementation in BB analog circuits is key.

• This talk focuses on opamps used in filters, VGA, ADCs.
• After reviewing some low-voltage techniques for realizing SW function, CMFB will be discussed.
Review: discrete-time Integrator

S1 is critical at a low supply voltage.
Review: floating switch

CMOS Switch

High Vdd

Low Vdd

gds is small at a low supply voltage

Remove or avoid floating SW
SC integrators w/ switched opamp

Vdd=1V
SCF(BPF) fo=435kHz
CK=1.8MHz

Baschirotto, JSSC’97

Crols, JSSC’94
During off state, the output is reset to $V_A$.

Compared with switched-opamp, higher operating speed can be obtained since opamp is not turned off.
Switched-RC integrators

- Floating SW is replaced by resistor.
- Good linearity
- Limitation of sampling speed

Ahn, JSSC’05

Vdd=0.6V
DSM with
BW=24kHz
CK≈3MHz
Switch bootstrapping

(a) On state

(b) Off state

(c) Bootstrapping circuit

Fayomi, ISCAS'01, Dessouky, JSSC'01, Draxelmayr, ISSCC'04, Fayomi, ISCAS'05, Ishii, CICC'05
Analog T-switch

Vdd=0.5V
Delta sigma w/ BW=8kHz
CK=2MHz

Ishida
2005 VLSI Sympo
Balanced structure -1-

Single-ended structure cannot deal with a large voltage swing.

Balanced structure can deal with a larger voltage swing.
Balanced structure -2-

Common-mode signal does not appear in differential-mode. At plus and minus outputs, CM signal appears! This CM signal may make DM signal distorted. CM signal should be suppressed by CMFB and/or CMFF.
Conventional CMFB

CMFB loop contains two amplifiers.

- CMFB makes CM gain low by reducing CM load impedance, not CM gm.
- To suppress CM signal, large loop gain is required, but this often causes instability.
Two SE amps for reduction of CM components

CM is cancelled.  \( \text{DM is added.} \quad \Rightarrow \quad \text{CM } \text{gm} \approx 0 \) 
Large loop gain is unnecessary for CMFB.

- Reduction of CM components by using two SE amps is useful.
CMFB - 1 -

Move comparator into individual amplifiers.

Czarnul, CICC’97
Each amplifier is not necessarily a differential-difference amp. Two differential-input amplifiers are sufficient.
CMFB - 3 -

Frequency responses of fully balanced and single-ended opamps
Design issues in wideband applications -1-

SE opamp introduces another pole at current mirror.

Avoid FB configuration using diff.-to-SE circuit.
Design issues in wideband applications -2-

For wideband applications, high transition frequency is required.

\[ f_T = \frac{g_m}{C_{GS}} \]

\[
\frac{W}{L} \mu C_{OX}(V_{GS} - V_{th}) = \frac{2}{3} WLC_{OX}
\]

\[
= \frac{3}{2} \frac{\mu C_{OX}(V_{GS} - V_{th})}{L^2}
\]

For achieving high transition frequency, \( V_{GS} \) should be large. This makes CM input range narrower.
Differential Pair

Preceding Stage

2-stage Amplifier

Vcm > 0.55V > Vdd/2 (Vth=0.25V, Vsat=0.15V)
Extra power dissipation is required
Strategy for new low-voltage opamp

1. No differential pair as input circuit

2. Remove lines connected to plus inputs for avoiding differential to single-ended circuit

3. Replace CM voltage detector with new one without resistors
Proposed opamp

\[ V_1 = \frac{1}{2} V_{in} + V_{cm} \]

\[ V_2 = -\frac{1}{2} V_{in} + V_{cm} \]

\[ I_A = \frac{1}{2} G_m V_{in} \]

\[ I_B = -\frac{1}{2} G_m V_{in} \]

Common-mode rejection without using differential pairs

Ueno, ISSCC’04
Large gain cannot be easily obtained in a single-stage amplifier.
2-stage opamp

Large DC gain
Input stage for adding 2 inputs
Improvement by no diff.-to-SE circuit

Current mirror as diff.-to-SE circuit degrades phase margin.
Differential Integrator

V_3 \approx V_{cm} - \frac{1}{2sCR} V_{in}

V_4 \approx V_{cm} + \frac{1}{2sCR} V_{in}

Differential mode:
Integrator

Common mode:
Unity gain Buffer
Mitigating CM component

CM output voltage is mitigated by AmpC
All input voltage is virtual GND to Vref
Design example 1: $\Delta \Sigma$ modulator for WCDMA

- Bandwidth: 1.92MHz
- Accuracy: > 8bit (SNDR of 49.9dB)
- Supply Voltage: 0.9V

Floating switch is removed
Low-voltage opamps for integrators/DACs are essential
Modulator Architecture

- 2nd order, Multi bit
- OSR=16 (61.44MHz Ck)
- NRZ-RZ converter to avoid code-dependent distortion
Measured Spectrum

Amplitude [dB]

Frequency [Hz]

57.1 dB
### Measured results

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>0.9 V</td>
</tr>
<tr>
<td>Clock frequency</td>
<td>61.44 MHz</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>1.92 MHz</td>
</tr>
<tr>
<td>Peak SNR</td>
<td>53.2 dB (8.54 bit)</td>
</tr>
<tr>
<td>Peak SNDR</td>
<td>50.9 dB (8.16 bit)</td>
</tr>
<tr>
<td>Power consumption</td>
<td>1.5 mW</td>
</tr>
<tr>
<td>Core area</td>
<td>750 μm x 160 μm (0.12 mm²)</td>
</tr>
<tr>
<td>Technology</td>
<td>0.13 μm CMOS</td>
</tr>
</tbody>
</table>
Design example 2: biquad filter

Cutoff frequency: 2MHz
**Measured intermodulation**

- **IIP3** = 23.8 dBm
- **57.9 dBc@700mVpp (differential)**
# Measured results

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</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>0.9V</td>
</tr>
<tr>
<td>IIP3 (Pass band)</td>
<td>23.8dBm</td>
</tr>
<tr>
<td>CMRR</td>
<td>49.3dB</td>
</tr>
<tr>
<td>Input referred noise</td>
<td>-18.5dB $\mu$V/$\sqrt{\text{Hz}}$</td>
</tr>
<tr>
<td>Power consumption</td>
<td>1.89mW</td>
</tr>
<tr>
<td>Pass band gain</td>
<td>-0.05dB</td>
</tr>
<tr>
<td>Cutoff frequency</td>
<td>2MHz</td>
</tr>
</tbody>
</table>
Passive elements and area

\[
\frac{S}{N} = \frac{V^2}{(kT/C)}
\]

When signal amplitude is halved, 
4 times larger capacitance is required 
to keep the same SNR.

For low cost, process and supply voltage are carefully chosen.
Passive elements and area

Thermal Noise: \( \frac{kT}{C} \)

\[ \frac{S}{N} = \frac{V^2}{(kT/C)} \]

When signal amplitude is halved, 4 times larger capacitance is required to keep the same SNR.

For low cost, process and supply voltage are carefully chosen.
Conclusions

1. From ISSCCs, trends of analog circuits were mentioned.
   - Over the past 20 years, supply voltage has decreased from 5V to 1.2 -1.8V.

2. Wireless applications will still be the driving force.
   - In future terminals, frequency conversion will be necessary.

3. ITRS roadmap indicates necessity of low supply voltage.

4. Low-voltage techniques were reviewed.

5. CMFB suitable for low-voltage opamps was discussed.
   - For wideband applications, avoid diff.-to-S.E. circuit.

6. Larger capacitance is needed in low-voltage circuits.
   Impact on chip area was discussed.
Thank you!