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UMI
Design and Analysis of a 3.3V, Unity-Gain, CMOS Buffer Amplifier

by

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A thesis submitted to the Department of Electrical and Computer Engineering in conformity with the requirements for the degree of Master of Science (Engineering)

Queen’s University
Kingston, Ontario, Canada
February, 1999

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0-612-42617-3
Abstract

This thesis reports the design and analysis of a unity-gain buffer amplifier for use in video applications. First, the performance of other reported buffer amplifiers is examined, and the results are combined with the requirements of the video applications to set the performance goals for the design. The design utilizes a 3.3V, 0.35µm minimum gate length process in order to achieve increased speed while minimizing power consumption.

The advantages and disadvantages of different circuit topologies are briefly discussed, leading to a description of the topology applied to the design. The circuit design is described and analyzed using first order models to predict the behavior. Computer simulations are then used to determine the necessary transistor dimensions and predict the circuit performance with more accuracy. The results of the first order analysis are evaluated in comparison to the simulation results.

The fabricated design meets the required specifications, achieving a 122MHz bandwidth while driving a 50Ω, 15pF load with a 1V p-p output swing and a THD of −32.8 dB. Quiescent current is only 2.10mA and a 5% settling time of 29.8 ns is achieved for a 1V input step. Shortcomings in the performance are discussed, and the performance of the amplifier is evaluated in comparison to previously reported designs. This leads to suggestions for future design work.
Acknowledgments

I would like to thank my two supervisors, Dr. A.P. Freundorfer and Dr. D.G. Nairn for their assistance and guidance throughout this project. I acknowledge the financial support of Micronet, NSERC, and PMC-Sierra which made this work possible. I would also like to thank the Canadian Microelectronics Corporation and PMC-Sierra for their access to fabrication facilities and their support for the design tools, and Nortel for their use of testing facilities. I thank my family, friends and fellow students for their support, especially Brian Frank and Jay Lee, who were always around for advice and conversation. Finally, I would like to thank Jessica Haney for being a constant source of inspiration and happiness in my life.
## Contents

Abstract ........................................................................................................................................ i

Acknowledgments ......................................................................................................................... ii

List of Figures ................................................................................................................................ v

List of Tables ................................................................................................................................... viii

List of Symbols and Acronyms ........................................................................................................... x

Chapter 1 - Introduction .................................................................................................................... 1

  1.1 Reported Performance .............................................................................................................. 1

  1.2 Areas of current work ............................................................................................................... 5

  1.3 Conclusions ............................................................................................................................. 6

  1.4 Thesis Goals ............................................................................................................................ 6

References .......................................................................................................................................... 8

Chapter 2 - Design Theory ................................................................................................................ 11

  2.1 Output Stages .......................................................................................................................... 11

  2.2 Error Amplifiers ....................................................................................................................... 15

  2.3 Circuit Analysis ......................................................................................................................... 20

  2.4 Compensation ......................................................................................................................... 26

  2.5 Biasing .................................................................................................................................... 29

References .......................................................................................................................................... 33

Chapter 3 - Process and Simulation .................................................................................................. 34

  3.1 The n-well Process .................................................................................................................... 34

  3.2 Simulations of Output Transistors and Error Amplifiers ......................................................... 37

  3.3 Simulation of Output Stage ...................................................................................................... 40
3.4 Adding Biasing and Compensation ......................................................... 45
3.5 Evaluating Circuit Analysis ...................................................................... 47
3.6 Unity Gain Configuration ...................................................................... 48
3.7 Design Layout ...................................................................................... 55

References ............................................................................................... 60

Chapter 4 - Results and Analysis ............................................................. 61
4.1 Experimental Set-Up ............................................................................ 62
4.2 Frequency Response ............................................................................ 64
4.3 Transfer Characteristic ........................................................................ 64
4.4 THD Analysis ....................................................................................... 65
4.5 Transient Response ............................................................................. 67
4.6 Quiescent Current and Offset Voltage .................................................. 69
4.7 Results Summary ................................................................................ 69

Chapter 5 - Discussion and Conclusions .................................................. 70
5.1 Performance Relative to Other Buffers ............................................... 70
5.2 Results vs. Simulation .......................................................................... 71
5.3 Conclusions ......................................................................................... 73
5.4 Future Work ......................................................................................... 74

Appendix A - Glossary of Terms ............................................................... 76

Vita ............................................................................................................. 77
List of Figures

Figure 1.1  Normalized Power vs. $f_t$ ................................................................. 4
Figure 1.2  Normalized Power vs. Output Voltage Squared ................................. 5
Figure 2.1(a) The Complimentary Source Follower .............................................. 11
Figure 2.1(b) Practical Implementation of the Source Follower ............................... 12
Figure 2.2(a) The Common Source Configuration .................................................. 13
Figure 2.2(b) Practical Implementation of the Common Source Configuration .......... 13
Figure 2.3  A Common Source Output Stage Using Negative Feedback .................. 15
Figure 2.4  The Standard Two-Stage Op. Amp ....................................................... 16
Figure 2.5  A Modified Two-Stage Op. Amp .......................................................... 18
Figure 2.6  Error Amplifier with Quiescent Current Control .................................... 19
Figure 2.7  Circuit Diagram of the Output Stage ..................................................... 21
Figure 2.8  High Frequency MOSFET Model with Source and Substrate Connected 21
Figure 2.9  Op. Amp Equivalent Circuit Using High Frequency Models ................. 23
Figure 2.10 Reduced Equivalent Circuit ............................................................... 23
Figure 2.11 Equivalent Circuit Incorporating Output Transistor ............................. 25
Figure 2.12 Error Amplifier with Compensation Capacitor ...................................... 26
Figure 2.13 Error Amplifier with Lead Compensation ............................................. 27
Figure 2.14 The Fully Compensated Output Stage .................................................. 29
Figure 2.15 A Bias Circuit Independent of Temperature and Process Variations ........ 30
Figure 2.16 The Complete Output Stage ............................................................... 32
Figure 3.1  Wafer with Photoresist Mask and Oxide Layer ...................................... 35
Figure 3.2  Wafer with Resulting n Well ............................................................... 35
Figure 3.3(a) Wafer with Thin Oxide, Field Oxide, and Polysilicon Gate

Figure 3.3(b) Wafer Following Implants in Source and Drain Regions

Figure 3.3(c) Finished Inverter with Metal Contacts

Figure 3.4 $V_{OUT}$ vs. $V_{IN}$ for Output Transistors Driven by Ideal Op. Amps

Figure 3.5 Frequency Response of Op. Amp Driving NMOS Output Transistor

Figure 3.6 $V_{OUT}$ vs. $V_{IN}$ for Output Stage with Real Error Amplifiers

Figure 3.7 Total Current Draw When Error Amplifiers Fail

Figure 3.8 $V_{IN} - V_{OUT}$ for Differing Sizes of M5 and M6

Figure 3.9 Open-Loop Frequency Response of the Output Stage

Figure 3.10 Open-Loop Magnitude and Phase Responses of Complete Output Stage

Figure 3.11 Unity Gain Frequency Response of Complete Output Stage

Figure 3.12 Unity Gain Frequency Response with Revised Compensation

Figure 3.13 Transient Response of the Output Stage

Figure 3.14 Frequency Response of Circuit With Revised Device Geometries

Figure 3.15 Improved Transient Response of the Output Stage

Figure 3.16 (a) NMOS Transistor Layout (b) PMOS Transistor Layout

Figure 3.17 Circuit Layout

Figure 4.1 Microphotograph of the Fabricated Circuit

Figure 4.2 Chip Package Attached to Circuit Board

Figure 4.3(a) Test Setup for Frequency Response

Figure 4.3(b) Setup for Transfer Characteristic, THD, and Transient Response

Figure 4.4 Measured Frequency Response

Figure 4.5 Transfer Characteristic: $V_{OUT}$ vs. $V_{IN}$
Figure 4.6  Transfer Characteristic with Lower Crossover Distortion .................. 65
Figure 4.7(a) Amp1 Output for 5MHz, 1V p-p Sine Wave Input .......................... 66
Figure 4.7(b) Amp2 Output for 5MHz, 1V p-p Sine Wave Input .......................... 66
Figure 4.8(a) Amp1 Transient Response ............................................................ 68
Figure 4.8(b) Amp2 Transient Response ............................................................ 68
Figure 5.1  Relative $P_{NORM}$ vs. $f_c$ Performance of this Buffer .................... 70
Figure 5.2  Relative $P_{NORM}$ vs. $V_{OUT}^2$ Performance of this Buffer ............ 71
Figure 5.3  Simulated Crossover Distortion ....................................................... 72
Figure 5.4  Simulated Compensation Problems .................................................. 73
List of Tables

Table 1.1  Output Stage Performance Goals.................................................................7
Table 3.1   Device Geometries of Output Transistors..................................................37
Table 3.2   Device Geometries for Op. Amp Driving NMOS Output Transistor..............39
Table 3.3   Device Geometries For Op. Amp Driving PMOS Output Transistor..............40
Table 3.4   Device Geometries of Quiescent Current Control Transistors .................41
Table 3.5   New Device Geometries of Transistors M5 and M6 .................................44
Table 3.6   Device Geometries for Bias Network.........................................................46
Table 3.7   Capacitance Values for Compensation Capacitors ....................................47
Table 3.8   Device Geometries of Compensation Transistors ....................................47
Table 3.9   Poles Predicted by Chapter 2 Circuit Analysis ..........................................48
Table 3.10  Poles Predicted After Addition of $C_C$.....................................................48
Table 3.11  New Capacitance Values for Compensation Capacitors .............................51
Table 3.12  New Device Geometries of Compensation Transistors ..............................51
Table 3.13  Performance Specifications of the Output Stage .......................................52
Table 3.14  Revised Device Geometries to Reduce Circuit Size ...................................53
Table 3.15  Performance Specifications of Improved Output Stage ..............................55
Table 3.16  Performance Specifications from Extracted Layout .................................58
Table 3.17  Summary of All Transistor Dimensions .....................................................59
Table 4.1   Voltage Sources Used..................................................................................62
Table 4.2   THD Levels for Varying Levels of Crossover Distortion ...............................67
Table 4.3   Amp1 and Amp2 Settting Times .................................................................67
Table 4.4   Quiescent Current and Offset Voltage for Amp1 and Amp2 .......................69
**List of Symbols and Acronyms**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMOS</td>
<td>complimentary metal-oxide semiconductor</td>
</tr>
<tr>
<td>$f_t$</td>
<td>unity-gain frequency</td>
</tr>
<tr>
<td>$f_{3dB}$</td>
<td>3dB (half-power) frequency</td>
</tr>
<tr>
<td>$R$</td>
<td>resistance</td>
</tr>
<tr>
<td>$C$</td>
<td>capacitance</td>
</tr>
<tr>
<td>$A_0$</td>
<td>dc gain</td>
</tr>
<tr>
<td>$P$</td>
<td>power</td>
</tr>
<tr>
<td>$V$</td>
<td>voltage</td>
</tr>
<tr>
<td>THD</td>
<td>total harmonic distortion</td>
</tr>
<tr>
<td>$V_{p-p}$</td>
<td>volts peak-to-peak</td>
</tr>
<tr>
<td>MOSFET</td>
<td>metal-oxide semiconductor field effect transistor</td>
</tr>
<tr>
<td>$I$</td>
<td>dc current</td>
</tr>
<tr>
<td>$K$</td>
<td>MOSFET gain constant</td>
</tr>
<tr>
<td>$V_{gs}$</td>
<td>MOSFET gate-to-source voltage</td>
</tr>
<tr>
<td>$V_t$</td>
<td>MOSFET threshold voltage</td>
</tr>
<tr>
<td>$g_m$</td>
<td>MOSFET small-signal transconductance</td>
</tr>
<tr>
<td>$r_o$</td>
<td>MOSFET output resistance</td>
</tr>
<tr>
<td>$V_A$</td>
<td>Early voltage</td>
</tr>
<tr>
<td>$L_{eff}$</td>
<td>effective transistor channel length</td>
</tr>
<tr>
<td>$X_d$</td>
<td>MOSFET depletion layer</td>
</tr>
<tr>
<td>$V_{DS}$</td>
<td>MOSFET dc drain-to-source voltage</td>
</tr>
<tr>
<td>$V_{GS}$</td>
<td>MOSFET dc gate-to-source voltage</td>
</tr>
<tr>
<td>$C_{gs}$</td>
<td>MOSFET gate-to-source capacitance</td>
</tr>
<tr>
<td>$C_{db}$</td>
<td>MOSFET drain-to-bulk (substrate) capacitance</td>
</tr>
<tr>
<td>$C_{gd}$</td>
<td>MOSFET gate-to-drain capacitance</td>
</tr>
<tr>
<td>$W$</td>
<td>transistor channel width</td>
</tr>
<tr>
<td>$L$</td>
<td>transistor channel length</td>
</tr>
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<td>Symbol</td>
<td>Definition</td>
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<td>--------</td>
<td>----------------------------------</td>
</tr>
<tr>
<td>$L_{ds}$</td>
<td>gate-source overlap</td>
</tr>
<tr>
<td>$L_{dd}$</td>
<td>gate-drain overlap</td>
</tr>
<tr>
<td>$C_{ox}$</td>
<td>gate oxide capacitance</td>
</tr>
<tr>
<td>NMOS</td>
<td>N-channel MOS</td>
</tr>
<tr>
<td>PMOS</td>
<td>P-channel MOS</td>
</tr>
<tr>
<td>$f_p$</td>
<td>pole location (Hz)</td>
</tr>
<tr>
<td>$\omega_p$</td>
<td>pole location (radians)</td>
</tr>
<tr>
<td>$\mu$</td>
<td>carrier mobility</td>
</tr>
<tr>
<td>SiO$_2$</td>
<td>silicon dioxide</td>
</tr>
<tr>
<td>SiN</td>
<td>silicon nitride</td>
</tr>
<tr>
<td>VLSI</td>
<td>very large scale integration</td>
</tr>
<tr>
<td>PSF</td>
<td>pseudo source-follower</td>
</tr>
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</table>
Chapter 1 - Introduction

Buffer amplifiers are essential components in many electronic systems. They function to increase the power of analog signals and allow them to be sent down low impedance transmission lines and across large loads. This allows communication between different system components in countless applications, including computing, radio, and video. As they are essential to the operation of systems, the performance of buffer amplifiers can limit the performance of the overall system, and thus buffer design is important. This performance can be limited in areas such as bandwidth, power draw, and the load driving capabilities and output swing. The power draw of a buffer is an important factor in design, as the buffer often consumes a large amount of the total power in a circuit. This leads to efforts to minimize power consumption, and makes class AB amplifiers a popular choice for their combination of low distortion and high efficiency. CMOS is an attractive technology as it offers the advantage of lower power consumption.

This chapter shows the results of a survey of recently reported buffer amplifier performances. These results reveal both limits in performance, and trends, in buffer design. A study of the results indicates areas of interest in amplifier design, and areas in which there is a potential for improved performance. From this, a set of goals for the design presented in this thesis are formulated.

1.1 Reported Performance

There are three basic parameters for evaluating amplifier performance. The first of these is the unity gain frequency \( f_u \), a measure of the range of signal frequencies (bandwidth) over which the amplifier can operate. This range can limit the possible applications
of the amplifier or, conversely, the unity gain frequency required may be specified by the intended application. The cost of higher $f_t$ is increased power consumption (i.e. faster operation requires more power). In the case of a unity gain buffer configuration, $f_t$ obviously loses any meaning. In this case, $f_{3dB}$, the half-power bandwidth can be used instead.

The second parameter is the open-loop dc gain ($A_0$), the amount by which the circuit can amplify the signal. This also indicates the accuracy with which the circuit will perform, since the higher the amplifier gain, the closer its performance is to the ideal op. amp presented in texts [1]. As a simple example of this one can consider an inverting amplifier configuration. The gain of this circuit is known to be

$$\frac{V_o}{V_i} = \frac{-R_2/R_1}{1 + \frac{R_2/R_1}{A_0}}$$

Eqn. (1.1)

where $R_1$ is the resistor between $V_i$ and the inverting input, and $R_2$ is the resistor between the inverting input and $V_o$. As the gain increases, the denominator approaches 1, and the gain of the circuit approaches $-R_2/R_1$, which is the ideal case. The third parameter is the power consumption of the circuit ($P$). The goal in amplifier design is to minimize $P$, while maximizing the other two performance parameters.

Surveying reported buffer performance fails to reveal any significant trends in $A_0$ vs. the year the amplifier was reported, $A_0$ vs. $f_t$, or $A_0$ vs. $P$ [2]-[16]. This indicates that designers are achieving the gains that they need, and this is not a driving research area. This survey will therefore focus on the $f_t$ and $P$ of the reported buffers.

Amplifier design is not an isolated process, rather amplifiers are designed with specific applications in mind. Because these applications vary and place greatly varying
demands on the amplifier's performance, it is hard to make a direct comparison between two different buffers. In particular, certain applications require a much larger load driving capability than others, so the buffer will consume more power. This loading can be taken into account by normalizing the power consumption by the size of the load. This allows a fairer comparison between the different buffers.

The normalized power with respect to 50Ω is given by

\[ P_{NORM} = P \times \frac{R_L}{50\Omega} = \frac{V_{SUPPLY}}{R_L} \times \frac{R_L}{50\Omega} \]  

Eqn. (1.2)

Those amplifiers driving lower resistance loads are “rewarded” as they require more power to do so. The power has been normalized to a 50Ω load, as this is a standard value used in telecommunications, and therefore covers most applications.

Figure 1.1 shows the normalized power for resistive loads, in mW, vs. the unity gain frequency, in MHz [2], [3], [5]-[10], [12]-[18]. Both axes are on a log scale. Output voltages vary, as shown in figure 1.2, and the amplifiers are assumed to have sine-wave outputs. A definite performance frontier can be seen for the CMOS amplifiers, consisting of the points 1-4 in the lower right side of the plot [3], [5], [10], [16]. The slope of a line drawn through these four points is 1.7. This indicates that a decade increase in \(f_t\) requires a 1.7 decade increase in power, which is far from the ideal case of a decade increase in power per decade increase in \(f_t\). Since these amplifiers are buffers, and thus driving heavy loads, this effect is not caused by the relatively small loading caused by parasitic capacitances, but by the larger load capacitance, which has not been taken into account because it is often not specified for buffers. As parasitics are not a major problem here, there is room for improvement in buffer performance. These four points do not appear in any chro-
nological order, which indicates that rather than trying to better previously reported amplifiers in

![Figure 1.1 Normalized Power vs. $f_i$](image)

performance, the designers had specific applications in mind. As a figure to give the frontier some numerical values, it can be observed that to drive a 50Ω load at a unity gain bandwidth of 10 MHz requires 30mW of power. This power consumption should drop significantly with the use of shorter channel length technologies, which achieve high speeds while operating at lower supply voltages.

Another plot of interest when considering resistive loads is the normalized power in mW vs. output voltage swing squared (since $P_{out} \propto V_o^2$), shown in figure 1.2 [2], [3], [5]-[7], [9], [10], [12], [14], [16]-[18]. Again both axes use a log scale. Here the six points on or close to the technology frontier, points 1-6, all use a common-source output stage, with five of the six using one of two output stages reported by John Fisher in the mid
1980's [2], [3], [10], [14], [17], [18]. These common source output stages therefore appear attractive for achieving a high output swing while minimizing power consumption.

![Figure 1.2 Normalized Power vs. Output Voltage Squared](image)

**1.2 Areas of current work**

The number of low voltage designs has increased in recent years [12], [15]. With the use of shorter channel length technologies, supply voltages must decrease to maintain E-field scaling. Low voltage designs are also attractive as they offer lower power consumption, which is important in small portable devices such as hearing aids [12]. As it is essential to make use of the full voltage swing when using low supply voltages, numerous designs have appeared incorporating input and output stages of buffers with rail-to-rail voltage swings. The common source configuration appears to be the most popular choice for buffer output stages driving low impedance loads [9], [10], [15], [16], [18]. Input stages employ parallel p and n-type differential input pairs, with many designs also
attempting to achieve constant transconductance in these input stages, as a constant transconductance in the input stage allows for more efficient frequency compensation [10], [16]. The most popular method controls the transconductance by varying the tail currents which bias the input pairs. This is achieved by a current switching circuit employing 3:1 current mirrors, and variations as low as 3.3% have been achieved [16]. However, one drawback of this technique is that it relies on the devices operating as square-law devices, and therefore may not be applicable to more linear, short-channel devices. There has also been some interest in higher bandwidth CMOS designs. These designs have specific applications in video, where the higher bandwidth is a necessity [16].

1.3 Conclusions

In conclusion, it is evident that buffer amplifiers are an area of continuing research. The number of reported buffer amplifiers shows that there is still an interest in improving amplifier performance. It is evident from the varying buffer loads, and the fact that designs on the $P_{NORM}$ vs. $f_T$ performance frontier appear in no chronological order, that the best performance designs are application driven. With increased use of shorter channel technologies, the limits of buffer amplifier performance will be pushed to meet the needs of specific applications, while overcoming the constraints imposed by lower supply voltages.

1.4 Thesis Goals

Following advances in technology, the buffer amplifier presented in this thesis will be designed using a 3.3V, 0.35μm process. This short channel length should allow a much higher $f_T$ while the lower voltage supply maintains the same moderate power consumption
levels as the circuits in this survey. Since it is apparent that the best performance is achieved in designs driven by a specific application, the amplifier will be designed to meet the specifications of high quality video, which requires a bandwidth of 75MHz. This output stage will drive a $50\Omega$, 15pF cable in a unity-gain configuration. To allow for the affects of temperature and process variations on performance, it will be designed to achieve a 3dB bandwidth of 100MHz. Given the limits imposed by the 3.3V supply, a 1V p-p output swing will be required. For video applications, the THD is required to be lower than -30dB. The complete set of goals for the performance of this output stage are summarized in table 1.1.

**Table 1.1 Output Stage Performance Goals**

<table>
<thead>
<tr>
<th>output swing</th>
<th>1V p-p</th>
</tr>
</thead>
<tbody>
<tr>
<td>quiescent current</td>
<td>&lt; 5mA</td>
</tr>
<tr>
<td>3dB bandwidth</td>
<td>100MHz</td>
</tr>
<tr>
<td>THD (1V p-p, 5MHz sine wave)</td>
<td>&lt; -30dB</td>
</tr>
<tr>
<td>load ($R_L, C_L$)</td>
<td>$50\Omega$, 15pF</td>
</tr>
</tbody>
</table>
References


Chapter 2 - Design Theory

The main goal in the design of an output stage is a circuit with a large current gain that can provide the current necessary to drive a large resistive or capacitive load. Since the purpose of the circuit is to provide sufficient current, a large voltage gain is not required. In addition to providing sufficient output power, an output stage must also avoid distortion of the input signal, and must therefore have a large signal swing and a very linear voltage transfer characteristic. It must be efficient, so quiescent power dissipation is a concern. Finally, it must provide protection from short circuits, high temperatures, and other unusual conditions. Since MOS devices are inherently self-limiting, this last condition is usually met. All these requirements must be met while considering the slew-rate limitations imposed by the large resistive and capacitive loads [1].

2.1 Output Stages

One possible output stage is the complimentary source follower, which is a CMOS implementation of the classical bipolar Class AB topology [2]. The basic principle of the circuit is shown in figure 2.1(a), and figure 2.1(b) shows a practical implementation of this.

![Figure 2.1(a) The Complimentary Source Follower](image)
design, where the two diode connected transistors, M4 and M5, provide the required voltage drop. This circuit meets many of the requirements listed above, but has a very limited output swing. Swing is limited because in order to provide a large current, the output transistors must have a large $V_{gs}$, since the current in a saturation-mode MOSFET is given by:

$$I = K(V_{gs} - V_t)^2$$  \hspace{1cm} \text{Eqn. (2.1)}

The $V_{gs}$ of M1 is limited by the positive supply rail, while the $V_{gs}$ of M2 is limited by the negative supply rail, so the available current, and therefore the available swing, is limited. For example, for an NMOS transistor in the CMOS35 process with an aspect ratio of 400 to drive a 50Ω resistance up to 1.75V would require a $V_{gs}$ of approximately 1.9V. This would require a total supply voltage of 3.65V, but the maximum supply in this process is only 3.3V. Due to its limited swing, the source follower is not a suitable configuration.

Other output stage configurations must therefore be investigated.

A greater output swing can be achieved by using a common source configuration.
This configuration allows typical swings of within 500mV of the supply rails [3]. Figures 2.2(a) and 2.2(b) show the principle of operation, and practical implementation of an inverting class AB common source output stage. Here, the output transistors do not suffer the limited $V_{gs}$ which causes problems in the source follower configuration, and can swing almost to the supply rails. In this case, swing is limited by the condition which must be met in order for a transistor to remain in saturation:

![Diagram](image-url)
\[ V_{ds} > V_{gs} - V_t \]  
Eqn. (2.2)

Thus the output can swing to within \( V_{gs} - V_t \) of the rails. The operation of the circuit in figure 2.2(b) can be class AB or class B depending on the bias voltages \( V_{G3} \) and \( V_{G4} \). When a positive voltage is applied at the input, \( V_{IN} \), the current in transistor M1 increases, while the current in M2 decreases. Transistors M7 and M8 form a current mirror, so the increased current in transistor M4 is mirrored to the output transistor M8. Similarly, the drop in current in transistor M3 is mirrored to output transistor M6. Thus, the current in M8 increases while the current in M6 decreases, causing the output voltage to fall. Conversely, a negative input increases the current in M2 and decreases the current in M1, increasing the current in M6 and decreasing the current in M8, causing the output voltage to rise [1].

Since a large voltage gain is not required, negative feedback can be applied in a unity-gain configuration to improve the linearity of the voltage transfer characteristic. Figure 2.3 shows a configuration which combines the benefits of negative feedback with the large output swing of the common source output stage [2]. Here the error amplifiers, E1 and E2, sense the difference between the input and output voltages, and drive the output transistors to decrease this difference. If the output is less than the input, a small increase in the input causes a large negative voltage to appear at the output of both amplifiers, causing a large increase in the \( V_{gs} \) of MP and a large decrease in the \( V_{gs} \) of MN. MP will then supply more current, and MN less current, until the output reaches the same level as the input. To avoid crossover distortion, the error amplifiers must have a high gain broadband frequency response which, coupled with the large capacitive load of the circuit, can cause problems in frequency compensation. Design of the error amplifiers must therefore
allow for a practical compensation scheme, while allowing a large signal swing and maintaining a reasonable quiescent current level [2].

2.2 Error Amplifiers

An operational amplifier (op. amp) must be designed to meet the requirements of the negative feedback output stage. The amplifier must have a sufficient voltage gain to provide the desired linearity, must be easily compensated, and must also have an offset at the output to avoid crossover distortion. For the output stage to provide the required signal swing, the op amp must have both a large common-mode input range, and a large output swing. In particular, the output of the error amplifier driving the PMOS output device should swing all the way to the negative supply rail, to allow that device to provide as much current as possible. The common mode input range should go all the way to the positive rail, to allow as large an input range as possible [4]. Similarly, the output of the error amplifier driving the NMOS output device should swing to the positive rail, and the input
common mode range should extend to the negative rail. To achieve this, the designs of the two error amplifiers can be complimentary, i.e. where one amplifier uses a PMOS device, the other will use an NMOS device, and vice-versa. With this approach in mind, the design of only one of the amplifiers need be considered, then this design can easily be adapted to the second amplifier. The following sections will therefore consider the design of the amplifier driving the NMOS output transistor.

The standard error amplifier is the basic two-stage CMOS op. amp shown in figure 2.4 [3]. The first stage consists of a differential pair driving an active load. The second stage uses a common source configuration to provide additional gain. This amplifier has a high voltage gain, a good common mode input range, and a large output swing. In addition, it can be compensated using only a single capacitor. The gain of the first stage of the amplifier is given by:

\[ A_1 = g_m l \left( r_{o2} / r_{o4} \right) \]  

Eqn. (2.3)

The gain of the second stage is given by:
\[ A_2 = g_m b_6 (r_{o6}/r_{o7}) \]

The total gain of the circuit is the product of the two gains:

\[ A = g_m b_6 (r_{o1}/r_{o4}) (r_{o6}/r_{o7}) \]

which indicates that:

\[ A \propto (g_m r_o)^2 \]

The expression \( g_m r_o \) can be expanded:

\[ g_m r_o = \frac{2 I}{V_{GS} - V_t} (\frac{V_A}{I}) = \frac{2 L_{eff}}{V_{GS} - V_t} \left[ \frac{dX_d}{dV_{DS}} \right]^{-1} \]

where \( X_d \) is the MOSFET depletion layer width. It is apparent from Eqn. 2.7 that the gain of the amplifier is dependent on the channel length of the devices used, and on the bias point of the transistors. However, it should be noted that adjusting either the bias current or the channel lengths to increase gain will affect the frequency response of the amplifier, decreasing the available bandwidth [2].

The input stage can be analyzed to determine whether the common mode range extends to the negative rail as desired. The input pair \( M_1 \) and \( M_2 \) will leave the saturation mode when the common mode input falls below the drain voltage. The drain of \( M_1 \) will be set by the \( V_{gs} \) of transistor \( M_3 \), so the negative limit of the common mode range will be:

\[ V_{cm/min} = V_{SS} + V_{GS3} - V_t \]

which is within \( V_{GS3} - V_t \) of the negative rail.

Analysis of the second stage determines whether the available output swing extends to the positive supply rail. Since the positive limit of the output range is determined by transistor \( M_7 \) leaving the saturation region, it will be given by:

\[ V_{o/max} = V_{DD} - V_{GS7} + V_t \]

17
which is within \( V_{GS7} - V_t \) of the positive rail. \( V_{GS7} \) is set by the bias voltage applied to the gate of M7 and is therefore easily controlled, so it is possible for the output to swing very close to the rail.

An adaptation of the basic two-stage op. amp is shown in figure 2.5. The changes made from the standard amplifier make the circuit more suitable to the output stage design, while retaining the desirable features of good input common mode range, large output swing, and simple compensation [5]. The circuit still features the input differential pair, and the common source transistors in the second stage, and therefore has the same common mode range and output swing as the standard amplifier. However, now only

![Figure 2.5 A Modified Two-Stage Op. Amp](image)

transistor M2 has an active load, and this load is connected to the common source transistor M4 to form a current mirror. This configuration provides an improved frequency response, as the loading on the input transistors is significantly reduced. By setting the widths of M4 and M3 at a ratio of 2:1, the second stage contributes a current gain of 2, while providing the output swing and output resistance of a common source output stage.
The small signal current through M3 is now:

\[ i = g_m \frac{v_i}{2} \quad \text{Eqn. (2.10)} \]

The output voltage of the amplifier is given by:

\[ v_o = 2i \left( r_{o4} / r_{o6} \right) \quad \text{Eqn. (2.11)} \]

Which gives the amplifier a gain of:

\[ A = g_m (r_{o4} / r_{o6}) \quad \text{Eqn. (2.12)} \]

The gain of the amplifier is now considerably lower, but is sufficient to provide the desired linearity. The circuit maintains the two-stage configuration which allows for frequency compensation using only a single capacitor.

As shown in figure 2.6, transistor M7 can be added to control the output voltage of the error amplifier. By causing an offset voltage at the error amplifier output, M7 biases the transistor that the amplifier drives in a manner that ensures class AB operation, eliminating crossover distortion. M7 thus controls the quiescent current of the transistor.

![Figure 2.6 Error Amplifier with Quiescent Current Control](image-url)
being driven. $V_{OUT}$ of the amplifier can be adjusted by varying the width of M7, which varies the voltage that will appear across the transistor for a given drain current.

2.3 Circuit Analysis

If the error amplifier shown in figure 2.6 is used to drive the NMOS output device, and a complimentary amplifier is used to drive the PMOS device, then the output stage will appear as shown in figure 2.7. Corresponding to figure 2.3, transistors M1-M7 form the error amplifier which drives the NMOS output transistor, MN. Similarly, transistors M8-M14 form the error amplifier which drives MP, the PMOS output transistor. The positive inputs of the two amplifiers are both connected to the output node of the circuit, while the negative inputs are both connected to the input node of the overall circuit. A detailed analysis of this circuit is now required to determine the frequency compensation necessary to ensure stable operation. Again, due to the symmetry of the circuit, only the amplifier driving the NMOS output transistor, and that output transistor, need be considered in the analysis.

In order to analyze the circuit, a high frequency equivalent circuit model of the MOSFET must be used. This circuit models the capacitances which appear in the device when operating at high frequencies, and replacing the transistors in a circuit with these models allows an analysis of the circuit to determine the behavior at high frequencies. The high frequency model of a saturation-mode MOSFET with the source connected to the substrate is shown in figure 2.8 [5]. The capacitance between the gate and the source, $C_{gs}$, consists of three components. The dominant component is the gate to channel capacitance, which in saturation mode appears between the gate and the source, with a value of
Figure 2.7 Circuit Diagram of the Output Stage

Figure 2.8 High Frequency MOSFET Model with Source and Substrate Connected
$\frac{2}{3} WLC_{OX}$. The second component is the parasitic capacitance between the gate and the substrate of the transistor. The third is the overlap capacitance, which occurs because the gate slightly overlaps the source region. The overlap capacitance has a value of $WL_{ds}C_{OX}$, where $L_{ds}$ is the length of the overlap. Capacitance $C_{gd}$ occurs due to the overlap of the gate and the drain region, and is equal to $WL_{dd}C_{OX}$, where $L_{dd}$ is the length of this overlap. Capacitance $C_{db}$, the capacitance between the drain and the substrate, is due to the charge storage which occurs in the depletion region in the substrate, under the active region of the transistor [5].

Substituting the transistors for their equivalent circuit models, the op. amp circuit of figure 2.6 can be analyzed. The resulting transfer function will reveal the location of the poles and zeros of the amplifier. In order to simplify analysis, both the input transistors M1 and M2, and the quiescent current control transistor M7 are modeled as having their source and substrate connected. The validity of this simplification will be evaluated in a comparison between the results of the circuit analysis, and those of sophisticated computer simulations in chapter 3. The equivalent circuit from the input to the output node is shown in figure 2.9. The connection between the gate and drain of M3 allows further simplification. Since the gate of M7 is grounded, that equivalent circuit is also simplified. The entire circuit can be reduced to the circuit shown in figure 2.10. Here it is assumed that the input stage is faster than the second stage, so the input can be modeled as a current source, $i_{in}$. Since the voltage $v_{gs3}$ appears across the dependent current source $g_{m}v_{gs3}$, the current source is equivalent to a resistor of value $1/g_{m3}$. The values of the circuit elements are:
Figure 2.9 Op. Amp Equivalent Circuit Using High Frequency Models

Figure 2.10 Reduced Equivalent Circuit

\[ R_1 = \frac{1}{g_{m3} R_{o2} R_{o3}} = \frac{1}{g_{m3}} \quad \text{Eqn. (2.13)} \]

\[ C_1 = C_{db2} + C_{gs3} + C_{gs4} + C_{db3} \quad \text{Eqn. (2.14)} \]

\[ C_f = C_{gd4} \quad \text{Eqn. (2.15)} \]

\[ g_m = g_{m4} \quad \text{Eqn. (2.16)} \]

\[ R_2 = \frac{r_{o4}}{r_{o7}} \quad \text{Eqn. (2.17)} \]

\[ C_2 = C_{db4} + C_{db7} + C_{gd7} \quad \text{Eqn. (2.18)} \]
Analysis of this circuit yields the transfer function:

\[
\frac{v_o}{i_{in}} = \frac{(sC_f - g_m)R_1 R_2}{1 + s[C_1 R_1 + C_2 R_2 + C_f (g_m R_1 R_2 + R_1 + R_2)] + s^2 [C_1 C_2 + C_f (C_1 + C_2)] R_1 R_2}
\]

Eqn. (2.19)

The zero of this transfer function is given by:

\[
\omega_z = \frac{g_m}{C_f}
\]

Eqn. (2.20)

This is at a frequency much higher than that of the dominant pole, but as it is in the right half plane, it can cause problems in stability. This problem will be addressed further when frequency compensation is considered. The denominator of the transfer function can be expressed in the form

\[
D(s) = \left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right) = 1 + s\left(\frac{1}{\omega_{p1}} + \frac{1}{\omega_{p2}}\right) + \frac{s^2}{\omega_{p1}\omega_{p2}}
\]

Eqn. (2.21)

and in the case where pole \(\omega_{p1}\) is dominant,

\[
D(s) \approx 1 + \frac{s}{\omega_{p1}} + \frac{s^2}{\omega_{p1}\omega_{p2}}
\]

Eqn. (2.22)

Thus \(\omega_{p1}\) can be determined from the coefficients of \(s\) in the denominator, giving:

\[
\omega_{p1} \approx \frac{1}{C_1 R_1 + C_2 R_2 + C_f (g_m R_1 R_2 + R_1 + R_2)}
\]

Eqn. (2.23)

Similarly, \(\omega_{p2}\) can be found from the coefficients of \(s^2\) in the denominator and the value of \(\omega_{p1}\) given in Eqn. 2.23, which results in:

\[
\omega_{p2} = \frac{C_1 R_1 + C_2 R_2 + C_f (g_m R_1 R_2 + R_1 + R_2)}{[C_1 C_2 + C_f (C_1 + C_2)] R_1 R_2}
\]

Eqn. (2.24)
Analysis can be furthered by also considering the output transistor that the error amplifier will drive. Just as it was assumed that the input stage was faster than the second stage of the error amplifier, here it will be assumed that the error amplifier is faster than the output transistor, so the input is modeled as a current source. A second equivalent circuit can thus be utilized to find a second transfer function, which will reveal the location of the poles and zeros at the output. This equivalent circuit, shown in figure 2.11, is of the same form as the equivalent circuit of figure 2.10. Here, simplifications taking advantage of the differences in magnitude of resistances and capacitances have been made:

\[
C_3 = C_{db4} + C_{db7} + C_{gd7} + C_{gsn}
\]

Eqn. (2.25)

\[
r_{o4} // R_L = R_L
\]

Eqn. (2.26)

\[
C_{dbn} + C_L = C_L
\]

Eqn. (2.27)

Resistance \( R_2 \) is as given in Eqn. 2.17. Analysis can be carried out on this circuit as was done on the circuit of figure 2.10. Using the same steps in the analysis, the pole locations for this second circuit are found to be:

\[
\omega_{p1,\,OUTPUT} = \frac{1}{C_3R_2 + C_LR_L + C_{gdn}(g_{mn}R_2R_L + R_2 + R_L)}
\]

Eqn. (2.28)

\[
\omega_{p2,\,OUTPUT} = \frac{C_3R_2 + C_LR_L + C_{gdn}(g_{mn}R_2R_L + R_2 + R_L)}{[C_3C_L + C_{gdn}(C_3 + C_L)]R_2R_L}
\]

Eqn. (2.29)
2.4 Compensation

In order for the closed-loop feedback circuit to achieve stability, the open-loop frequency response of the circuit must have a phase margin of at least 60° [6]. To achieve this, a compensation capacitor, \( C_C \), can be placed between the gate and the drain of transistor M4 as shown in figure 2.12, increasing the effective \( C_f \) of the circuit. As can be seen from Eqn.2.23 and Eqn. 2.24, for a large \( C_f \), the approximations for \( \omega_{p1} \) and \( \omega_{p2} \) reduce to:

\[
\omega_{p1} \approx \frac{1}{C_f g_m R_1 R_2} \quad \text{Eqn. (2.30)}
\]

\[
\omega_{p2} = \frac{g_m C_f}{C_1 C_2 + C_f (C_1 + C_2)} \quad \text{Eqn. (2.31)}
\]

It is clear from these expressions for \( \omega_{p1} \) and \( \omega_{p2} \) that increasing the effective \( C_f \) will make \( \omega_{p1} \) smaller while making \( \omega_{p2} \) larger, splitting the poles [5]. Furthermore, this
large $C_f$ ensures that $\omega_{p1}$ is much smaller than $\omega_{p1,\text{OUTPUT}}$, and thus is the dominant pole of the circuit. This is contrary to the previous assumption that the error amplifiers are faster than the output stage, but does not invalidate the simple analysis done above. The decrease in $\omega_{p1}$ and increase in $\omega_{p2}$ caused by the pole-splitting are both actions that increase the phase margin. If $C_C$ is significantly larger than $C_1$ and $C_2$ of Eqn. 2.24, then the expression for $\omega_{p2}$ reduces to

$$\omega_{p2} = \frac{g_m}{C_1 + C_2}$$  \hspace{1cm} \text{Eqn. (2.32)}$$

In this case, increasing $C_C$ will no longer affect $\omega_{p2}$, but it will continue to decrease $\omega_{p1}$.

One problem that occurs in this compensation process is that as $C_C$ is increased, the right half plane zero $\omega_z$ given in Eqn. 2.20 decreases. This zero brings a negative phase shift that can cause stability problems, but the effects of this zero can be counteracted by introducing a resistor in series with the compensation capacitor as shown in figure 2.13. This

![Figure 2.13 Error Amplifier with Lead Compensation](image_url)
technique is known as lead compensation [6].

Analysis of this circuit results in a third order denominator with poles at locations very close to those given by Eqn. 2.23 and Eqn. 2.24, and a third high frequency pole which has little effect. The main effect of the resistor is the new location of the zero:

\[ \omega_z = \frac{-1}{C_C\left(\frac{1}{g_m} - R_C\right)} \]  
Eqn. (2.33)

It is apparent that the zero can now be cancelled by setting the value of \( R_C \) to \( \frac{1}{g_m} \). Furthermore, \( R_C \) can be made larger, moving the zero into the left half plane. In fact, it can be set to

\[ R_C = \frac{1}{g_m}\left(1 + \frac{C_1 + C_2}{C_C}\right) \]  
Eqn. (2.34)

in which case the zero will cancel the second pole of the amplifier, \( \omega_{p2} \). Increasing \( R_C \) still further will move the zero further into the left half plane, and will continue to increase the phase margin to some extent [6]. In the design process, \( C_C \) and \( R_C \) can be adjusted until an arrangement is found which maximizes the unity gain frequency \( f_t \) of the op amp for the required phase margin.

For simplicity in both design and layout of the circuit, the resistor \( R_C \) can be replaced by a triode-mode transistor. The transistor will be guaranteed to operate in the triode region since there is no path for a dc current to flow through the device. The gate of the transistor should be attached to a bias voltage which will adjust to accommodate variations due to process and temperature. It can thus be attached to \( V_{BIAS1} \), the bias voltage for the current-source transistors of the op. amp, as the bias circuit that sets this voltage will be designed to adjust to such variations. The effective resistance of the transistor can be
adjusted by adjusting the W/L ratio of the transistor. Utilizing the symmetry of the output stage, a similar compensation technique can be applied to the error amplifier driving the PMOS output transistor. The circuit diagram of the resulting, fully compensated output stage design is shown in figure 2.14.

![Circuit Diagram of Output Stage](image)

**Figure 2.14 The Fully Compensated Output Stage**

### 2.5 Biasing

As mentioned above, it is desirable to have a biasing network which is independent...
of both process and temperature variations. In particular, the MOSFET gain constant $K$ is temperature sensitive, increasing with temperature as the carrier mobility increases. The threshold voltage $V_t$ decreases with increasing temperature, and can also vary due to inconsistencies arising from the manufacturing process [5]. Variations in $K$ and $V_t$ both cause variations in the resulting current through a transistor, as is apparent from Eqn. 2.1. This results in variations in the transconductance of the transistors in the circuit, since

$$g_m = \sqrt{2\mu C_{OX} \sqrt{W/L}} \sqrt{I_D}$$

Eqn. (2.35)

and thus leads to improper circuit operation. A bias circuit which provides bias currents independent of these variations is shown in figure 2.15. Since the bias network operates on the current-mirror principle, the amplifier bias currents are now set by the device geometries only. The input is a bias current, which is equal to the quiescent current desired in transistor M12 divided by some integer, $N$:

$$I_{IN} = \frac{I_{QM12}}{N}$$

Eqn. (2.36)
To achieve the correct bias voltage at the gates of the current source transistors M12 and M13, the width of MB1 is then set to

\[ W_{MB1} = \frac{W_{M12}}{N} \quad \text{Eqn. (2.37)} \]

while the channel length remains constant. To set the current in transistors M5 and M6 in a similar manner, the width of MB2 is set to

\[ W_{MB2} = W_{MB1} \frac{I_{QM5}}{I_{QM12}} \quad \text{Eqn. (2.38)} \]

which sets the current in MB2 to the desired quiescent current in M5 divided by \( N \). Transistor MB3 allows the voltage at the drain of MB2 to differ from that at the drain of MB4, and the second bias voltage is set by choosing:

\[ W_{MB4} = \frac{W_{M5}}{N} \quad \text{Eqn. (2.39)} \]

The complete output stage, including the biasing arrangement and the load resistance and capacitance, is shown in figure 2.16.
Figure 2.16 The Complete Output Stage
References


Chapter 3 - Process and Simulation

The output stage design is implemented using TSMC’s CMOS P35 manufacturing process, which is made available through CMC and PMC-Sierra. This is a 3.3V n-well process with a minimum device length of 0.35μm and three metal layers. Since shorter channel length devices have lower parasitic capacitances and operate at higher speeds with lower supply voltages, using this sub-micron technology should allow the design of a high speed amplifier without having to pay a large penalty in power consumption. This process has a p-type lightly doped substrate, into which NMOS devices can be directly fabricated. To create PMOS devices, a well of n-type substrate must be formed, in which the device can be situated and, thus, this is known as an n-well process.

3.1 The n-well Process

In order to form this well, first a photoresist mask must be made. Photoresist is a polymer which changes properties when exposed to ultraviolet light. The silicon wafer is first given a thin coating of SiO₂, then covered in photoresist. The surface is then exposed to ultraviolet light through a glass mask, which has opaque regions through which the light does not penetrate. The photoresist which is exposed to the ultraviolet light will polymerize, which changes its molecular bonds. An organic solvent is then used, which dissolves the unexposed photoresist, but does not affect that which has been polymerized. The photoresist mask has now been created. Such masks are used in several stages of the fabrication process. The exposed SiO₂ can then be etched away using acid, and the resulting wafer appears as shown in figure 3.1. The remaining photoresist can now be removed using acetone, and the remaining oxide layer now acts as a mask during the doping process.
There are two methods for doping the well region: diffusion and ion implantation. Of the two, ion implantation is preferred as it allows greater accuracy, and therefore this method will be discussed. It involves the exposure of the wafer to a purified ion beam, with the depth to which the ions penetrate the wafer being controlled by the accelerating voltage which propels them. This is followed by an annealing step, in which the wafer is heated to about 1000°C for approximately 30 minutes, then allowed to cool. This allows bonds damaged in the ion bombardment to reform, while at the same time causing a more uniform ion concentration in the well. The resulting n well is shown in figure 3.2 [1].

With the n well fabricated, both NMOS and PMOS transistors can now be built. Processes similar to that described above are used to fabricate the devices, with different masks being used in each step. First a thin oxide layer which will act as the gate oxide is deposited. The gate oxide is then covered with SiN, and this is used as a mask for the channel stop implant and field oxide growth, which both act in isolating individual devices. Following the removal of the SiN, the gate polysilicon is deposited and patterned.
For the fabrication of an inverter, with an NMOS device in the native substrate and a PMOS device in the n well, the wafer will now appear as in figure 3.3(a). The polysilicon is patterned so that the gates of the two transistors are connected, and the gate now acts as a mask in the implants of first n+ then p+ regions which form the source and drain in the two transistors. The wafer now appears as in 3.3(b). The surface is now covered in SiO₂, which is etched away wherever a contact is required. Metal is then deposited and etched to form the required connections, as shown in figure 3.3(c). Another layer of SiO₂ can now.
be added and etched away where desired to form contacts with a second metal layer. Once the second layer of metal has been patterned as desired, the process can be repeated to allow connections to a third metal layer. Connections between the metal layers are known as vias. Finally, a passivating layer of oxide can be added to protect the chip, and openings to the bond pads are etched through the passivation layer to allow wire bonding [2].

3.2 Simulations of Output Transistors and Error Amplifiers

Detailed models of the device parameters for the CMOS P35 process allow circuit simulations to be run using Hspice software. These simulations help to verify the operation of the designed circuit, allowing the selection of correct device geometries and bias levels, and indicating any problems in circuit performance which the design theory may not have accounted for. First, using ideal op. amps with a gain of 40dB in place of the error amplifiers, simulations show the device geometries required to deliver the necessary current to the output of the circuit. The device geometries are listed in table 3.1. The devices are minimum length, to ensure fast operation and achieve the desired bandwidth. The

<table>
<thead>
<tr>
<th>Transistor</th>
<th>Width (μm)</th>
<th>Length (μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MP</td>
<td>420</td>
<td>0.35</td>
</tr>
<tr>
<td>MN</td>
<td>140</td>
<td>0.35</td>
</tr>
</tbody>
</table>

device widths are then chosen to meet the current requirements of the load. Figure 3.4 shows the simulation results for a dc sweep of the input voltage with the geometries as listed in table 3.1. The output is seen here to follow the input very closely, indicating that the required current is being supplied to the output. Once the geometries of the output
transistors have been determined, the design of the error amplifiers that drive them must be incorporated, and their operation simulated.

The error amplifiers should have a gain of approximately 40dB in order for the output stage to perform as in the simulation results of figure 3.4. In addition, as the entire output stage is desired to operate up to 100MHz, the error amplifiers must have a unity gain frequency $f_r$ greater than 100MHz, to avoid crossover distortion. In this stage of the design and simulation flow, the error amplifier shown in figure 2.5 will be considered, with quiescent current control and frequency compensation being added once the error amplifier has been incorporated into the output stage. The device geometries required for the op. amp are given in table 3.2. The devices are four times longer than minimum length in order to provide the required gain. The required bias current through the current-source transistors M5 and M6 is a total of 400μA, 200μA through each transistor, which is
Table 3.2 Device Geometries for Op. Amp Driving NMOS Output Transistor

<table>
<thead>
<tr>
<th>Transistor</th>
<th>Width (μm)</th>
<th>Length (μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1</td>
<td>420</td>
<td>1.4</td>
</tr>
<tr>
<td>M2</td>
<td>420</td>
<td>1.4</td>
</tr>
<tr>
<td>M3</td>
<td>92</td>
<td>1.4</td>
</tr>
<tr>
<td>M4</td>
<td>184</td>
<td>1.4</td>
</tr>
<tr>
<td>M5</td>
<td>600</td>
<td>1.4</td>
</tr>
<tr>
<td>M6</td>
<td>600</td>
<td>1.4</td>
</tr>
</tbody>
</table>

achieved by setting the bias voltage $V_{BIAS}$ to 0.81V. The simulated frequency response of the op.amp is shown in figure 3.5. To simulate the loading effect of the NMOS output transistor that the op. amp drives, the output node of the amplifier is attached to the gate of a transistor of the same dimensions, with its source tied to the negative rail, and its drain grounded. The results show that the op. amp achieves a gain close to 40dB and an $f_t$ of over 100MHz, and thus performs as desired.

Figure 3.5 Frequency Response of Op. Amp Driving NMOS Output Transistor
The device geometries for the error amplifier driving the PMOS output transistor, again leaving quiescent current control and frequency compensation until later design stages, are given in table 3.3. Again, devices four times longer than minimum length are used. The required bias current in current-source transistors M12 and M13, 375\(\mu\)A through each, is provided by setting \(V_{BIAS2}\) to -0.89V. Simulations similar to those performed on the other error amplifier again show a gain close to 40dB and a \(f_c\) of over 100MHz, indicating that this design achieves the desired performance.

**Table 3.3 Device Geometries For Op. Amp Driving PMOS Output Transistor**

<table>
<thead>
<tr>
<th>Transistor</th>
<th>Width ((\mu)m)</th>
<th>Length ((\mu)m)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M8</td>
<td>140</td>
<td>1.4</td>
</tr>
<tr>
<td>M9</td>
<td>140</td>
<td>1.4</td>
</tr>
<tr>
<td>M10</td>
<td>280</td>
<td>1.4</td>
</tr>
<tr>
<td>M11</td>
<td>560</td>
<td>1.4</td>
</tr>
<tr>
<td>M12</td>
<td>200</td>
<td>1.4</td>
</tr>
<tr>
<td>M13</td>
<td>200</td>
<td>1.4</td>
</tr>
</tbody>
</table>

**3.3 Simulation of Output Stage**

Once the operation of the output transistors and the error amplifiers have been individually tested under simulation, they can be incorporated into the overall output stage design, and the operation of this overall design can be simulated under load conditions. This allows the sizing of the quiescent current control transistors M7 and M14 to ensure both that the quiescent output current is kept at reasonable levels, and that the quiescent current in the two output transistors is equal to avoid any offset voltage at the output node. The quiescent current should be kept at a level between 1mA and 5mA to ensure that the
output transistors are sufficiently turned on to be well into the saturation region, while keeping quiescent power consumption at acceptable levels. The geometries of the two current control transistors are given in Table 3.4. These geometries yield an output offset voltage of only $-57\mu V$, and a quiescent current of $1.31 mA$ through each of the output transistors, for a total quiescent current level of $2.46 mA$. If a dc sweep of the input of this output stage design is performed, an unexpected shortcoming arises. Figure 3.6 shows the simulated results of a sweep of the input from the negative to the positive supply voltage. It is apparent that the output does not follow the input from rail to rail as expected, but

<table>
<thead>
<tr>
<th>Transistor</th>
<th>Width ($\mu$m)</th>
<th>Length ($\mu$m)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M7</td>
<td>105</td>
<td>1.4</td>
</tr>
<tr>
<td>M14</td>
<td>21.0</td>
<td>1.4</td>
</tr>
</tbody>
</table>

Figure 3.6 $V_{OUT}$ vs. $V_{IN}$ for Output Stage with Real Error Amplifiers
starts to level out to a maximum level when it gets within approximately 0.9V of the supply rails. Investigation of all circuit nodes in this simulation reveals that the circuit’s performance is limited by M5 and M12, the current source transistors supplying the differential input stages of the two error amplifiers. If a negative swing is considered, and assuming that for a unity gain configuration the output voltage equals the input, it can be noted that for M8 and M9 to stay turned on they require

\[ V_{GS} \geq V_t \quad \text{Eqn. (3.1)} \]

and the limiting case is therefore

\[ V_{GS} = V_t \quad \text{Eqn. (3.2)} \]

This implies that, as the input voltage decreases, the voltage at the drain of transistor M12 is forced lower. However, in order for M12 to stay in saturation the condition

\[ V_{DS} \geq V_{GS} - V_t \quad \text{Eqn. (3.3)} \]

must be met, for which the limiting condition is

\[ V_{DS} = V_{GS} - V_t = (V_{BIA\text{S}2} - V_{SS}) - V_t \quad \text{Eqn. (3.4)} \]

and the minimum input voltage for which this input stage works is therefore

\[ V_{IN,\text{min}} = V_{SS} + V_{DSS} + V_{GS} = V_{SS} + (V_{BIA\text{S}2} - V_{SS} - V_t) + V_t = V_{BIA\text{S}2} \quad \text{Eqn. (3.5)} \]

So the minimum input voltage is limited by the bias voltage for the error amplifier driving the PMOS transistor, and similar analysis shows that the maximum input voltage is set by the bias voltage for the other error amplifier, \( V_{BIA\text{S}1} \). Thus, while the two error amplifiers were designed such that their inputs could swing to the rail while they were driving the output transistor supplying the output current, it is when the corresponding transistor is not supplying the output current that they fail, allowing that transistor to turn on and draw
current from the output. At this point, the error amplifier which is still functioning correctly turns the transistor it is driving further on, as a larger voltage now starts to appear at it’s input terminals, which results in a very large current draw. This is illustrated in figure 3.7, which shows the sudden increase in total current drawn by the circuit when the error amplifiers fail.

![Figure 3.7 Total Current Draw When Error Amplifiers Fail](image)

As the output stage is only required to have a swing of $\pm 0.5$ V, this limited performance does not severely affect the design. However, to allow a large error margin in the circuit’s performance, it is desired to have a signal swing up to $\pm 0.75$ V. This condition is already met by the negative swing of the output, but the positive swing must be extended. This can be achieved by widening the current source transistors M5 and M6, which allows the same amount of current flow for a higher value of $V_{BIAS}$. Figure 3.8 shows the difference between the input and output voltages for the original sizing of M5 and M6, for the
transistors increased to be four times wider, and for the transistors 16 times wider than their original sizings. It is apparent that the difference in swing is significantly larger.

![Graph showing the relationship between V_in and V_out for different transistor sizes.](image)

**Figure 3.8 V_in - V_out for Differing Sizes of M5 and M6**

between the original size and the four times increase in size, than between the four times and sixteen times increases. Since increasing the width of these transistors incurs a penalty in bandwidth, the four times increase appears to be the optimal choice, increasing swing to achieve the ±0.75 V desired, without incurring a large loss of bandwidth. The bias voltage \( V_{BIAS} \) is now set to 0.91V, and the new transistor dimensions are given in table 3.5. Transistor M14 is also adjusted slightly to eliminate an offset voltage arising from these.

**Table 3.5 New Device Geometries of Transistors M5 and M6**

<table>
<thead>
<tr>
<th>Transistor</th>
<th>Width (µm)</th>
<th>Length (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M5</td>
<td>2400</td>
<td>1.4</td>
</tr>
<tr>
<td>M6</td>
<td>2400</td>
<td>1.4</td>
</tr>
</tbody>
</table>
changes, it's width changing from 21.0 μm to 21.3 μm. The open-loop frequency response of the output stage shown in figure 3.9 indicates that the circuit achieves the required 100MHz unity-gain bandwidth.

Figure 3.9 Open-Loop Frequency Response of the Output Stage

3.4 Adding Biasing and Compensation

Once the operation of the fundamental blocks has been established, the bias and compensation networks must be added to complete the circuit. The currents and transistor sizes of the bias network are dependent on the sizes of the current-source transistors and the integer $N$, which determines the ratio of the input bias current to the bias currents provided by the current sources. Choosing $N = 50$, the input bias current will be 7.50 μA, 50 times smaller than the current flowing through M12 and M13. It follows that the width of MB1 should be 50 times narrower than that of M12 and M13. Since the ratio of current
in M12 and M13 to that in M5 and M6 is 15:8, MB2 should be 0.53 times the width of MB1, or 0.5 times to keep the device ratios unit multiples. For this same reason, MB3 can be chosen to be the same size as MB2, and following the factoring by $N = 50$, MB4 should have a width 50 times smaller than the widths of M5 and M6. These sizings are given in table 3.6. Under simulation, the introduction of this real bias network provides the required bias voltages, and allows correct circuit operation.

**Table 3.6 Device Geometries for Bias Network**

<table>
<thead>
<tr>
<th>Transistor</th>
<th>Width (µm)</th>
<th>Length (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MB1</td>
<td>4</td>
<td>1.4</td>
</tr>
<tr>
<td>MB2</td>
<td>2</td>
<td>1.4</td>
</tr>
<tr>
<td>MB3</td>
<td>2</td>
<td>1.4</td>
</tr>
<tr>
<td>MB4</td>
<td>48</td>
<td>1.4</td>
</tr>
</tbody>
</table>

As the open-loop frequency response of the output stage has a phase margin well below $60^\circ$, compensation must now be added. Under simulation, lead compensation can first be tested using capacitors and resistors. The achievement of a $60^\circ$ phase margin by lead compensation in the two op. amps indicates that earlier assumptions in the frequency analysis of the circuit are correct. Once the required resistance values have been determined, the resistors can then be replaced with the triode-mode transistors of equal resistance. For symmetry, the error amplifier that drives the PMOS output device is compensated using a NMOS transistor, and the other error amp is compensated using an PMOS transistor. Due to the capacitances associated with the transistors, substituting transistors of equivalent resistance to the resistors does not provide identical compensation, and both the widths of the transistors and the size of the compensation capacitors require
further adjustments. The capacitance values and transistor sizings which provide
the desired 60° phase margin are given in table 3.7 and table 3.8, respectively. The open-
loop frequency response of the complete output stage is shown in figure 3.10, with both
the magnitude and phase plots included. In order to attain the 60.3° phase margin achieved
here, the unity-gain bandwidth is reduced to 93MHz, which is lower than the desired
100MHz but still gives a good margin of error above the 75MHz required for video sig-
nals.

<table>
<thead>
<tr>
<th>Capacitor</th>
<th>Capacitance (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{C1}$</td>
<td>1.3</td>
</tr>
<tr>
<td>$C_{C2}$</td>
<td>1.3</td>
</tr>
</tbody>
</table>

Table 3.8 Device Geometries of Compensation Transistors

<table>
<thead>
<tr>
<th>Transistor</th>
<th>Width (µm)</th>
<th>Length (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$MC_1$</td>
<td>12</td>
<td>1.4</td>
</tr>
<tr>
<td>$MC_2$</td>
<td>2.7</td>
<td>1.4</td>
</tr>
</tbody>
</table>

3.5 Evaluating Circuit Analysis

At this point, the capacitances and resistances of the transistors can be extracted
from the simulations, and used to test the circuit analysis of chapter 2. Substituting in the
values without the compensation capacitor gives the poles as listed in table 3.9. While fig-
ure 3.9 shows that a single dominant pole exists at approximately 1-2MHz, the results of
the first-order model of chapter 2 show poles $\omega_{p1}$ and $\omega_{p1, \text{OUTPUT}}$ placed very closely in
the 5-6MHz range. Adding $C_C$ changes $\omega_{p1}$ and $\omega_{p2}$ to the values listed in table 3.10.
Table 3.9 Poles Predicted by Chapter 2 Circuit Analysis

<table>
<thead>
<tr>
<th>Pole</th>
<th>Location</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{p1}$</td>
<td>5.1MHz</td>
</tr>
<tr>
<td>$f_{p2}$</td>
<td>129MHz</td>
</tr>
<tr>
<td>$f_{p1,,OUTPUT}$</td>
<td>6.2MHz</td>
</tr>
<tr>
<td>$f_{p2,,OUTPUT}$</td>
<td>230MHz</td>
</tr>
</tbody>
</table>

Table 3.10 Poles Predicted After Addition of $C_C$

<table>
<thead>
<tr>
<th>Pole</th>
<th>Location</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{p1}$</td>
<td>0.72MHz</td>
</tr>
<tr>
<td>$f_{p2}$</td>
<td>250GHz</td>
</tr>
</tbody>
</table>

This is seen to split the poles of the error amplifier, and make $\omega_{p1}$ the dominant pole of the circuit, as predicted. Thus, while the first order model fails to accurately predict the poles, it is useful in predicting the effects of added compensation.

### 3.6 Unity Gain Configuration

To test the intended operation of the circuit, the performance of the output stage in its unity gain configuration can be observed under simulation. When the output stage is in the unity gain configuration, the frequency response should appear as a constant 0dB, followed by a smooth roll-off at higher frequencies. The desired 3dB bandwidth is 100MHz, but as the unity gain bandwidth of the open-loop frequency response failed to achieve this mark, it is expected that this 3dB bandwidth will not be realized. It is apparent from the simulated frequency response, shown in figure 3.11, that the circuit does not behave as expected. At low frequencies, the output is close to the expected 0dB, but rather than a
smooth roll-off, the output begins to fall and then rises again to a peak, before continuing its descent. This peak leads to large, undesirable oscillations in the transient response.
of the circuit, and indicates that the circuit cannot simply be viewed as a two-pole system, as a third pole is being contributed here by the 15pF capacitance $C_L$ at the output. However, adjusting the lead compensation in the op. amps succeeds in eliminating this peak and much of the associated oscillations while maintaining a phase margin greater than $60^\circ$, indicating that the compensation technique is still effective. The new frequency response is shown in figure 3.12. The response now maintains a constant level, followed by a smooth rolloff, and has a 3dB frequency of 90MHz. The capacitance values and transistor sizings which provide this response are given in table 3.11 and table 3.12, respectively. The $f_c$ of the open-loop frequency response has dropped significantly, to 70MHz. The phase margin is $60.5^\circ$.

![Figure 3.12 Unity Gain Frequency Response with Revised Compensation](image)

Figure 3.12 Unity Gain Frequency Response with Revised Compensation

Varying the capacitive load that the output stage drives has an unexpected effect.

When the capacitive load decreases, the 3dB bandwidth decreases, where we would
Table 3.11 New Capacitance Values for Compensation Capacitors

<table>
<thead>
<tr>
<th>Capacitor</th>
<th>Capacitance (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{C1}$</td>
<td>1.1</td>
</tr>
<tr>
<td>$C_{C2}$</td>
<td>1.1</td>
</tr>
</tbody>
</table>

Table 3.12 New Device Geometries of Compensation Transistors

<table>
<thead>
<tr>
<th>Transistor</th>
<th>Width (μm)</th>
<th>Length (μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MC₁</td>
<td>20</td>
<td>1.4</td>
</tr>
<tr>
<td>MC₂</td>
<td>5.3</td>
<td>1.4</td>
</tr>
</tbody>
</table>

expect it to increase as the load gets smaller. This is further evidence that this is more than a two-pole system. Decreasing the load capacitance $C_L$ to 7pF decreases the 3dB bandwidth to 67MHz, but increases the phase margin, giving greater stability. The transient response of the output stage under the full capacitive load, $C_L=15pF$, is shown in figure 3.13. It can be seen that the oscillations in the transient response do not swing about the

Figure 3.13 Transient Response of the Output Stage
final settling value, as would occur in an underdamped second-order system, but about some rising value. This once again emphasizes the effect of another pole. While this transient response still has some oscillations, it is a significant improvement over the response corresponding to the compensation values of tables 3.7 and 3.8. Further increasing the phase margin to decrease the ringing effect causes a large decrease in bandwidth, with little improvement in settling time, so the compensation values used here are deemed appropriate.

To complete the analysis of circuit performance, Hspice simulations were used to determine the THD of the circuit. Using the.fft function, and inputting a 1V p-p, 5MHz sine wave gives a THD of 0.42%, or -47.5dB, which is well below the -30dB acceptable for video. The performance of the output stage is summarized in table 3.13. Once the

<table>
<thead>
<tr>
<th>Table 3.13 Performance Specifications of the Output Stage</th>
</tr>
</thead>
<tbody>
<tr>
<td>output swing</td>
</tr>
<tr>
<td>quiescent current</td>
</tr>
<tr>
<td>3dB bandwidth</td>
</tr>
<tr>
<td>THD (1V p-p, 5MHz sine wave)</td>
</tr>
<tr>
<td>5% settling time (1V step)</td>
</tr>
<tr>
<td>load (RL, CL)</td>
</tr>
</tbody>
</table>

design is complete, the layout of the circuit must be considered. In order to save space on the silicon die, efforts should be made to minimize circuit size. With this in mind, the large size of transistors M5 and M6 is a large price to pay in size for the small change in voltage swing that it gives. Since the voltage swing is only required to reach 0.5V, the extra swing at 0.75V is negligible for the significant increase in transistor size. The operation of the
circuit using the original sizes for M5, M6, and quiescent current control transistor M14 was therefore investigated. In addition, the bias circuit transistor MB4 must be adjusted to provide the correct bias voltage for M5 and M6. The revised transistor sizings are given in table 3.14.

Table 3.14 Revised Device Geometries to Reduce Circuit Size

<table>
<thead>
<tr>
<th>Transistor</th>
<th>Width (μm)</th>
<th>Length (μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M5</td>
<td>600</td>
<td>1.4</td>
</tr>
<tr>
<td>M6</td>
<td>600</td>
<td>1.4</td>
</tr>
<tr>
<td>M14</td>
<td>21.0</td>
<td>1.4</td>
</tr>
<tr>
<td>MB4</td>
<td>12</td>
<td>1.4</td>
</tr>
</tbody>
</table>

The frequency response of the circuit with these revised device geometries is shown in figure 3.14. Remarkably, this modification has extended the 3dB bandwidth of the circuit a further 27MHz, to 117MHz. The phase margin of the open-loop response is 61.6°. The transient response, shown in figure 3.15, has a faster settling time, while the THD remains well within the acceptable range. The improved performance is summarized in table 3.15.

This improvement in performance is likely due to the reduction in parasitic capacitance of M5 and M6, as they are significantly reduced in size. Since the bandwidth is 17MHz higher than required, the compensation could be adjusted to sacrifice some of this bandwidth for more phase margin, and thus a lower settling time. However, some loss of bandwidth is expected due to the physical limitations determined by the circuit layout. For this reason, layout is performed using the current geometries, and the circuit can then be further adjusted following layout, if desired.
Figure 3.14 Frequency Response of Circuit With Revised Device Geometries

Figure 3.15 Improved Transient Response of the Output Stage
Table 3.15 Performance Specifications of Improved Output Stage

<table>
<thead>
<tr>
<th>output swing</th>
<th>1V p-p</th>
</tr>
</thead>
<tbody>
<tr>
<td>quiescent current</td>
<td>2.46mA</td>
</tr>
<tr>
<td>3dB bandwidth</td>
<td>117MHz</td>
</tr>
<tr>
<td>THD (1V p-p, 5MHz sine wave)</td>
<td>-42.1dB</td>
</tr>
<tr>
<td>5% settling time (1V step)</td>
<td>24.8ns</td>
</tr>
<tr>
<td>load (R_L, C_L)</td>
<td>50Ω, 15pF</td>
</tr>
</tbody>
</table>

3.7 Design Layout

Once the circuit design is complete, its physical realization must be laid out. This layout can be done using Cadence design tools, in combination with the CMOSP35 tool kit provided by CMC. The circuit is laid out from the transistor components up, specifying the dimensions, placement, and connection of n-wells, active regions, gate silicon, and other transistor components. All aspects of the layout must conform to design rules set by the process technology, ensuring that the design can be manufactured as laid out. Typical NMOS and PMOS transistor layouts are shown in figure 3.16 (a) and (b), respectively. In this case, the transistors have their drain connected to the substrate.

Once the individual transistors and capacitors have been laid out, they must be connected. As this circuit contains a relatively small number of transistors, there is no need for complex VLSI layout techniques to create large transistors. Rather, a large transistor can be broken down into several individual ones, which are then connected in parallel. For example, transistor M5, which is 600μm wide, can be broken down into 12 parallel 50μm transistors. Where convenient, transistors with the same gate connection can be attached using the gate silicon. In all other cases, transistors or capacitors are
connected by one of the three metal layers, with the appropriate vias and contacts. With the large currents necessary in the output transistors, care is taken to ensure that the metal connections between these transistors and the output are wide enough that the maximum allowed current density is not exceeded. Once the circuit has been laid out, bonding pads must be added to allow wire bonding between the circuit and the input and output pins on the chip package in which the device is placed. The circuit layout is shown in figure 3.17. Once completed, the design layout can be extracted from Cadence and simulations performed using Hspice. This ensures that the layout corresponds exactly to the circuit design, and also indicates any performance limitations imposed by the layout. The performance specifications derived from the extracted layout are given in table 3.16.

The 3dB bandwidth has decreased by 7MHz, but is still 10MHz greater than the
100MHz required. There is also a slight increase in settling time, and a 1 dB increase in THD, but both remain well within acceptable levels. The compensation could now be adjusted to trade off the surplus bandwidth for more phase margin, which would decrease the settling time. However, one alternative to this is to leave the compensation as is, and
investigate the possibility of using the output stage to drive different capacitive loads. Simulations reveal that the circuit can drive as low as 10pF load capacitance and still maintain a 3dB bandwidth of over 100MHz. In addition, as the phase margin is higher for this smaller load, the settling time would improve.

The final dimensions of all transistors are summarized in table 3.17. Once the design and layout have proved functional under simulation, this layout can be sent to the manufacturer for fabrication. A bonding diagram is sent with the layout to specify the connections between the bonding pads and pins on the chip packaging. Once the circuit has been fabricated and delivered to the designer, measurements are performed to determine if it performs as predicted under simulation.
## Table 3.17 Summary of All Transistor Dimensions

<table>
<thead>
<tr>
<th>Transistor</th>
<th>Width (µm)</th>
<th>Length (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1</td>
<td>420</td>
<td>1.4</td>
</tr>
<tr>
<td>M2</td>
<td>420</td>
<td>1.4</td>
</tr>
<tr>
<td>M3</td>
<td>92</td>
<td>1.4</td>
</tr>
<tr>
<td>M4</td>
<td>184</td>
<td>1.4</td>
</tr>
<tr>
<td>M5</td>
<td>600</td>
<td>1.4</td>
</tr>
<tr>
<td>M6</td>
<td>600</td>
<td>1.4</td>
</tr>
<tr>
<td>M7</td>
<td>105</td>
<td>1.4</td>
</tr>
<tr>
<td>M8</td>
<td>140</td>
<td>1.4</td>
</tr>
<tr>
<td>M9</td>
<td>140</td>
<td>1.4</td>
</tr>
<tr>
<td>M10</td>
<td>280</td>
<td>1.4</td>
</tr>
<tr>
<td>M11</td>
<td>560</td>
<td>1.4</td>
</tr>
<tr>
<td>M12</td>
<td>200</td>
<td>1.4</td>
</tr>
<tr>
<td>M13</td>
<td>200</td>
<td>1.4</td>
</tr>
<tr>
<td>M14</td>
<td>21</td>
<td>1.4</td>
</tr>
<tr>
<td>MN</td>
<td>140</td>
<td>0.35</td>
</tr>
<tr>
<td>MP</td>
<td>420</td>
<td>0.35</td>
</tr>
<tr>
<td>MC₁</td>
<td>20</td>
<td>1.4</td>
</tr>
<tr>
<td>MC₂</td>
<td>5.3</td>
<td>1.4</td>
</tr>
<tr>
<td>MB₁</td>
<td>4</td>
<td>1.4</td>
</tr>
<tr>
<td>MB₂</td>
<td>2</td>
<td>1.4</td>
</tr>
<tr>
<td>MB₃</td>
<td>2</td>
<td>1.4</td>
</tr>
<tr>
<td>MB₄</td>
<td>12</td>
<td>1.4</td>
</tr>
</tbody>
</table>
References


Chapter 4 - Results and Analysis

A microphotograph of the fabricated circuit is shown in figure 4.1. The circuit is shown complete with bond-wire connections, which are part of the packaging. These fabricated circuits are tested in the lab to evaluate their performance. First, the circuit must be set up. This involves establishing circuit connections, and setting power supply and bias inputs. Once this is complete, various lab instruments are used to both provide the circuit input signal and monitor, measure, and analyze the output signal.
4.1 Experimental Set-Up

The fabricated circuits are packaged in the 40 pin dual-inline package available through CMC, which allows testing of the circuit using conventional lab-bench equipment. High-speed connections are ensured by mounting the chip on a custom designed printed circuit board. The bottom of the fiberglass board is covered by a copper ground plane, while the copper traces necessary for circuit connections run across the top of the board. The dimensions of the traces leading to the input and output pins are chosen to provide a 50Ω impedance, and lead to BNC connectors which allow connection to 50Ω cables. The package is soldered flat to the board, with ground connections made through holes drilled through to the ground plane, and the input bias current and power supplies are capacitively decoupled at the chip pins. This is shown in figure 4.2. The two power supplies are supplied by voltage sources, while the input bias current is supplied by a voltage source connected to the $I_{BIAS}$ input through a 2MΩ resistor. The voltage sources used are listed in table 4.1. $I_{BIAS}$ is monitored using a Hewlett-Packard 34401A multimeter.

<table>
<thead>
<tr>
<th>Supply</th>
<th>Voltage Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD}$</td>
<td>Heathkit IP-2718</td>
</tr>
<tr>
<td>$V_{SS}$</td>
<td>Hewlett-Packard E3611A</td>
</tr>
<tr>
<td>$I_{BIAS}$</td>
<td>Hewlett-Packard E3610A</td>
</tr>
</tbody>
</table>

The test setup for frequency response measurements is illustrated in figure 4.3(a). Figure 4.3(b) shows the setup for determining the transfer characteristic, the THD, and the transient response of the amplifier.
Figure 4.2 Chip Package Attached to Circuit Board

Figure 4.3(a) Test Setup for Frequency Response

Figure 4.3(b) Setup for Transfer Characteristic, THD, and Transient Response
4.2 Frequency Response

The frequency response of the circuit is measured by connecting the buffer input and output to a Hewlett-Packard 8754 network analyzer. The frequency response for the buffer with an input power of -10dBm is shown in figure 4.4. The frequency scale on the x-axis goes from 300kHz to 1GHz, while the y-axis shows the magnitude of the output voltage, with a scale of 5dB/division. At 300kHz, the output is at 0dB, and the 3dB frequency is 122MHz. The frequency response is as expected until it rises in a peak at approximately 200MHz.

![Figure 4.4 Measured Frequency Response](image)

4.3 Transfer Characteristic

The transfer characteristic of the amplifier is measured by inputting a low-frequency 1V p-p sine wave using a Wavetek Model 166 function generator. The output and input are both connected to a Hewlett-Packard 54504A 400MHz digitizing oscilloscope, which plots output vs. input. This plot, shown in figure 4.5, shows the buffer achieving the desired 1V signal swing.
Due to the output limits of the oscilloscope, the axes are not the same scale, but for both $V_{IN}$ on the x-axis, and $V_{OUT}$ on the y-axis, the plot traces from -0.5V to +0.5V. It is apparent from the flattening of the plot at the origin that the circuit is contributing crossover distortion to the output. This crossover distortion varies from chip to chip. Figure 4.6, for example, shows the output of a chip with lower crossover distortion.

![Figure 4.5 Transfer Characteristic: $V_{OUT}$ vs. $V_{IN}$](image)

![Figure 4.6 Transfer Characteristic with Lower Crossover Distortion](image)

### 4.4 THD Analysis

The varying crossover distortion is visible when a 5MHz, 1V p-p sine wave is input for THD analysis. The signal is generated by a Ramsey RSG-10 signal generator. Figures 4.7(a) and (b) show the oscilloscope plots for the two circuits whose transfer
Figure 4.7(a) Amp1 Output for 5MHz, 1V p-p Sine Wave Input

Figure 4.7(b) Amp2 Output for 5MHz, 1V p-p Sine Wave Input
characteristics are shown above. Amp1 and Amp2 are the buffers corresponding to figure 4.5 and figure 4.6, respectively. The larger crossover distortion is clearly visible in figure 4.7(a). This larger crossover distortion obviously leads to increased THD, as is apparent from the results given in table 4.2, which are generated by observing the output spectrum using a Hewlett-Packard 3588A spectrum analyzer. The difference in THD is greater than 20dB, with Amp2 meeting the required THD specs, while Amp1 fails to meet this requirement.

**Table 4.2 THD Levels for Varying Levels of Crossover Distortion**

<table>
<thead>
<tr>
<th>Buffer</th>
<th>THD</th>
</tr>
</thead>
<tbody>
<tr>
<td>Amp1</td>
<td>-12.6dB</td>
</tr>
<tr>
<td>Amp2</td>
<td>-32.8dB</td>
</tr>
</tbody>
</table>

**4.5 Transient Response**

A Hewlett-Packard 8007B pulse generator is used to generate a 1V step input to test the transient response of the circuit. The resulting output of Amp1 is shown in figure 4.8(a), and the output of Amp2 is shown in figure 4.8(b). In each case, a trace of the input step precedes the output trace. The measured settling times from the start of the output step are given in table 4.3. The two chips have differing settling times, with the crossover distortion adding an extra 1.6ns. This additional time occurs, as expected in the case of crossover distortion, in the rise time. The effect of the crossover distortion can be clearly seen.

**Table 4.3 Amp1 and Amp2 Settling Times**

<table>
<thead>
<tr>
<th>Buffer</th>
<th>5% Settling Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>Amp1</td>
<td>31.4ns</td>
</tr>
<tr>
<td>Amp2</td>
<td>29.8ns</td>
</tr>
</tbody>
</table>
seen in the bump at the start of the output rise of Amp1.

Figure 4.8(a) Amp1 Transient Response

Figure 4.8(b) Amp2 Transient Response
4.6 Quiescent Current and Offset Voltage

With the input grounded, the quiescent current is measured using the multimeter. The output offset voltage is also measured. These results are summarized in table 4.4. As expected, the circuit with the larger crossover distortion has a lower quiescent current, indicating that the output transistors are not correctly biased. The larger output offset voltage of Amp2 indicates that, while they are biased closer to expected levels, the two output transistors are not biased to have equal currents.

Table 4.4 Quiescent Current and Offset Voltage for Amp1 and Amp2

<table>
<thead>
<tr>
<th>Buffer</th>
<th>Quiescent Current</th>
<th>Offset Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Amp1</td>
<td>1.21mA</td>
<td>0.67mV</td>
</tr>
<tr>
<td>Amp2</td>
<td>2.10mA</td>
<td>2.23mV</td>
</tr>
</tbody>
</table>

4.7 Results Summary

The optimum testing results, corresponding to Amp2 are summarized in table 4.5.

Table 4.5 Summary of Optimum Results

<table>
<thead>
<tr>
<th>output swing</th>
<th>1V p-p</th>
</tr>
</thead>
<tbody>
<tr>
<td>output offset voltage</td>
<td>2.23mV</td>
</tr>
<tr>
<td>quiescent current</td>
<td>2.10mA</td>
</tr>
<tr>
<td>3dB bandwidth</td>
<td>122MHz</td>
</tr>
<tr>
<td>THD (1V p-p, 5MHz sine wave)</td>
<td>-32.8dB</td>
</tr>
<tr>
<td>5% settling time (1V step)</td>
<td>29.8ns</td>
</tr>
<tr>
<td>load</td>
<td>50Ω, 15pF</td>
</tr>
</tbody>
</table>
Chapter 5 - Discussion and Conclusions

Once all measurements are complete, the buffer’s performance can be compared with that of previously reported amplifiers, and with the results predicted in simulation. Discrepancies between real and predicted results can be analyzed, and their causes used to suggest areas for future work on this design.

5.1 Performance Relative to Other Buffers

Given the 3dB frequency, the power consumption, and the resistive load, the performance of the buffer can be plotted on the graph of figure 1.1. The results are shown in figure 5.1. The buffer designed in this thesis is positioned far beyond the performance frontier of figure 1.1. It should be noted that the performance figure for this buffer would deteriorate if crossover distortion problems were corrected, which would increase the qui-
escent power. Similarly, correcting the frequency response would lower the bandwidth. However, the main reason for the superior performance is the use of shorter channel technology with lower power supply voltages, which allows a significant increase in bandwidth at comparable power levels.

Using the output swing achieved, performance can also be plotted on the graph of figure 1.2, as shown in figure 5.2. Here the performance is seen to be inferior to other reported designs. This is due to the relatively low output swing of the buffer, and indicates a potential area for improvement in future work.

![Graph showing performance comparison](image)

Figure 5.2 Relative $P_{NORM}$ vs. $V_{OUT}^2$ Performance of this Buffer

### 5.2 Results vs. Simulation

Simulations did not predict the crossover distortion which arose in the fabricated circuits. This is because they did not account for the variations in threshold voltage which
occur in the manufacturing process. Thus, while the aspect ratios of transistors M7 and M14 were set to bias the output transistors at correct quiescent levels, process variations in all the transistors, including M7 and M14, cause offset voltages in the error amplifiers. This upsets the bias arrangement, with the resulting voltage at the gates of the output transistors leaving them insufficiently turned on, which has severe effects for input voltages close to zero. A similar effect can be shown in simulation by varying the aspect ratios of M7 and M14 to alter the biasing of the output transistors. Figure 5.3 shows the results of a 20% increase in M7 and M14 for a 1V p-p, 5MHz sine wave, as used in THD analysis.

![Graph showing simulated crossover distortion](image)

**Figure 5.3 Simulated Crossover Distortion**

The frequency compensation network was also subject to process variations, which caused the unexpected peak in the frequency response at approximately 200MHz. In this case, the variations affected MC1 and MC2, the two triode-mode transistors which act as lead-compensation resistors. Variations in the threshold voltage change the expected resis-
tance value of the transistor, and thus make the compensation inadequate. This can again be modeled in simulation by varying the aspect ratio of transistors MC₁ and MC₂. One such simulated result is shown in figure 5.4.

![Graph showing frequency response](image)

Figure 5.4 Simulated Compensation Problems

### 5.3 Conclusions

Using the optimum performance specs of the buffer amplifier, those corresponding to the chip with low crossover distortion, the design meets the performance goals. The buffer drives a 50Ω, 15pF load while achieving a half-power bandwidth of 122MHz, with an output voltage swing of 1V p-p, and a THD of -32.8dB. This is achieved while maintaining a quiescent current level of only 2.10mA. A 5% settling time of 29.8 ns is achieved for a 1V input step. However, there is an unsatisfactory peak in the frequency response at approximately 200MHz, and crossover distortion makes the buffer unsuitable for small
signals. Correction of these problems will increase the quiescent current level and
decrease bandwidth, but it should be possible to make the adjustments while keeping these
two parameters within acceptable levels. Furthermore, these corrections will improve the
THD of the circuit and allow operation for any input level from 0 to ±0.5V.

The use of shorter channel technology with reduced supply voltage has produced
buffer amplifier that far outperforms others reported in terms of bandwidth per power. This
is due to the increased speed of the short channel devices, while the use of a lower voltage
supply lowers power consumption. The buffer does not perform well compared to others
in terms of output voltage swing squared per power, due to its limited output swing.

First order models used to analyze the circuit predicted trends, but were not accu-
rate in predicting pole placements. This shows that the first order analysis is useful in pro-
viding an understanding of the circuit operation, though it obviously lacks the accuracy of
a 28-level SPICE model. Hspice simulations closely model the circuit behavior, but do not
account for the effects of process variations. This is verified by the ability to simulate
crossover distortion by varying the sizes of quiescent current control transistors, and simu-
late a peak in the frequency response by adjusting the sizes of the compensation transis-
tors.

5.4 Future Work

One technique which could be used to reduce the crossover distortion would be to
alter the output stage to a pseudo-source-follower (PSF) configuration. This would involve
adding a source-follower output stage in parallel with the existing output stage. The
source-follower stage would then operate for the low input voltages, and the existing out-
put stage would take over at higher input levels. Another way to reduce crossover would be to adjust the error amplifier design. The quiescent current control transistors could be removed, and the offset could instead be generated by varying the relative widths of the two input transistors. The offset would then be based on device geometries, avoiding sensitivity to process variations. This has the added advantage of removing unnecessary transistors from the circuit.

In order to avoid distortion at high frequencies, the bandwidth of the error amplifiers should be improved to provide relatively high gain even at 100MHz. Possible ways of increasing this bandwidth should be investigated. Stricter compensation must also be applied to improve the frequency response. One approach is to compensate the two amplifiers differently, rather than treating them as identical. One of the amplifiers can be made to have a dominant pole lower than the other, which eliminates the likelihood of stability problems occurring simultaneously in both of them. This should make the compensation simpler and less sensitive to the process variations.

The output swing of the amplifier should be increased to give a performance comparable to other reported buffer amplifiers. While the swing will be limited by the lowered supply voltage, the current limitation imposed by the error amplifier failure can be overcome. One possibility is to design the error amplifier driving the NMOS output transistor to turn off during a positive input swing, holding the gate of that transistor at quiescent levels. This would avoid the failure of the amplifier which limits the positive output swing. The other error amplifier could be designed to turn off in a similar manner for negative input voltage swings.
Appendix A - Glossary of Terms

Class AB  An output stage biased at a small current; so both transistors conduct for small input signals and crossover distortion is virtually eliminated.

Crossover Distortion  Distortion in the output waveform which occurs when neither output transistor is conducting.

Common-Source  A common-source output stage consists of an NMOS and a PMOS transistor with their gates attached the input, their drains attached to the output, and their sources attached to the negative and positive supply rails, respectively.

Common-Mode Input Range  The range of inputs over which the differential pair acts as a linear amplifier for differential signals.

E-field scaling  The reduction of supply voltage to maintain similar electronic field levels in the transistor after reductions in device length.

Linearity  The accuracy with which the amplifier reproduces the input signal.

Parasitic Capacitance  Capacitance which appears in the transistor due to it’s physical nature, and impedes high-frequency performance.

Quiescent Current  The current consumed by the circuit for zero input voltage.

Rail-to-Rail  The range from the positive supply voltage to the negative supply voltage.

Source-Follower  A source-follower output stage consists of an NMOS and a PMOS transistor with their gates attached the input, their sources attached to the output, and their drains attached to the positive and negative supply rails, respectively.

Unity-Gain  The unity gain configuration for an amplifier is a configuration in which the output is fed back to the input, such that the output waveform is the same voltage as the input, giving a gain of one.