APPLICATIONS OF QUASI-FLOATING-GATE TRANSISTORS FOR USE
IN LOW-VOLTAGE CLOSED-LOOP AMPLIFIER CIRCUITS

BY

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ABSTRACT

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The current trend for today's computing products has been mobile technology solutions. These products include cellular phones, laptop computers, personal digital assistants (PDA), and more. In order to provide reliable computing and communication devices such as the ones listed above, the components necessary to construct these devices must be designed for a low-power environment. This implies that the supply voltage and supply currents must be lowered to realize longer battery life and thus consumer approval.

A novel design technique for closed-loop amplifier circuits, suited to very low supply voltages, is proposed. This paper will show a method known as Quasi-Floating-Gate (QFG) MOS transistors that allows the operation of amplifier circuits at very low supply voltages. QFG transistors are particularly suitable to...
applications involving closed-loop amplifier circuits based on multiple-input capacitive dividers. QFG transistors have noticeable gains over current floating-gate MOS transistors in that floating-gate MOS structures are subject to Gain-Bandwidth product degradation and large initial floating gate charge.

The applications presented in this paper are vital for the mobile system environment. Included herein are a programmable gain inverting amplifier, a sample and hold circuit, and a digital-to-analog converter, which are all composed of QFG input pair transistors. Each circuit will be discussed in detail as well as the building blocks for these circuits, including the QFG transistor.
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1 INTRODUCTION

The communications, electronics, and computer industries are constantly striving to create products that require very low power to operate. From cellular phones to portable DVD players, the need for low-power components is becoming increasingly important. Over the past few years several different methods, including design considerations to new technologies, have been proposed to operate said devices at lower power specifications. In the following text, many topics of low-voltage (LV) techniques will be covered. This chapter will contrast these designs with the recently proposed method of Quasi-Floating Gate (QFG) transistors. In particular, this section will cover a category of circuit topology that is particularly suited to QFG transistors.

1.1 Low-Voltage (LV) Techniques

Many different design strategies and CMOS technologies exist for the implementation of low-voltage/low-power devices. The main requirement for low-voltage (power) operation is to maintain the same speed, accuracy, and area of current “high-voltage” designs. These techniques can be broken into several categories, which include technology considerations and LV implementation techniques. Both of the above strategies have benefits and drawbacks and will be discussed in this section starting with technology considerations.

1.1.1 Technology Considerations

Some proposals for reducing the supply requirements of today’s battery-powered mobile systems have been based purely on the technology used to create the circuitry. One such method is to use multi-threshold transistor technologies. The downside is that this technology tends to be expensive and low threshold volt-
age transistors show considerable leakage [4]. Another technology-based strategy is to use BiCMOS processes. In recent years, the push for mixed-signal designs, primarily by the digital CMOS designers, have lead researchers to develop novel ways for reproducing circuits with the same characteristics of BiCMOS designs. This is advantageous because the CMOS technology is less expensive than the BiCMOS. At very high frequencies, integrated designs have primarily involved GaAs as well as SiGe. For radiation-hard applications, such as military and aerospace, the use of Silicon-On-Insulator (SOI) technology has proven very valuable. In any case, the idea is to maintain a low-cost alternative in existing CMOS technologies that will realize the same performance gains shown in these alternate processes.

1.1.2 Implementation Techniques

Several transistor implementation techniques can be employed to lower the supply voltage. Within this section, three techniques will be covered: i) bulk-driven MOSFETs, ii) floating-gate MOSFETs, and iii) self-cascoded MOSFETs. Each of these topics can be seen in more detail in the tutorial paper by S. Yan and E. Sanchez-Sinencio in [4]. This section will show the basic operation and structure for each topology.

1.1.2.1 Bulk-Driven MOSFETs

Bulk-driven MOSFETs offer a few desirable qualities for low-voltage designs. Typically used as the transistors in the input pair of a differential amplifier, bulk-driven transistors offer the ability to operate without concern for the threshold voltage. In other words, by keeping the gate-source voltage, $V_{GS}$, constant, and thus the DC quiescent current $I_D$ constant, the signal can be transmitted by applying the input to the bulk-source voltage, $V_{BS}$, terminal. Figure [1.1] shows the cross-section and implementation of a bulk-driven MOSFET. Utilizing this technique creates a JFET type transistor and allows the circuit to operate based
on the transconductance at the bulk interface, $g_{mb}$, rather than the gate transcon-ductance, $g_m$. It has been shown in literature [5] that, for bulk-driven transis-tors, the voltage swing is increased and a minimum operational supply voltage is achieved. The drawbacks to the bulk-driven transistor implementation is that $g_{mb}$ is considerably less than $g_m$, about a factor of 0.2 to 0.4 [5]. The limitation in transconductance translates to a poor gain-bandwidth product and a worse frequency response. These transistor implementations also have a technology lim-itation. That is, in an N-well technology only a bulk-driven PMOS transistor can be implemented and vice versa. Hence, this limits the designer’s choices when creating low-voltage circuitry.
1.1.2.2 Floating-Gate MOSFETs

Interestingly enough, other researchers have employed techniques used in digital designs to analog low-voltage circuitry. Floating-gate MOSFETs have been available in digital EEPROM and are now being used for the design of amplifier circuits as well as digital-to-analog converters, both of which are of particular interest to this research. The layout for a 2-input FGMOS and equivalent circuit schematic for an N-input floating-gate MOSFET are shown in Figure 1.2 labeled (a) and (b), respectively. The term “floating” comes from the fact that the input voltages are capacitively, or AC, coupled to the gate of the input pair for differential amplifiers. This voltage can be expressed as the sum of the charge on each input capacitor plus the charge found on the parasitic capacitances associated with the transistor. The floating-gate voltage can be described as

\[
V_{FG} = \left( Q_{FG} + C_{GD}V_D + C_{GS}V_S + C_{GB}V_B + \sum_{i=1}^{n} C_{Gi}V_{Gi} \right)/C_{\Sigma} \quad (1.1)
\]
where $Q_{FG}$ is the static charge on the floating-gate and $C_{Σ}$ is the total capacitance seen at the floating gate. According to [4] the floating gate voltage, $V_{FG}$, is independent of the drain voltage, $V_D$, and, due to the parasitic capacitance $C_{GD}$, the output impedance is degraded when compared to that of a conventional MOSFET.

One main advantage to using the floating gate design is the electrical isolation provided by the AC coupling capacitors. Another advantage is that the threshold voltage at the gate of the transistor can be programmed using several methods that include ultra-violet light, hot electron injection, and Fowler-Nordheim tunneling. The downside to the programming process are numerous. For one, most of the methods for changing the threshold voltage require a large voltage differential, thus defeating the purpose of a low-voltage design. Others rely on added circuitry yielding larger area on chip. In addition, the initial charge problem can also lead to undesirable results of a DC offset at the transistor gate. In [6], it has been shown that the floating-gate technique based on capacitive dividers also leads to degraded gain-bandwidth products. This is because the input capacitive dividers act as coupling capacitors that degrade the signal path as the frequency increases.

In the case of MITE circuits presented in [6], the capacitance values are required to be small in order to minimize the gain-bandwidth reduction.

1.1.2.3 Self-Cascoded MOSFETs

Cascoded MOSFET structures have been employed in a number of analog designs. Primarily, the conventional cascode design is used to boost output impedance of current mirrors and gain stages of amplifier structures. However, this can cause larger voltage drops due to the operation of each cascoded transistor. Thus, one implementation method is to use the self-cascode configuration. Shown in Figure 1.3 a self-cascoded structure allows for a lower voltage drop but higher output impedance [7]. Transistor M1 operates in non-saturation and transistor M2 operates in the saturation region. According to [4], when $\left(\frac{w}{L}\right)_2 \gg \left(\frac{w}{L}\right)_1$, the
circuit behaves like transistor M1 operating in saturation without channel-length modulation effects. The output resistance is roughly proportional to \(\frac{(W/L)_2}{(W/L)_1}\). An alternative to the \((W/L)_2 \gg (W/L)_1\) approach is the use of a multiple threshold technology for the self-casode design. However, this method is expensive as discussed earlier. In addition, the self-casoded structure only allows for very small improvements in output resistance resulting in small gain improvements on the order of 6dB.

1.2 The Quasi-Floating-Gate MOSFET

The Quasi-Floating-Gate MOSFET is very similar to the floating-gate MOSFET. Both types of transistors utilize AC capacitive weighted input voltage dividers to allow signals to be coupled to the gate of the transistor. In the case of the floating-gate transistor, the DC biasing point for the transistor is left floating. This can cause numerous problems such as the necessity for programming the threshold voltage and floating gate charge. The Quasi-Floating Gate (QFG) MOSFET is not subject to these undesirable traits. The idea is very similar to the floating-gate transistor. Again, weighted voltage input dividers are used at the gate of the transistor, however, the gate is not left floating at DC. Instead, a large valued resistor is attached to the gate of the transistor and then connected.
to one of the power rails. In other words, for an NMOS (PMOS) transistor, the gate is tied to $V_{DD}$ ($V_{SS}$) through a large value resistor. This resistor, in practice, is implemented as a reverse-biased diode-connected transistor. So for a PMOS (NMOS) transistor, an NMOS (PMOS) transistor is used as the large value, DC biasing resistive element. By utilizing the large resistance, the quiescent voltage at the gate of transistor is based to the power rail allowing for reduced supply requirements. This allows the input stage of a CMOS Op-Amp using QFG transistors to operate in the saturation region and with low-voltage requirements. Figure 1.4(a) shows a 2-input layout of a P-type QFG transistor and Figure 1.4(b) shows the equivalent circuit representation of an N-input PMOS QFG transistor. The AC voltage at the gate of the QFG transistor can be found by simple inspection of the input capacitance voltages and the parasitic capacitances of the transistor. The circuit can be simplified to a frequency dependent voltage divider circuit using the leakage resistance, $R_{\text{leak}}$, and the total capacitance, $C_T$. The gate voltage, $V_G$, 

![Figure 1.4: Quasi-Floating Gate MOSFET (a) layout (b) schematic symbol with parasitic capacitors](image-url)
can be expressed as a voltage divider circuit equal to

\[ V_G = V_{in} \frac{sR_{\text{leak}}C_T}{1 + sR_{\text{leak}}C_T} \]  

(1.2)

where \( C_T = \left( \sum_{i=1}^{N} C_i + C_{GD} + C_{GB} + C_{GS} + C'_{GB} \right) \) and \( C_i \) is the \( i^{th} \) input capacitance and has an associated input voltage, \( V_i \). By substituting

\[ V_{in} = \left( \sum_{i=1}^{N} C_i V_i + C_{GD}V_D + C_{GB}V_B + C_{GS}V_S \right)/C_T \]  

(1.3)

into Equation (1.2), \( V_G \) becomes

\[ V_G = \left( \sum_{i=1}^{N} C_i V_i + C_{GD}V_D + C_{GB}V_B + C_{GS}V_S \right) \frac{sR_{\text{leak}}}{1 + sR_{\text{leak}}C_T}. \]  

(1.4)

The equivalent circuit created is a high-pass filter with cutoff frequency equal to \( \frac{1}{2\pi R_{\text{leak}}C_T} \). As stated earlier, the pull-up or pull-down resistor that weakly connects the gate of the input transistor to one of the power rails can be implemented by the large leakage resistance of a reverse-biased PN junction of an NMOS (PMOS) transistor for a PMOS (NMOS) QFG MOSFET. The pull-up transistor operates in the cutoff region allowing the resistance to be quite large. Upon further inspection, the exact value of \( R_{\text{leak}} \) is unimportant nor is the exact value of the total capacitance, \( C_T \) needed. The only consideration for the value of \( R_{\text{leak}} \) is that it is large enough so as to not distort the circuit operation at the lowest frequency required.

The input signal(s) to the QFG transistor are superimposed onto the value of the DC voltage that has been placed at the gate. So, if an NMOS transistor is used as the QFG MOSFET, then the input signal is superimposed onto \( V_{DD} \) and vice versa for the PMOS QFG transistor. As long as the source-body junction of the reverse-biased cutoff transistor does not become forward-biased, this method of signal transfer is not a problem. Theoretically, the diode can become forward biased if the gate voltage drops below the rail voltage by an amount equal to the cut-in voltage of the source-body junction, typically 0.5V to 0.7V. For feedback amplifiers, this problem becomes less likely. Such is the case with the D/A converter, where the AC voltage swings become almost negligible.
Not only does the method of QFG transistors lower the voltage supply requirements, it also eliminates the initial charge problems associated with true floating-gate approaches \[6\]. Another benefit to the QFG transistor is the transistor is able to operate in continuous-time. QFG transistors have proven frequency response at very low frequencies and experimental results for the implementation of QFG transistors has been shown in \[3\].

1.3 Research Focus

This research will attempt to show a novel technique for low-voltage design. Of primary interest is developing/discovering circuit topologies that are well suited for the use of QFG transistors. Three such applications are proposed that yield results favorable to the QFG transistor implementation. Previous implementations of QFG transistors in low-voltage RF circuits has been shown in \[3\]. All of the circuits that will be discussed in this thesis can be placed in a category known as closed-loop amplifier structures where QFG transistors are used in the input stage of an operational amplifier. QFG transistors are particularly suitable to the closed-loop amplifier design structure. Each contain multiple input capacitors acting as AC weighted voltage dividers. Fully-differential closed-loop implementations are essentially feedback amplifiers that connect each of the input QFG transistors to the opposite polarity output terminals through capacitors. Operation at very low supply voltages is possible while also allowing for gain-bandwidth products of tens of MHz in current CMOS technology. The capacitive feedback leads to very high input resistance compared to conventional inverting amplifiers with resistive feedback. Many other advantages are present in closed-loop configurations for QFG MOSFETs:

1. For QFG transistors used as the input pair for differential amplifiers, the source and bulk voltages are the same (and the drain voltages are very similar as well). The advantage to this is that when computing the differential gate
voltage, the parasitic capacitance terms cancel [6].

2. The capacitive feedback not only improves the input impedance but it also minimizes the input signal swing around the voltage rails in the QFG transistor gates. This allows the use of very nonlinear resistors for the pull-up or pull-down elements leading to compact designs.

3. The QFG resistors set the DC bias voltage at the input of each gate allowing operation at minimum supply voltages and avoids the need for level shifting in the feedback loop to set the input and output DC levels.

The last item leads to one of the disadvantages of the QFG MOSFET. The DC offset voltages at the gates of the input pair can cause the output of the amplifier to saturate. By utilizing capacitors in the feedforward and feedback paths, there is no DC path. Thus, the input offset voltages are increased by the gain equal to the open-loop gain of the amplifier. Thus, the designer must consider that this trait can cause the output voltage to saturate and must design the amplifier accordingly.

Analysis will be performed to show the functionality, performance, and advantages of the proposed QFG circuits. Before each of the topologies is shown, the building blocks for each circuit will be discussed. Specifically, the OTA (Operational Transconductance Amplifier) will be covered in theoretical and simulation detail in Chapter 2. Careful consideration must be taken in designing said OTA for use in low-voltage designs that include QFG transistors. Once the OTA specifics have been covered, this thesis will present each circuit in detail from theoretical performance through simulation and experimental results. Following the OTA, a programmable gain amplifier, sample and hold circuit, and digital-to-analog converter will be explored in detail.
2 OPERATIONAL TRANSCondUCTANCE AMPLIFIER

2.1 Introduction

The Operational Transconductance Amplifier (OTA) chosen for this research was chosen based on several key characteristics. However, before discussing the implemented OTA structure, the conventional OTA structure must be introduced. Figure 2.1 shows the schematic symbol for a single-ended OTA.

![Figure 2.1: Single-Ended OTA Schematic Symbol](image)

The simplest explanation for the operation of an OTA is a device that translates a differential voltage into an output current. This implies that the device is most suitable for capacitive loads. This is because a resistive load could decrease the output gain and thus reduce the effectiveness of the amplifier. The conventional OTA structure is shown in Figure 2.2. The basic operation is as follows. A biasing current source is connected to the sources of the differential input pair transistors, M1 and M2. When $V_{IN+}$ equals $V_{IN-}$, the signal currents generated by M1 and M2 are equal. This current is then mirrored to the outer shell of the OTA by the mirrors M3-M5 and M4-M6. Transistors M7 and M8 form a mirror that
sinks current from the output node while the M4-M6 mirror sources current to the output node. Thus, for equal value input signals, the output current is zero. For a differential input signal, the operation is very much the same, however, the key difference is that the currents generated by M1 and M2 are not equal. This allows the differential pair to amplify the input to the outer shell. The M4-M6 mirror then will push or pull the current from the output node while the M3-M5 mirror using the M7-M8 mirror will pull or push the current at the output node. Thus, creating an amplified output current proportional to the differential input signal and the transconductance of the amplifier. The open-loop gain of the conventional OTA can be shown as

\[ A_V = G_m R_{out} \]  

(2.1)
where $G_m$ is the transconductance gain of the OTA and $R_{out}$ is the total output resistance of the OTA given by $R_{out} = r_{o6} || r_{o8}$, where $r_{o6}$ and $r_{o8}$ are the small-signal output resistance of transistors M6 and M8, respectively. The small-signal OTA transconductance is defined by

$$G_m = \frac{i_{out}}{v_{id}}$$

(2.2)

where $i_{out}$ is the output current generated by the OTA and $v_{id}$ is the differential input voltage given by $v_{id} = V_{i+} - V_{i-}$ and is assumed to be very small. Typically, the OTA will use output current mirrors that can be $K$ times the width of the input current mirror transistors. By substituting this knowledge into Equation 2.2, the transconductance can be thought of as

$$G_m = Kg_m$$

(2.3)

where $g_m$ is the small-signal transconductance of the differential input transistors (either M1 or M2).

The basic operation of a conventional OTA has been discussed in terms of the open-loop gain. However, current industry designs do not typically implement single-ended OTA designs. Another alternative for OTA design must be considered for allowing operation at low-voltages such as in this research. The following section will cover one such OTA design.

2.2 The Implemented OTA

The operation of the Miller-compensated OTA, shown in Figure 2.3, is similar to that of conventional OTA structures. There are a couple of differences between the conventional OTA and the implemented OTA that are noteworthy. First, the OTA in Figure 2.3 is a fully-differential structure whereas the typical OTA is single-ended. The term “fully-differential” is the relationship of the input signals to the output signals. In other words, a fully-differential (FD) design
amplifies the difference of two input signals and produces \textit{complementary} output signals, $V_{o+} = -V_{o-}$. The FD design is highly desirable for several reasons listed in [8] that include:

1. Since complementary outputs exist, common-mode noise signals are rejected when considering the differential output.

2. The output voltage swing is doubled thus allowing the FD OTA to operate at much lower supply voltages and increase dynamic range by 6dB; a promising trait for this research.

3. Larger output swing can translate into a higher signal-to-noise ratio.

4. Even-order harmonic distortion terms are rejected.

Since this OTA will be connected in a closed-loop feedback form, the idea of compensation must be mentioned. In order to stabilize the OTA under feedback, a compensation scheme must be used to maintain that the output of the OTA does not oscillate. Two measures for the stability of a closed-loop system follow.
directly from the Nyquist stability criterion. The most common metric is known as the *phase margin* (PM), which can be defined as \( PM = 180^\circ + \text{phase at the frequency where the magnitude is 0dB} \). For stability, the phase margin must be greater than 0° and nominally must be in the range \( 45^\circ \leq PM \leq 90^\circ \). Most designers adjust the compensation scheme to realize a PM equal to 60°. A second measure of stability is known as the *gain margin*, which is defined as the reciprocal of the magnitude of the frequency response in decibels at the frequency where the phase is \(-180^\circ\). [8]

The compensation scheme used in the implemented OTA from Fig. 2.3 is known as a Miller-compensated OTA. This refers to the resistors and capacitors located between the drain-gate connection of transistors M6 and M9. For this technique to work, Miller’s Theorem is employed on the \( C_C \) capacitor. Miller’s Theorem allows the admittance in the signal path to be split into two admittances connected at the input and output nodes to AC ground. The new input and output capacitance values are calculated based on the equations shown below. Equation 2.4 is used to calculate the Miller input capacitance given by

\[
C_{MI} = C_C(1 - A_2)
\]

where \( A_2 \) is the second stage gain of the OTA. The Miller output capacitance equation is given by

\[
C_{MO} = C_C \left(1 - \frac{1}{A_2}\right)
\]

The value of \( C_C \) can now be set such that it creates a dominant pole for the OTA. The poles of the OTA in Fig. 2.3 are located at the drains of the input differential pair and the drains of the output shell transistors. In order to maintain stability in closed-loop configurations, the \( C_C \) capacitor is said to separate the poles by a technique known as pole splitting [9]. The stability measures, the phase margin and gain margin of the implemented OTA, will be covered in the following sections.
2.2.1 Common-Mode Feedback

Many different types of fully-differential OTA designs exist but each require additional circuitry compared to the single-ended design. This additional circuit is known as the Common-Mode Feedback (CMFB) circuit. Since the OTA has a differential output, there must be a common reference point for each output. The CMFB circuit attempts to create a common-mode or reference point for the output signals. The CMFB circuit utilized for this design is shown in Figure 2.4.

As with most CMFB designs, the common-mode voltage is created by sampling both output voltages, comparing the average output voltage to the common-mode input voltage, and thus generating a corresponding common-mode output voltage. This common-mode output voltage is then sent to the OTA for biasing. The CMFB circuit shown in Figure 2.4 is based on resistive dividers and a differential amplifier. First, the output voltages are each attached to two resistors each with a value of $R_1$. The $R_1$ resistors are then connected to a resistor $R_2$ to form a voltage divider circuit. The output of the voltage divider is then fed to one of the inputs of the differential amplifier ($M_{11}$). At the same time, an external voltage is placed at the terminal labeled $V_{CM}$. This voltage is then sent through a divider as
well. The purpose of the resistive dividers in the CMFB is to shift voltage levels so that the gates of transistors $M_{17}$ and $M_{18}$ operate close to the lower supply rail, therefore minimizing the supply requirements of the CMFB circuit. The differential pair then performs the subtraction between the common-mode voltage and the output voltage difference and amplifies the resulting voltage. Finally, the resulting common-mode output voltage, $V_{CMO}$, is sent to the gates of $M_7$ and $M_8$. A more detailed analysis of CMFB and related circuitry can be found in §.

2.2.2 Autozeroing Circuitry

For quasi-floating gate transistor circuits, the gates of the differential input transistors are biased using the reverse-biased PN junctions of an NMOS transistor to the value of the negative voltage rail. The QFG transistors allow the amplifier to operate with a much lower power supply. A problem arises for low-voltage QFG designs in the event of mismatch between the input pair. Mismatch typically causes an offset voltage at the input of the OTA. The combination of this offset in addition with the DC biasing and large open-loop gain can cause the OTA to saturate at the output terminals. In order to counteract this undesirable trait, an autozeroing circuit, shown in [10], is required in the OTA design. Presented in Figure 2.5, the autozeroing technique is designed to reduce the offset voltage found at the input of each differential pair. Essentially, the autozeroing (AZ) circuit is used to sample the offset voltage and then to compensate the OTA. Before using the OTA, the switches denoted $SW_A$ and $SW_B$ are closed and the inputs are connected to ground. With no inputs applied, the capacitors, $C_{AZ}$, sample the voltage at each output terminal through a resistive divider that uses equal resistance values, $R_1$. After an amount of time equal to the time constant for the capacitors has elapsed, the switches are opened and the capacitors send the sampled voltages to the input of the differential pair formed by $M_{1B}$ and $M_{2B}$. By designing the widths of $M_{1B}$ and $M_{2B}$ to be twice as large as the input pair formed
by $M_{1A}$ and $M_{2A}$, a current is generated in each branch that is then fed to the drains of $M_{1A}$, $M_{7}$, $M_{2A}$, and $M_{8}$. This compensation current will then adjust the amount of current seen in the input stage and attempt to reduce the unwanted offset voltage. The OTA can be viewed as two separate amplifiers: the main amplifier and the autozeroing amplifier. Each differential pair has an associated offset voltage demonstrated in Figure 2.6. During the autozeroing sample phase
(SW_A and SW_B closed and inputs grounded), the differential output offset voltage can be expressed as

\[ V_{os}^{out} = 2V_{os}^{in}A_{OL} + 2V_{az}^{az}A_{az} \]  \hspace{1cm} (2.6)

where \( V_{os}^{in} \) is the input offset voltage of the \( M_{1A} \) and \( M_{2A} \) pair, \( A_{OL} \) is the OTA open-loop gain (defined later), \( V_{os}^{az} \) is the autozeroing pair offset voltage, and \( A_{az} \) is the autozeroing gain. After the autozeroing capacitances have been charged, the output offset voltage during normal operation can be shown as Equation 2.6 divided by the gain of the autozeroing pair and shown as

\[ V_{os}^{out} = \frac{2V_{os}^{in}A_{OL}}{A_{az}} + 2V_{az}^{az} \]  \hspace{1cm} (2.7)

Thus, the output offset voltage will be comprised of the offset of the AZ amplifier and the amplified then attenuated offset of the input pair. In addition to lowering the offset, another advantage to this approach is the amount of time necessary for operating the AZ circuit. The circuit can be operated for very long periods of time (several seconds) before needing to refresh the AZ capacitors (microseconds), \( C_{AZ} \).

2.3 Characterizing the Implemented Amplifier

It is necessary to discuss the OTA shown in Fig. 2.7 for several different defining characteristics. That is, the FD Miller-compensated OTA must be robust enough to be used in QFG closed-loop amplifier configurations. The characterization parameters that will be discussed are as follows:

1. Open Loop Gain
2. Gain Bandwidth Product
3. Slew Rate
4. Offset Voltage
5. Output Voltage Range

6. Static Power Dissipation

2.3.1 Signal Analysis

Signal analysis is the characterization of a particular circuit from the standpoint of signal performance. The metrics involved are typically the open-loop gain, AC or frequency analysis, Gain-Bandwidth product (GB), and the slew rate (SR). For the FD Miller-compensated OTA in Figure 2.7, the analysis can be done by considering each output separately and then calculating the differential output. For this analysis, consider the OTA separately from the QFG transistors. That is, this section will ignore the capacitive attenuation at the input until later chapters.

2.3.1.1 Open-Loop Gain

In order to understand each characteristic of the implemented OTA, consider the circuit shown in Figure 2.7. The term “open-loop” refers to the fact that
the circuit does not have a negative feedback loop. The analysis for the gain can be found by examining the current in one of the output branches and then doubling this value for the overall differential gain. This is due to the complimentary output signals produced by the fully-differential design. Consider the OTA as two separate gain stages in series. The first gain stage is the gain of the differential amplifier while the second stage is the common source output stage created by transistors $M_4$ and $M_9$. Let us consider the gain for the first stage.

The differential output voltage to input voltage ratio can be expressed as the transconductance of the input pair multiplied by the resistance found at the node between $M_{1-2A}$ and $M_{7-8}$. That is, by grounding the positive input terminal, the gain with respect to the negative input terminal is

$$A_{\text{diff}} = -g_{m1-2A}R_{2A,8}$$

(2.8)

where $A_{\text{diff}}$ is the differential stage gain, $g_{m1-2A}$ is the small-signal transconductance of the input pair, and $R_{2A,8}$ is the resistance at the differential amplifier output node. The resistance $R_{2A,8}$ is given by

$$R_{2A,8} = r_{o2A}||r_{o8}||r_{o1B}$$

(2.9)

where $r_{o2A}$, $r_{o8}$, and $r_{o1B}$ are the output resistances of transistors $M_{2A}$, $M_8$, and $M_{o1B}$, respectively. Thus, by substituting Equation 2.9 into Equation 2.8 and realizing that $g_{m1A} = g_{m2A}$, then $A_{\text{diff}}$ equals

$$A_{\text{diff}} = -g_{m2A} (r_{o2A}||r_{o8}||r_{o1B})$$

(2.10)

The second stage gain of the OTA is the gain of a common-source amplifier. Therefore,

$$A_{cs} = -g_{m9}R_{out}$$

(2.11)

where $g_{m9}$ is the transconductance of transistor M9 and $R_{out}$ is given by

$$R_{out} = r_{o4}||r_{o9}||2R_1$$

(2.12)
where $r_{o4}$ and $r_{o9}$ are the small signal resistance of the transistors M4 and M9, respectively, and $R_1$ is the value of the level-shifting autozeroing resistor used in sampling the output offset voltage.

Finally, the total gain of one output for the OTA is the product of the differential amplifier and the common-source amplifier gains. By substitution,

$$A_{V_{o+}} = g_{m2}A_{m9} (r_{o2A}||r_{o8}||r_{o1B}) (r_{o4}||r_{o9}||2R_1) \tag{2.13}$$

The overall differential open-loop gain is given by

$$A_{OL} = g_{m2}A_{m9} (r_{o2A}||r_{o8}||r_{o1B}) (r_{o4}||r_{o9}||2R_1) \tag{2.14}$$

2.3.1.2 Gain Bandwidth

The Gain-Bandwidth (GB) product defines the maximum frequency range for a particular OTA. The definition of GB is straightforward and can be shown as the product of the bandwidth, or 3-dB frequency, and the open-loop gain of the OTA \[2\]. The open-loop gain has been defined in Equation 2.14. The bandwidth of the OTA is based on the location of the dominant low-frequency pole. The frequency pole locations are found by examining the high impedance nodes of the circuit. For Figure 2.7, the high impedance nodes are located at the input and output nodes and the nodes connecting the input differential pair to the current source load. From a theoretical standpoint, all poles were analyzed and the location of the dominant pole was found. In this case, the dominant pole is found at the drains of the input differential pair due to the Miller effect on the compensation capacitance and assuming the output capacitance is low in comparison. The Miller compensation scheme performs what is known as “pole-splitting.” By utilizing the gain of the second stage, the two poles of the amplifier are split causing one pole to be dominant and occur at a much lower frequency than the output pole. The location of the pole in terms of frequency can be
described as
\[ f_{p1} = \frac{1}{2\pi R_{2A,8}C_{p1}} \]  
(2.15)
where \( R_{2A,8} \) is the parallel equivalent resistance of transistors \( M_{2A} \) and \( M_8 \) and is given by Equation 2.9 and \( C_{p1} \) is the total capacitance at this node. By considering the parasitic and Miller capacitances, the total capacitance can be expressed as
\[ C_{p1} = C_{d2A} + C_{d8} + C_{gd4} + C_{gs9} (C_{gd9} + C_C) (1 + A_{cs}) \]  
(2.16)
The compensation capacitance and the gate-drain capacitance of \( M_9 \) are scaled based on Miller’s Theorem. Equation 2.16 can be approximated by assuming the parasitics are negligible when compared to the Miller capacitances. Therefore, Equation 2.16 can be written as
\[ C_{p1} = (C_{gd9} + C_C) (1 + A_{cs}) \]  
(2.17)
From Equations 2.13 and 2.15, the gain-bandwidth can be expressed as
\[ GB = A_{V_{o+}}f_{p1} \]  
(2.18)
Or, more simply, by substitution,
\[ GB = \frac{g_{m2A}g_{m9} (r_{o4}||r_{o9}||2R_1)}{\pi (C_{gd9} + C_C) (1 + A_{cs})} \]  
(2.19)
2.3.1.3 Slew Rate
Theoretically, slew rate is defined as the maximum change in output voltage for a given time period. The slew rate metric is often written in units of volts per microseconds (V/\( \mu \)s). Like GB analysis, the slew rate analysis is performed at the maximum capacitance node. To calculate the slew rate for the OTA shown in 2.7 refer to the equation below
\[ SR = \frac{I_{D2A}}{C_{p1}} \]  
(2.20)
where \( I_{D2A} \) is the DC biasing current in transistor \( M_{2A} \) and \( C_{p1} \) is the dominant pole capacitance given by Equation 2.16.
2.3.2 DC Analysis

For low-voltage designs, it is extremely important to consider the DC transfer voltage characteristics. Intuition tells us that when reducing the supply voltage, the input voltage range and the output voltage range are also reduced. However, there are a few techniques to limit this effect. As stated before, one of the main advantages of a fully-differential design is the increased output voltage swing. Low-voltage techniques also do not rely on cascoding, or stacking, transistors in the input and output stages, which causes a reduction in signal swing. One of the advantages for a low-voltage design is the fact that by reducing the supply voltage and keeping the bias current fixed, the static power dissipation is therefore reduced. These items will be evident in the following sections.

2.3.2.1 Offset Voltage

It is especially important in this research to consider the offset voltage of the OTA. A large offset voltage, in addition to the QFG biasing design, can cause the OTA output to saturate. As discussed before, the autozeroing circuitry is intended to reduce this offset but characterizing this behavior is still of interest. The offset voltage can be placed in one of two categories: systematic offset and random offset.

Random offset occurs by nature of the physical transistor differences. This is usually evident in transistor mismatch, threshold voltage variations, and process variations. In many cases, the random offset effects can be somewhat subsided by employing matching techniques during the layout of differential amplifiers.

Systematic offset voltage typically are related to the design itself. In some cases, the systematic offset is created by a mismatch in biasing currents or a poorly designed CMFB circuit. In addition, systematic offsets arise from a poorly controlled output voltage potential.
2.3.2.2 Output Voltage Range

Due to the low-voltage supply requirements, the output voltage range can become severely limited for the OTA. Thus, it is recommended that the design not use cascoded output transistors for boosting the open-loop gain. This allows the single-ended output at either $V_{o+}$ or $V_{o-}$ to be limited by the drain-source voltage of the output transistors. Consider the positive output voltage and refer to Figure 2.8 such that the maximum output voltage can be expressed as

$$V_{\text{max}} = V_{DD} - V_{\text{sat}_{SD,M4}}$$

(2.21)

where $V_{\text{sat}_{SD,M4}}$ is the drain-source saturation voltage of transistor M4. The minimum output voltage is

$$V_{\text{min}} = V_{SS} + V_{\text{sat}_{DS,M9}}$$

(2.22)

where $V_{\text{sat}_{DS,M9}}$ is, again, the drain-source saturation voltage of transistor M9. Thus,

![Figure 2.8: OTA Positive Output Stage](image)

for the single-ended output, the output voltage range is within the power rails plus or minus the saturation voltage for each output transistor. As mentioned before,
the fully-differential design has an advantage when considering the maximum output swing. For a fully-differential OTA, let $V_{o+} = V_{max}$ and the negative output voltage is $V_{min}$ and the output swing is therefore $V_{max} - V_{min}$ for $V_{o+}$. By utilizing the differential output voltage, the total peak-to-peak swing is now $2(V_{max} - V_{min})$ or essentially twice that of a single-ended design.

2.3.2.3 Static Power Dissipation

Typically, lowering the voltage supply in analog IC designs causes the designer to use more current. By inspection, this reduces the effectiveness of the circuitry for low-power applications. In order to maintain the robust nature of a low-voltage circuit, the biasing current must be kept at a low level as well. The static power dissipation characteristic is used to determine the effectiveness of the circuitry while idling. This can be expressed as the difference between the supply rails multiplied by the sum of the static current in each branch of the OTA.

$$P = (V_{DD} - V_{SS})(I_{M1} + I_{M2} + I_{M3} + I_{M4} + I_{M5} + I_{10})$$  \hspace{1cm} (2.23)

The total static power dissipated can be represented in terms of the biasing current, $I_{bias}$.

$$P = (V_{DD} - V_{SS})(3 + 2K)I_{bias}$$  \hspace{1cm} (2.24)

Since the gain-bandwidth and slew rate are directly proportional to the biasing current, a tradeoff occurs when lowering the biasing current for conservation of static power dissipation. This means that lowering the current will decrease the static power dissipation and will lower the GB and SR. A more detailed analysis of the power dissipation will be shown in a later section.

2.4 OTA Analysis

The characteristics discussed in the previous sections will be presented here in terms of the designed and implemented OTA shown in Figure 2.7 The nature of
this paper is not, however, to discuss the advantages and disadvantages of the OTA as the primary subject. Instead, this paper is more concerned with presenting quasi-floating gate transistors for use in low-voltage designs. Therefore, the OTA characterization will only be shown from theoretical and simulation standpoints.

2.4.1 OTA Design

The OTA transistors were chosen based upon an assumed drain-source saturation voltage drop \( V_{DS}^{sat} \), the technology given threshold voltages, and a chosen biasing current. The design characteristics are summarized in Table 2.1.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>AMI 0.5µm CMOS</td>
</tr>
<tr>
<td>Threshold Voltages ( V_{THN}, V_{THP} )</td>
<td>0.7V, 0.95V</td>
</tr>
<tr>
<td>Transconductance ( KP_N, KP_P )</td>
<td>( 120\mu A/V^2, 40\mu A/V^2 )</td>
</tr>
<tr>
<td>Power Supply ( V_{DD}, V_{SS} )</td>
<td>1.5V, 0V</td>
</tr>
<tr>
<td>CMFB Ref ( V_{cm} )</td>
<td>750mV</td>
</tr>
<tr>
<td>Bias Current ( I_{bias} )</td>
<td>20µA</td>
</tr>
</tbody>
</table>

Table 2.1: OTA Design Specifications

course, each of the circuit structures presented in the latter chapters require added specifications. The basic request is high-speed operation as well as a relatively high gain while maintaining stability. Thus, once the transistors were sized, some tweaking of those sizes must be done in order to maintain the computational accuracy needed in each of the proposed applications. Compensation capacitors and compensation resistors were sized based on a trial-and-error procedure shown in [11]. Autozeroing resistors and capacitors were sized based on techniques listed in [10]. Transistor sizes, resistor values, and capacitor values are shown in Table 2.2 and the location of each element is shown in Figures 2.7 and 2.4. Each transistor was designed based on the assumed bias current and saturation voltage level as
well as the technology driven threshold voltages. Of particular interest is the connection for the bulk terminals for the three differential pairs. Normally, it is acceptable to tie all bulk terminals to their respective voltage rails, i.e., \( V_{DD} \) for PMOS. However, for the transistors in each differential pair, this leads to a phenomenon known as the “body effect,” which causes the threshold voltage to increase. This is a disadvantage when considering low-voltage designs, thus, the differential pair bulk terminals were connected to the source terminals of their respective transistors and therefore eliminated the body effect. Design calculations for transistor sizing are shown in Appendix A.

### 2.4.2 Results

The results presented within this section are shown in terms of the theoretical and simulation analysis levels. All simulation analysis was performed in the Cadence Analog Design Environment using the IC Front to Back design suite under license of the Cadence University Program at New Mexico State University. Each simulation used the Cadence NCSU kit and BSIM3v3 MOSFET models for the 0.5\( \mu \)m AMI Analog CMOS process. Theoretical analysis calculations can be found in Appendix B.
2.4.2.1 Open-Loop Gain

The open-loop gain for this design is somewhat less than desirable than for typical OTA implementations. However, the structure and accuracy of the circuit topologies to be discussed in the latter chapters does not require that the open-loop gain be greater than what is shown. Figure 2.9 shows the AC setup for testing the OTA in simulation. Figure 2.10 shows the simulation output for an AC sweep given the setup shown in Fig. 2.9. Using a bias current of 20\mu A and a 1.5V total power supply and common-mode reference voltage of 0.75V, the open-loop gain is approximately 40dB. From a theoretical standpoint, the open-loop gain is 47dB. Typically, these values are compared in units of V/V instead of decibels. Therefore, the corresponding gain values are 100V/V for simulation, 224V/V for theory, and a percentage error of -55%.

2.4.2.2 Gain Bandwidth

As described in the earlier section, the Gain-Bandwidth (GB) can be calculated based on the product of the dominant pole and the open-loop gain. The GB frequency value occurs when the decibel magnitude reaches unity. This measurement can be made using the same simulation setup as shown in Fig. 2.9. By using...
the same biasing setup (20µA and 1.5V supply), the GB was found in simulation to be 27.381MHz whereas theoretical analysis shows a GB of 31.2MHz.

2.4.2.3 Slew Rate

Slew rate for the OTA determines the maximum speed the OTA can operate given a capacitive load and maximum output current. Using a compensation capacitance of 0.75pF and a biasing current of 20µA, the slew rate is determined using the setup shown in Figure 2.11. Using an input pulse, the slew rate is determined by finding the amount of time needed to transition from 10% of the
differential output to 90%. The slew rate simulation analysis points to a value of

$$1.278V/\mu s$$ and theoretical calculations list a value of $$1.059V/\mu s$$. This is a noticeable trait in that the slew rate can determine the transition speed of the OTA. Typical designs at higher voltage yield values roughly five times that of the low-voltage OTA implemented here. However, as stated earlier, the purpose of this paper is not to develop an extremely high-speed OTA but to rather demonstrate the amazing low-voltage capabilities introduced by the QFG transistors.

2.4.2.4 Stability

The stability is determined based on a simulation standpoint only. Two of the defining metrics of stability are discussed in Section 2.2. The phase margin and gain margin stability criterion were determined using the setup in Figure 2.9. In terms of the phase margin, as long as the value is positive, the OTA is stable. However, designers attempt to compensate the OTA such that the phase margin is between 45° and 90°, where 60° is ideal. By using a compensation capacitance of 5pF and a compensation resistance of 1kΩ, the phase and gain margins were
found using the simulation setup in Fig. 2.9. By assuming this design will have a rather small capacitive load, on the order of $1\text{pF}$, the phase margin was found from simulation as $62.0447^\circ$ and the gain margin was found to be $24.0851\text{dB}$.

### 2.4.2.5 Output Voltage Range

The output voltage range equation was found earlier in Equation 2.21 and Equation 2.22. Using these two equations, the range was found to be within each voltage rail by the value of the drain-source saturation voltage. Theoretical calculations show an output voltage range of $1.1\text{V}$ and simulation results show a value of roughly $1.098\text{V}$.

### 2.4.2.6 Offset Voltage

The offset voltage characteristics of the amplifier are somewhat dictated by the effectiveness of the autozeroing circuit. In some cases, the simulator can predict a small portion of the offset voltage but a true measure of offset analysis is to add an offset voltage to the input pair of the main amplifier and autozeroing amplifier and demonstrate the effectiveness of the autozeroing circuit. This can be done by applying a small input offset voltage and simulating the amplifier in an open-loop configuration. As discussed in the autozeroing section, the output offset voltage will be comprised of the input offset voltage of the amplifier multiplied by the open-loop gain and attenuated by the autozeroing amplifier gain. The second offset component comes from the product of the autozeroing pair offset voltage with the AZ gain. By setting both input offset voltages to $10\text{mV}$ each, transient analysis indicates a differential output offset voltage of $52.93\text{mV}$ when the AZ is active.
2.4.2.7 Static Power Dissipation

Static power dissipation is a vital performance criterion for low-voltage designs. Typically, when lowering the supply voltage for analog circuits, designers must resort to increasing the biasing current to maintain the same performance. The static power dissipation for the implemented OTA is roughly 0.81mW in theory and 0.7977mW from simulation.

2.4.2.8 Implemented Silicon Area

It is always necessary with any type of design to consider the amount of silicon area required. The semiconductor industry considers silicon “real estate” as the most expensive real estate in the world. Thus, the layout must be very compact to be robust for mixed-signal applications. Figure 2.12 shows the layout for the implemented OTA in 0.5µm AMI process. The large capacitor array shown on the right in Fig. 2.12 comprise the autozeroing capacitors, $C_{AZ}$.

Figure 2.12: OTA Layout 96729.36 $\mu m^2$ (478.65 $\mu m$ x 206.4 $\mu m$)
2.4.2.9 OTA Results Summary

The theoretical and simulation results for the characterization of the implemented transconductance amplifier are shown in Table 2.3. The final column lists the percentage error between the calculated and simulated values. Theoretical analysis of the OTA is shown in Appendix B. In order to maintain a somewhat high level of accuracy, the values for small-signal transconductance, current, and small-signal resistance were found using an operating point analysis in simulation. This allowed the comparison of the characteristics to be based more on the theoretical equations rather than the constant inputs. The major source of error for the OTA analysis occurs for the open-loop gain calculation of the OTA. Since the simulation results indicate a gain of roughly 40dB, the OTA will not perform with the same accuracy in closed-loop amplifier form as current industry designs that have a minimum gain of 60dB. This is evident in the next chapter regarding the programmable gain amplifier.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Theory</th>
<th>Sim</th>
<th>% Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>$A_{OL}$ (dB)</td>
<td>47.026</td>
<td>40.0237</td>
<td>-55.35%</td>
</tr>
<tr>
<td>GB (MHz)</td>
<td>32.1</td>
<td>27.38</td>
<td>-12.25%</td>
</tr>
<tr>
<td>SR (V/µs)</td>
<td>1.059</td>
<td>1.278</td>
<td>20.67%</td>
</tr>
<tr>
<td>Offset (mV)</td>
<td>42</td>
<td>52.93</td>
<td>26.02%</td>
</tr>
<tr>
<td>Out Range (V)</td>
<td>1.1</td>
<td>1.098</td>
<td>-0.18%</td>
</tr>
<tr>
<td>Static Power (mW)</td>
<td>0.81</td>
<td>0.7977</td>
<td>-1.52%</td>
</tr>
<tr>
<td>PM</td>
<td>–</td>
<td>62.04°</td>
<td>–</td>
</tr>
<tr>
<td>GM (dB)</td>
<td>–</td>
<td>24.08</td>
<td>–</td>
</tr>
</tbody>
</table>

Table 2.3: OTA Characterization Results


3 PROGRAMMABLE GAIN AMPLIFIER

3.1 Introduction

One of the most common structures in analog and mixed-signal designs is the amplifier. Amplifiers are used for many applications including filters and data converters. From cellular phones to portable CD players, analog signal amplifiers are an integral part of every day battery powered electronics. Thus, a low-voltage amplifier is very important. Particularly, an amplifier with programmable gain realizes a much more robust design. This chapter will discuss in theoretical, simulation, and experimental detail a low-voltage, closed-loop, programmable-gain, inverting amplifier known in this chapter by the acronym PGA.

3.2 Operation

The schematic of the programmable gain inverting amplifier is shown in Figure 3.1. Using the switches denoted SW₁, SW₂, SW₃, or SW₄, a gain of 1, 2, 4, or 8 can be selected, respectively. Since the feedback elements are capacitors, the operation of the amplifier is based on charge transfer. The net differential input charge can be expressed as

\[ Q_{in} = kCV_{in} \]  \hspace{1cm} (3.1)

where k is 1, 2, 4, or 8 depending on the switch selection, C is the unit capacitance, and \( V_{in} \) is the differential input voltage. Thus, the net output charge becomes

\[ Q_{out} = -kCV_{in} \]  \hspace{1cm} (3.2)

leading to a net output voltage of

\[ V_{out} = \frac{Q_{out}}{C} = -kV_{in} \]  \hspace{1cm} (3.3)

and the voltage gain is \(-k\).
3.2.1 Gain Analysis

The PGA is known as a closed-loop amplifier because of the negative feedback loops provided by the feedback capacitors. In order to obtain an appropriate gain response, the analysis of closed-loop amplifiers is as follows. By analyzing the input capacitor to output capacitor ratio, the gain can be determined as discussed in the previous section. However, feedback amplifier gains are best described by the equation below.

$$A_{CL} = \frac{A_{OL}}{1 + \beta A_{OL}}$$  \hspace{1cm} (3.4)
where $A_{OL}$ is the open-loop gain of the OTA and $\beta$ is the ratio of the feedback element to the feed-forward element. The actual closed-loop gain for the PGA can be found by using the gain for the OTA and Equation 3.4. Typically, a designer will choose/design an OTA with a high gain such that the closed-loop gain is approximately $\frac{1}{\beta}$. Thus, a gain of 1000 V/V (60dB) with a unity-gain feedback would realize an error of -0.1%. By using an amplifier with less than 1000 V/V, the accuracy decreases much more rapidly as the feedback increases. Table 3.1 lists the actual closed-loop gain of the PGA found using an open-loop gain of 100.31 V/V (40.0273dB) found from simulation in Section 2.4.2.1.

<table>
<thead>
<tr>
<th>Ideal Gain (V/V)</th>
<th>Actual Gain (V/V)</th>
<th>Error (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.99</td>
<td>-0.987</td>
</tr>
<tr>
<td>2</td>
<td>1.961</td>
<td>-1.955</td>
</tr>
<tr>
<td>4</td>
<td>3.847</td>
<td>-3.835</td>
</tr>
<tr>
<td>8</td>
<td>7.409</td>
<td>-7.386</td>
</tr>
</tbody>
</table>

Table 3.1: PGA Closed-Loop Gain Analysis

3.2.2 Frequency Response

Due to the structure of the quasi-floating gate input and capacitive dividers, the overall frequency response of the PGA becomes a bandpass filter. The operating frequency range, in large part, can be determined by the time constants associated with each capacitor in the programmable gain amplifier. From Chapter 2, it is apparent that the OTA has a two pole transfer function and lowpass filter response. However, the programmable gain inverting amplifier configuration shown in Figure 3.1 creates a pole at the input of the OTA. When a particular gain is selected, the resistance associated with each capacitor can be determined using the channel resistance of the selection switches and plus the resistance of the QFG transistors. In order to determine the overall response, the dominant poles of the design will control its frequency dependent nature. Due to the extremely
high resistance of the QFG transistors, the highpass pole is found from the input capacitance in combination with the QFG transistor resistance (typically in GΩ), which will dominate the resistance calculation. Equation 3.5 describes the approach necessary for determining the frequency response at the highpass end.

\[ f_{hp} = \frac{1}{2\pi R_{\text{leak}} C_T} \]  

(3.5)

where \( R_{\text{leak}} \) is the QFG leakage resistance and \( C_T \) is the total capacitance composed of the input capacitance and some parasitic capacitances. The frequency response for each gain selection is listed in Table 3.2. The highpass cutoff frequency is listed as \( f_0 \) and the lowpass cutoff frequency is listed as \( f_1 \). Calculation of the lowpass pole for each gain selection is based on a technique known as bandwidth extension [2]. The negative feedback increases the usable bandwidth of the amplifier based on the equation below.

\[ f_{FB} = f_{3\text{dB}} (1 + A_{OL}\beta) \]  

(3.6)

where the \( f_{FB} \) is the feedback extended frequency, \( f_{3\text{dB}} \) is the OTA 3dB cutoff frequency, \( A_{OL} \) is the OTA open-loop gain, and \( \beta \) is the feedback ratio discussed in the previous section (\( \beta = \frac{1}{8} \) for a gain selection of 8). The QFG implementation has a slight disadvantage when compared to the multiple input floating-gate design in terms of frequency response. For the “full” floating-gate structure, the input capacitors are able to hold a DC signal instead of blocking DC signals. This is because the input capacitors do not have a discharge path for the charge being

<table>
<thead>
<tr>
<th>Gain (V/V)</th>
<th>( f_0 ) (Hz)</th>
<th>( f_1 ) (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>35.81</td>
<td>28.15</td>
</tr>
<tr>
<td>2</td>
<td>17.905</td>
<td>14.22</td>
</tr>
<tr>
<td>4</td>
<td>8.952</td>
<td>7.247</td>
</tr>
<tr>
<td>8</td>
<td>4.476</td>
<td>3.762</td>
</tr>
</tbody>
</table>

Table 3.2: Programmable Gain Amplifier Frequency Response


stored. However, as discussed earlier, the quasi-floating gate implementation creates a highpass filter at the input. The QFG biasing transistor creates a very large resistance at the input node. This, in addition to the input capacitors, creates a highpass response that tends to block true DC signals.

3.2.3 Harmonic Distortion

Gain analysis and frequency response are important characteristics of an amplifier but another defining metric is also used. Harmonic distortion is a common method of describing the nonlinearity of an amplifier [8]. Specifically, harmonic distortion is measured by applying a sinusoidal signal to the input of the amplifier. Let us consider an input signal defined by

\[ V_i = V_m \sin(w_o t) \] (3.7)

where \( A \) is the amplitude and \( w_o \) is the fundamental frequency. The single-ended output voltage of the amplifier can be expressed as

\[
V_o = a_1V_m \sin(w_o t) + a_2V_m^2 \sin^2(w_o t) + a_3V_m^3 \sin^3(w_o t) + \ldots \\
V_o = a_1V_m \sin(w_o t) + \frac{a_2V_m^2}{2}(1 - \cos(2w_o t)) + \\
\frac{a_3V_m^3}{4}(3\sin(w_o t) - \sin(3w_o t)) + \ldots 
\] (3.8)

where \( a_n \) are the distortion amplitude coefficients. It is evident from Equation 3.8 that the output signal contains second, third, and higher order harmonics. For a more detailed analysis of the distortion coefficients, see [8]. In most cases, the harmonic distortion is referred to as the total harmonic distortion (THD). The THD is calculated as the rms value of the harmonic components of the output signal, excluding the fundamental, expressed as a percentage of the rms of the fundamental [9]. As stated in Section 2.2, a fully-differential design has an advantage over single-ended designs when considering nonlinearity due to harmonic distortion. The advantage is that the fully-differential design rejects even order harmonics.
3.3 Simulation Results

All simulations for this design were performed in the Cadence Affirma Analog Environment using the SpectreS SPICE simulator. MOSIS BSIM3v3 models for the 0.5µm CMOS process were used for the transistor models realizing a threshold voltage of approximately 0.7V and 0.95V for the NMOS and PMOS transistors, respectively. The positive supply voltage, $V_{DD}$, was set to 1.5V, the negative supply voltage, $V_{SS}$, was set to zero, and the common-mode voltage was set to 0.75V.

3.3.1 Gain Analysis

For this design, a unit capacitance of 1pF was used. For an accurate gain analysis under ideal conditions, the input offset and autozeroing pair offset voltages were set to 0V. Since the OTA has a relatively low finite gain, as discussed earlier, the output differential voltage is somewhat less than the desired. Figure 3.2 shows the output sinusoid for each gain selection as the result of a 1kHz, 100mV amplitude input signal. Simulation results indicate gains listed in Table 3.3.

<table>
<thead>
<tr>
<th>Theoretical Gain (V/V)</th>
<th>Sim Gain (V/V)</th>
<th>Error (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.99</td>
<td>0.971</td>
<td>-1.943</td>
</tr>
<tr>
<td>1.961</td>
<td>1.923</td>
<td>-1.927</td>
</tr>
<tr>
<td>3.847</td>
<td>3.773</td>
<td>-1.901</td>
</tr>
<tr>
<td>7.409</td>
<td>7.268</td>
<td>-1.905</td>
</tr>
</tbody>
</table>

Table 3.3: PGA Simulation Gain Analysis

Each of the gain values were calculated based on the ratio of the peak-to-peak voltage of the output sinusoid with respect to the peak-to-peak voltage of the input sinusoid.
3.3.2 Frequency Response

The evaluation of the frequency response of the programmable gain, inverting amplifier was performed using an AC input signal with amplitude of 1 and phase of 0 degrees connected to the amplifier with a 1pF load capacitance. A frequency sweep was performed on the AC source to determine the overall transfer function for each gain selection. The magnitude (dB) and phase (deg) were graphed and the frequency range of the OTA was determined. The frequency range was determined by the 3dB corner frequencies associated with the magnitude plot for each gain selection. Table 3.4 summarizes the results found during simulation.
<table>
<thead>
<tr>
<th>Gain (V/V)</th>
<th>$f_0$ (mHz)</th>
<th>$f_1$ (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>560</td>
<td>10.035</td>
</tr>
<tr>
<td>2</td>
<td>661.1</td>
<td>6.005</td>
</tr>
<tr>
<td>4</td>
<td>698.6</td>
<td>3.353</td>
</tr>
<tr>
<td>8</td>
<td>715.7</td>
<td>1.824</td>
</tr>
</tbody>
</table>

Table 3.4: PGA Simulation Frequency Response

3.3.3 Harmonic Distortion

From a simulation point of view, harmonic distortion measurements were made using Cadence Affirma Analog Design Environment’s Calculator tool. By using a 1kHz sinusoidal source with varying amplitude, the circuit was simulated for 10ms. The second through tenth harmonics were computed as well as the total harmonic distortion. Table 3.5 lists the second, third, and fourth harmonic distortion levels in decibels as well as the total harmonic distortion (%) for each amplitude chosen for each gain selection. In each case, the simulations were performed with a zero-Volt offset as in the gain analysis simulations. Input amplitudes of 100mV to 300mV were used for gain selections of 1 and 2 whereas amplitude values reaching a maximum of 125mV were used for gains of 4 and 8.

<table>
<thead>
<tr>
<th>PGA Harmonic Distortion (dB) and THD (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1kHz</td>
</tr>
<tr>
<td>Amp</td>
</tr>
<tr>
<td>100mV</td>
</tr>
<tr>
<td>200mV</td>
</tr>
<tr>
<td>300mV</td>
</tr>
</tbody>
</table>

| 1kHz | Gain Selection = 4 | Gain Selection = 8 |
| Amp  | 2nd  | 3rd  | 4th  | THD  | 2nd  | 3rd  | 4th  | THD  |
| 50mV | -109.3 | -89.8 | -117.2 | 0.00326 | -110.2 | -74.42 | -120.3 | 0.019 |
| 100mV| -100.1 | -77.74 | -112.2 | 0.013 | -98.94 | -60.47 | -112.3 | 0.095 |
| 125mV| -95.85 | -73.54 | -108.5 | 0.0211 | -94.88 | -54.32 | -107.7 | 0.194 |

Table 3.5: PGA Simulation Harmonic Distortion
This is due to the low-voltage operation of the amplifier. Input signals that are much higher than 125mV for the gain selection of 8 realize a closed-loop gain that is greater than 10% in error from ideal simulations because the output is limited by the supply voltage. It is apparent that for lower input voltage amplitudes, the harmonic distortion levels are low. A noteworthy response to increasing gain selections shows a decrease in harmonic distortion.

3.3.4 Implemented Silicon Area

As always, silicon area is an important metric to use when considering an integrated circuit design. Using the OTA layout shown in Figure 2.12 the PGA layout is shown below in Figure 3.3. The feedback and feed-forward capacitors were constructed using a 250fF unit capacitance. Each switch was built using 15µm PMOS widths, 7.5µm NMOS widths, and lengths of 1µm. The sizes of the QFG biasing transistors are 120µm in width and 1µm in length. The overall area of the programmable gain amplifier is 0.191mm².

![PGA Layout](image)

Figure 3.3: PGA Layout 191340.45 µm² (479.55µm x 399µm)
3.4 Experimental Results

The programmable gain closed-loop amplifier configuration shown in Fig. 3.1 was fabricated in the AMI 0.5\(\mu\)m CMOS process. Sizes for the OTA and QFG transistors are listed in Table 2.2. The circuit was packaged in a 40 pin DIP chip by MOSIS. The chip was connected to a standard breadboard in the laboratory. The setup for the amplifier is listed in Table 3.6. In order to realize complimentary input signals, the signal from the function generator was inverted using a unity-gain analog inverting amplifier built using an Intersil CA3280 and equal value resistors. The CA3280 ICs contain two 9MHz bandwidth BJT-based OTAs, which is useful as a multiplier, comparator, function generator, etc. The output signals were subtracted by constructing two buffers, each connected to one of the differential outputs, then fed serially to a difference amplifier. The difference amplifier and buffers were built using two CA3280 ICs.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Supply (V_{DD}, V_{SS})</td>
<td>1.5V, 0V</td>
</tr>
<tr>
<td>Common-mode Voltage (V_{cm})</td>
<td>750mV</td>
</tr>
<tr>
<td>Bias Current (I_{bias})</td>
<td>20(\mu)A</td>
</tr>
</tbody>
</table>

Table 3.6: PGA Simulation & Experimental Setup

3.4.1 Gain Analysis

Gain analysis at 1kHz and 100mV input was performed on the setup listed above. The output signals were viewed on an oscilloscope and the gain measured using a digital multimeter. Results indicate a similar response seen in simulation. That is, the gain is slightly less than desirable due to the finite gain of the OTA used to construct the programmable gain amplifier. In this case, experiments show gains listed in Table 3.7. Each gain is compared using percentage error analysis to the actual closed-loop gain found in Table 3.1.
### Table 3.7: PGA Experimental Gain Analysis

<table>
<thead>
<tr>
<th>Theoretical Gain (V/V)</th>
<th>Experimental Gain (V/V)</th>
<th>Error (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.99</td>
<td>0.991</td>
<td>0.117</td>
</tr>
<tr>
<td>1.961</td>
<td>1.978</td>
<td>0.879</td>
</tr>
<tr>
<td>3.847</td>
<td>3.923</td>
<td>1.989</td>
</tr>
<tr>
<td>7.409</td>
<td>7.777</td>
<td>4.962</td>
</tr>
</tbody>
</table>

### 3.4.2 Frequency Response

Using an HP 4195A Network Analyzer, the programmable gain amplifier was tested in the laboratory for bandwidth. As stated in the operation section, the frequency response should resemble that of a bandpass filter. The frequencies listed below in Table 3.8 were found experimentally. Due to the frequency limitations of the 4195A analyzer, the low frequency cutoff value was found using an HP digital multimeter and HP function generator. The frequency range for a sine wave output from the HP 33120A Function generator is from 100µHz to 15MHz and the measurement accuracy of the HP 34401A digital multimeter is rated as plus or minus one percent for frequencies ranging between 3Hz and 5Hz. Thus, the low frequency results may not be as accurate due to the limitations of the DMM.

### Table 3.8: PGA Experimental Frequency Response

<table>
<thead>
<tr>
<th>Gain (V/V)</th>
<th>$f_0$ (Hz)</th>
<th>$f_1$ (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1.8</td>
<td>3.994</td>
</tr>
<tr>
<td>2</td>
<td>1.7</td>
<td>2.944</td>
</tr>
<tr>
<td>4</td>
<td>1.6</td>
<td>1.968</td>
</tr>
<tr>
<td>8</td>
<td>1.6</td>
<td>1.178</td>
</tr>
</tbody>
</table>
3.4.3 Harmonic Distortion

Distortion analysis was performed in the laboratory using an HP 4195A Network/Spectrum Analyzer and the fabricated circuit setup listed above. By utilizing the Spectrum configuration feature on the analyzer, experiments were done that yielded results for the second, third, and fourth order harmonics. As stated previously, one of the main advantages in a fully-differential design are the elimination of even-order harmonics. Therefore, it stands to reason that the third order harmonic should have a larger value than that of the second and fourth. Results for the experimental harmonic distortion are shown in Figure 3.4. The fundamental input signal was a 400mV peak-to-peak sinusoid with frequency of 10kHz. Analysis indicates a THD of roughly 1% with this fundamental.

Figure 3.4: PGA Experimental Harmonic Distortion for 10kHz, 400mVpp input: $\text{THD} = 1\%$
3.5 Summary

It is apparent that the gain analysis for the amplifier is somewhat lacking when comparing the theoretical operation to that of the simulation or the experiment. This is in large part due to the finite open-loop gain of the OTA that was implemented. Upon further inspection, if the gain of the amplifier were increased, the programmable gain closed-loop amplifier configuration would yield substantially better results. Table 3.9 lists the results comparisons for the amplifier for each gain selected. Future research is necessary to realize an industry worthy programmable gain amplifier configuration using a higher open-loop gain OTA.

<table>
<thead>
<tr>
<th>Gain (V/V)</th>
<th>( f_1 ) (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Theory</td>
<td>Sim.</td>
</tr>
<tr>
<td>0.99</td>
<td>0.965</td>
</tr>
<tr>
<td>1.961</td>
<td>1.917</td>
</tr>
<tr>
<td>3.847</td>
<td>3.768</td>
</tr>
<tr>
<td>7.409</td>
<td>7.245</td>
</tr>
</tbody>
</table>

Table 3.9: Programmable Gain Amplifier Results
4 SAMPLE AND HOLD

4.1 Introduction

Quasi-Floating Gate transistors are also particularly well suited to applications of a discrete time nature. The Sample and Hold circuitry presented in this Chapter will prove the low-voltage operation of a very simple discrete-time application.

4.2 Operation

The operation of the sample and hold circuit in Figure 4.1 is very basic. After the period of time required for the autozeroing circuit in the OTA, the input sampling switches, denoted $SW_1$, are closed allowing the input signal to charge
the storage capacitors. Based on the set sampling frequency, the switches are then opened such that the capacitors “hold” the values stored.

Discrete-time circuitry operates on the principle of sampling. According to [2], Nyquist developed an equation that governs the minimum sampling rate given a particular bandwidth-limited input signal. In other words,

\[ f_s \geq 2f_o \]  

(4.1)

where \( f_o \) is the input signal frequency and \( f_s \) is the sampling frequency. In the case that the sampling frequency is less than twice the signal frequency, a phenomenon known as aliasing occurs. The term aliasing refers to the fact that the reconstructed signal from the sample output can take on “aliases,” or different forms, of the original input signal. This can best be described by considering the frequency domain representation of the input signal. Figure 4.2 shows the frequency domain response of a given input signal. The input signal, sampling function, and overall output signals are shown in Fig. 4.2(a), (b), and (c), respectively. By sampling too low, the output waveforms begin to overlap each other as shown in Fig. 4.2(d). In terms of the frequency domain, this is aliasing. Aliasing can be eliminated by a number of methods, the simplest of which is to increase the sampling frequency. But, this solution does not reject wide band noise. A second popular method is to filter the input signal for frequencies greater than one-half of the sampling frequency. Known as an anti-aliasing filter, this tends to add delay so the best option is to use a combination of the two. For this research, the goal is to prove the low-voltage operation of a S/H circuit and not to build one that has the features of filtering. The S/H in this chapter was primarily sampled at 5 times that of the input frequency allowing for easy visualization and error analysis of the output signal.
4.2.1 Frequency Response

As with the programmable gain amplifier, the S/H circuit behaves as a bandpass filter with respect to the input frequency. Although the sample and hold is a discrete-time application, it is important to calculate the minimum and maximum frequencies the device can pass as an input. This means that the sampling switches are left closed and the frequency response is determined for the resulting unity-gain negative feedback amplifier. Due to the high resistance of the QFG transistors (GΩ), the low frequency pole creates a high pass filter in the millihertz to low Hertz range. This is given by the equation

$$f_{hp} = \frac{1}{2\pi R_{\text{leak}} C_T} \quad (4.2)$$
where $R_{\text{leak}}$ is the QFG leakage resistance and $C_T$ is the total input capacitance composed of the sampling capacitance and some parasitic capacitance terms. Analysis of Equation 4.2 using a leakage resistance of 4.44GΩ and total capacitance of 5pF, gives a highpass pole equal to 7.162Hz.

On the high end of the frequency range, the OTA creates a lowpass filter with cutoff found in the low megahertz range. Just as with the PGA, the dominant pole of the OTA is extended by the equation

$$f_{FB} = f_{3dB}(1 + A_{OL}\beta)$$  \hspace{1cm} (4.3)

where the $f_{FB}$ is the feedback extended frequency, $f_{3dB}$ is the OTA 3dB cutoff frequency, $A_{OL}$ is the OTA open-loop gain, and $\beta$ is the feedback ratio and in this case equal to 1. Using Equation 4.3 with an open-loop gain of 100.32V/V and $f_{3dB}$ frequency equal to 277.9kHz, the lowpass pole is found to be 28.15MHz.

4.2.2 S/H Error Analysis

Characterizing the sample and hold circuit is based in many ways on the speed of the input signal, speed of the sampling clock, and accuracy. Each of the metrics listed below are used in determining the robustness of the design. In most cases, the abilities of the S/H are based almost entirely on the amplifier chosen. Figure 4.3 below illustrates the errors commonly found when analyzing a sample and hold circuit.

4.2.2.1 Sample Mode

The sample mode is the amount of time when the sampling switches are closed and the input signal charges the hold capacitors. The amount of time necessary for the S/H to track the signal to a specified tolerance is known as acquisition time. This can be found by analyzing the worst case acquisition time that occurs when the analog signal varies from zero volts to its maximum value.
Once the signal is acquired, the stability and speed of the amplifier are considered. As with control theory, the overshoot is the maximum amplitude the held value reaches when the sampling clock goes to a high state. Overshoot typically occurs when the OTA, or Opamp, used is not compensated well enough which, in turn, yields a low phase margin value. Overshoot error can be attributed to the stability of the amplifier used. Similarly, settling time can also be attributed to the OTA chosen. If the OTA is slightly unstable, this will be apparent when considering the output of the S/H. Basically, the settling time is the amount of time necessary for the sampled voltage to "settle" to a steady-state voltage within a certain tolerance.

4.2.2.2 Hold Mode

Hold mode is the time at which the sampling switches are opened and the capacitors attempt to hold the value stored from the input signal. Droop, or leakage, occurs during the hold phase of the S/H circuit. The output voltage level during the hold phase should remain constant. However, due to diode leakage, the voltage will drift. The amount of voltage loss from the initial voltage level is
called droop. One cure for reducing the effects of droop is to increase the size of the hold capacitor. However, this leads to increased time to charge the hold capacitor. Some accuracy errors can also occur as the result of charge injection or clock feedthrough. This is otherwise known as pedestal error. This occurs when part of the charge built in the channel of the switch is sent to the hold capacitor. In turn, this charge injection causes the voltage on the capacitor to increase.

4.3 Simulation Results

All simulations for the sample and hold circuit were performed in the Cadence Affirma Analog Design Environment. Each MOSFET in the design uses the NCSU Kit with AMI 0.5 µm CMOS process models. The setup listed in Table 4.1 below describes the inputs used. Unlike the programmable gain amplifier, the

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Supply ((V_{DD}, V_{SS}))</td>
<td>1.8V, 0V</td>
</tr>
<tr>
<td>Common-mode Voltage ((V_{cm}))</td>
<td>900mV</td>
</tr>
<tr>
<td>Bias Current ((I_{bias}))</td>
<td>20µA</td>
</tr>
</tbody>
</table>

Table 4.1: Sample and Hold Simulation & Experimental Setup

S/H was given a slightly higher power rail. This allows each switch more room to operate and pass the input signal more effectively. In addition to Table 4.1, the input offset voltage was set to zero for a representation of an ideal response. Figure 4.4 shows the response of the differential sample and hold output from a 1kHz sinusoidal differential input and sampling clock rate of 5kHz and various amplitudes. Figure 4.5 shows the response of the differential sample and hold output from a 1MHz sinusoidal differential input and sampling clock rate of 5MHz. Each capacitor in the design has a value of 5pF and the sampling switches were built using PMOS transistors with width of 15µm, NMOS transistors with width of 7.5µm, and lengths for both N- and P-type of 1µm.
Figure 4.4: Sample and Hold Simulation Analysis for 1kHz Input (a) 100mV (b) 500mV (c) 700mV (d) 900mV

4.3.1 Frequency Response

For simulation frequency response analysis, the input of the sample and hold circuit was a one volt amplitude, zero degree phase, AC signal. The sampling switches were closed to obtain the frequency response during the tracking phase. The output phase and magnitude (dB) were plotted and measurements were taken of the two cutoff frequencies. Again, as stated in previous sections, the S/H circuit behaves as a bandpass filter in terms of its frequency response. Table 4.2 compares the frequencies calculated in Section 4.2.1 with the values found in simulation.
4.3.2 S/H Error Analysis

Error calculations for the S/H were performed by loading the output signals into Matlab for analysis. Code for calculating each error associated with the sample and hold is shown in Appendix C. The S/H circuit input was varied in terms of amplitude, signal frequency, and sampling frequency. Sample mode errors are listed for the worst case response of the S/H at high frequencies (MHz). Each of the hold errors are listed below in terms of the mean and maximum errors occurred during two cycles of the input signal.
Table 4.2: S/H Theory and Simulation Frequency Response

<table>
<thead>
<tr>
<th>Pole</th>
<th>Theory</th>
<th>Simulation</th>
<th>Error (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_0$ Hz</td>
<td>7.162</td>
<td>0.3135</td>
<td>-95.63</td>
</tr>
<tr>
<td>$f_1$ MHz</td>
<td>28.15</td>
<td>28.82</td>
<td>2.365</td>
</tr>
</tbody>
</table>

Table 4.2: S/H Theory and Simulation Frequency Response

4.3.2.1 Sample Mode

Sample mode errors basically reiterate the errors associated with the OTA. This means that errors involving acquisition time, output slewing, and overshoot are related to the OTA characteristics. Table 4.3 lists each error associated with the S/H for various input signal amplitudes, input signal frequency of 1MHz and sampling frequency of 5MHz. The value associated for each of the sample mode errors typically occurs for the worst case input. That is, the worst case response occurs when the sampling switch is told to sample the maximum input signal amplitude. The measurements for acquisition time, overshoot, and settling time were performed using the calculator tool in the Affirma simulation environment.

<table>
<thead>
<tr>
<th>Error</th>
<th>Amplitude 100mV</th>
<th>Amplitude 500mV</th>
</tr>
</thead>
<tbody>
<tr>
<td>Acquisition Time (ns)</td>
<td>440</td>
<td>760</td>
</tr>
<tr>
<td>Overshoot (mV)</td>
<td>0.7</td>
<td>2</td>
</tr>
<tr>
<td>Settling Time (ns)</td>
<td>390</td>
<td>670</td>
</tr>
</tbody>
</table>

Table 4.3: S/H Simulation Sample Mode Error Analysis

4.3.2.2 Hold Mode

Hold mode errors are dependent on the switches used in the S/H as well as the hold capacitors. Measurements for hold mode errors were calculated in
Matlab and the code is shown in Appendix C. Refer to Table 4.4 for hold mode errors.

<table>
<thead>
<tr>
<th>Error</th>
<th>Amplitude 100mV</th>
<th>Amplitude 500mV</th>
</tr>
</thead>
<tbody>
<tr>
<td>Droop/Leakage (mV)</td>
<td>0.115</td>
<td>1.7</td>
</tr>
<tr>
<td>Pedestal (mV)</td>
<td>0.138</td>
<td>1.6</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Error</th>
<th>Amplitude 700mV</th>
<th>Amplitude 900mV</th>
</tr>
</thead>
<tbody>
<tr>
<td>Droop/Leakage (mV)</td>
<td>8.8</td>
<td>19</td>
</tr>
<tr>
<td>Pedestal (mV)</td>
<td>10.4</td>
<td>20</td>
</tr>
</tbody>
</table>

Table 4.4: S/H Simulation Hold Mode Error Analysis

4.3.3 Implemented Silicon Area

Using Cadence Virtuoso XL Layout Editor, the sample and hold circuitry was created using an AMI 0.5µm CMOS analog process. The implemented layout is shown in Figure 4.6. The total silicon area used is 479.1µm in width by 302.55µm in height yielding an area of 0.145mm². The unit capacitance chosen is 250fF and the switch sizes are listed in Section 4.3.

4.4 Experimental Results

Experimental analysis was performed on the designed sample and hold circuitry shown in Figure 4.1. The circuit was fabricated by MOSIS using an AMI 0.5µm CMOS process. The DC signal setup used for the S/H is the same as listed for the simulation setup in Table 4.1. Complimentary input signals were created using a single CA3280 OTA as an inverting amplifier with unity gain. In addition, the differential output was measured using two CA3280 OTAs as buffers feeding the inputs of a third CA3280 used as a differential-to-single ended converter.
Figure 4.6: S/H Layout 144951.7 $\mu m^2$ (479.1$\mu m \times 302.5\mu m$)

Figure 4.7 shows the operation of the S/H circuit for 250mV (500mVpp) and 500mV (1Vpp) input signals with 1kHz signal frequency and 5kHz sampling frequency. The operational analysis was stored onto an HP digital storage oscilloscope and plotted in Matlab. Accuracy analysis was performed on the data vectors for comparison to the simulation response. See Appendix C for analysis software.

4.4.1 Frequency Response

As with the programmable gain amplifier, an HP 4195A Network/Spectrum Analyzer was used to test the frequency response of the sample and hold. In order to measure the maximum, and minimum, input frequencies, the sampling switches are closed and the frequency of the input signal was swept over the range from 1kHz to 30MHz. Due to the limitations of the network analyzer, the minimum operating frequency was not measurable but maximum frequency measurements show a value of approximately 4.01MHz.
4.4.2 S/H Error Analysis

Upon taking measurements using a digital storage oscilloscope as discussed before, the output signal was analyzed for S/H errors in Matlab. Code used for analysis is the same as the code used in analyzing the simulation results and can be found in Appendix C.

4.4.2.1 Sample Mode

Sample mode errors were found using the same method described in the Simulation section. Using the setup listed above, the differential output voltage was stored to disk using an HP storage oscilloscope. This data was loaded into Matlab for error analysis using the same software as in the simulation section. By using a sampling frequency 5 times that of the input signal frequency, measurements for acquisition time, overshoot, and settling time were stored for roughly two periods. Two cycles of measurements include roughly 10 measurements, which is well within the Nyquist criterion. Table 4.5 lists each error for the fabricated S/H.

Figure 4.7: Sample and Hold Experimental Analysis for 1kHz Input
### Table 4.5: S/H Experimental Sample Mode Error Analysis

<table>
<thead>
<tr>
<th>Error</th>
<th>Amplitude 250mV</th>
<th>Amplitude 500mV</th>
</tr>
</thead>
<tbody>
<tr>
<td>Acquisition Time ($\mu$s)</td>
<td>1.19</td>
<td>1.424</td>
</tr>
<tr>
<td>Overshoot (mV)</td>
<td>85.5</td>
<td>93.75</td>
</tr>
<tr>
<td>Settling Time (ns)</td>
<td>748</td>
<td>612</td>
</tr>
</tbody>
</table>

4.4.2.2 Hold Mode

Just as with sample mode errors, an HP storage oscilloscope was used to record the differential output signal as well as the differential input signal. Using Matlab the hold mode errors, droop and pedestal errors, were calculated. Table 4.6 lists each error for the fabricated S/H, including hold mode errors.

### Table 4.6: S/H Experimental Hold Mode Error Analysis

<table>
<thead>
<tr>
<th>Error</th>
<th>Amplitude 250mV</th>
<th>Amplitude 500mV</th>
</tr>
</thead>
<tbody>
<tr>
<td>Droop/Leakage (mV)</td>
<td>5.2 21.3</td>
<td>8.1 59.8</td>
</tr>
<tr>
<td>Pedestal (mV)</td>
<td>8 21.7</td>
<td>21.6 53.9</td>
</tr>
</tbody>
</table>

4.5 Summary

Analysis of the sample and hold circuit indicate favorable results for low-voltage operation. The input amplitude used in simulation demonstrate adequate results for peak-to-peak values close to the power supply rails. Laboratory experiments of the fabricated sample and hold show slightly higher errors in hold mode accuracy as well as sample mode. This could be attributed to the breadboard setup including parasitic resistances and capacitances as well as introduction of noise from measurement devices and instrumentation. In all, the low-voltage operation of a sample and hold circuit was performed. The power supply for this design, however, is different than that of the programmable gain amplifier and the
DAC. The increase to 1.8V was used to allow the sampling switches more room to operate and thus higher accuracy for large input signal amplitudes. Table 4.7 list the various sample and hold results from simulation and experimental analysis with a 500mV input signal amplitude.

<table>
<thead>
<tr>
<th>Error</th>
<th>Simulation</th>
<th>Experimental</th>
</tr>
</thead>
<tbody>
<tr>
<td>Acquisition Time (ns)</td>
<td>760</td>
<td>1424</td>
</tr>
<tr>
<td>Overshoot (mV)</td>
<td>2</td>
<td>93.75</td>
</tr>
<tr>
<td>Settling Time (ns)</td>
<td>670</td>
<td>612</td>
</tr>
<tr>
<td>Droop/Leakage (mV)</td>
<td>4.9</td>
<td>59.8</td>
</tr>
<tr>
<td>Pedestal (mV)</td>
<td>3.9</td>
<td>53.9</td>
</tr>
</tbody>
</table>

Table 4.7: S/H Error Analysis Results for 500mV Input Sinusoid
5 DIGITAL-TO-ANALOG CONVERTER

5.1 Introduction

Digital-to-Analog converters are an important component of electronic design. The world of digital technology has pushed the boundaries of portable consumer electronics to the realms of MP3 players and cellular phones. However, in order for these devices to be useful, the audio signal must reach the consumer’s ear and thus the need for converting the digital code to a usable analog output. This is just one of many applications for the digital-to-analog converter or better known as the DAC. The design presented in this section is a low-voltage, 6-bit, charge-scaling DAC.

5.2 Operation

The operation of this particular DAC shown in Figure 5.1 is based on capacitive charge transfer and thus the name charge-scaling. Most charge-scaling D/A converters are based on a switch structure that includes ground and a single reference voltage for single-ended designs, and dual polarity reference voltages for fully-differential designs. By examining the circuit in Fig. 5.1 the charge stored on each capacitor is given by

\[ Q_n = d_n 2^n CV_n \]  \hspace{1cm} (5.1)

where \( Q_n \) is the n-bit capacitor charge, \( d_n \) is nth bit value, \( C \) is the unit capacitance value, and \( V_n \) is the nth bit reference voltage value. For low-voltage design, the voltage value corresponding to \( d_n = 0 \) is given as \(-V_{ref}\) and \( d_n = 1 \) is given as \( V_{ref} \). Fig. 5.1 uses the voltage rails to set the reference voltage (i.e. \( V_{ref} = V_{DD} \)). This allows operation for the entire range of the supply. By summing the charge on each input capacitor and finding the difference between the input nodes, the
net charge transfer to the feedback capacitors for an N-bit converter is given as

$$\Delta Q = \sum_{k=0}^{N-1} d_k 2^k 2V_{\text{ref}} = 2V_{\text{ref}} C \sum_{k=0}^{N-1} 2^k d_k$$  \hspace{1cm} (5.2)$$

The differential output voltage can therefore be found by the equation

$$v_{\text{out}} = \frac{\Delta Q}{C_{FB}}$$  \hspace{1cm} (5.3)$$

where $v_{\text{out}}$ is the differential output voltage, $\Delta Q$ is the net charge transfer shown in Equation (5.2) and $C_{FB}$ is the feedback capacitance equal to $2^{N-1}C$. By substituting Equation (5.2) into Equation (5.3) the differential output voltage can be shown as

$$v_{\text{out}} = \frac{2V_{\text{ref}} C \sum_{k=0}^{N-1} 2^k d_k}{2^{N-1}C} = 2V_{\text{ref}} \frac{\sum_{k=0}^{N-1} 2^k d_k}{2^{N-1}}$$  \hspace{1cm} (5.4)$$

For the case illustrated in Fig. 5.1 where the reference voltage is equal to the power rails, the QFG DAC has a total conversion range from $2V_{DD}$ to $2V_{SS}$. 

Figure 5.1: N-Bit Charge-Scaling QFG Digital-to-Analog Converter [1]
The resolution of the converter is directly related to the reference voltage and the number of bits. Since this design is fully differential, the least significant bit (LSB) voltage, or resolution, is given as

\[ V_{LSB} = \frac{2(V_{ref+} - V_{ref-})}{2^N} = \frac{V_{ref}}{2^{N-2}} \]  

(5.5)

5.2.1 Accuracy Analysis

Quite simply, accuracy analysis for a digital-to-analog converter is based on how well the digital word is converted into an analog output signal. The characteristics for an accurate and robust design include the linearity of the design, quantization error, maximum clock signal, settling time, and so on. The metrics presented below are used to analyze the proposed design using the QFG approach.

5.2.1.1 Differential Nonlinearity

Differential nonlinearity, or DNL, refers to the transition width of the analog output for equally spaced bit intervals. Figure 5.2 demonstrates the step transitions for an ideal 3-Bit digital-to-analog converter along with the analog output resulting from DNL error. The DNL for a digital-to-analog converter can be considered as the quantization error. In other words, the difference between the output levels corresponding to each digital word of an ideal DAC and an actual DAC is known as DNL. DNL can be calculated by the equation

\[ DNL_n = \frac{h'_n - h_n}{res} \]  

(5.6)

where \( DNL_n \) is the DNL error at transition \( n \), \( h'_n \) is the actual height of transition \( n \), \( h_n \) is the ideal height of transition \( n \), and \( res \) is the resolution of the least significant bit (LSB) of the converter. The DNL specification defines the DACs ability to generate uniform analog LSB multiples at the output \( \Box \).
5.2.1.2 Integral Nonlinearity

Integral nonlinearity, or INL, is the measure of the linearity of the output of a DAC with respect to the first and last transition points. INL can be defined as the difference between the data converter output values and a reference line drawn through the first and last output values. The equation for INL error is given by

\[ INL_n = \frac{V_{out,n} - V_{ref,n}}{res} \]  

(5.7)

where \( INL_n \) is the INL error for input code \( n \), \( V_{out,n} \) is the output value for input code \( n \), \( V_{ref,n} \) is the value of the reference line at input code \( n \), and \( res \) is the LSB resolution of the DAC. Figure 5.3 shows an example of INL error for a 3-Bit DAC.
5.2.1.3 Gain Error

Gain error for a DAC can occur because of poorly matched devices and low amplifier gain. Essentially, gain error is defined as the difference between the slope of the best-fit line through the DAC transfer curve and the slope of the ideal output curve. Gain error is illustrated in Figure 5.4.

5.2.1.4 Offset Error

The ideal response of a digital-to-analog converter will realize an output voltage equal to the reference voltage (typically ground) for the digital word corresponding to all zeros. However, at times, an offset can exist causing the curve to shift up or down. This offset error is typically removed before analyzing other
errors associated with the DAC.

5.2.2 Speed Analysis

Conversion speed of a digital-to-analog converter is an extremely important characteristic. As digital technologies increase in frequency, the methods for converting this data to an analog output (when necessary) is of utmost importance. The speed of a DAC is typically based on the speed of the amplifier used and size of the capacitors in the case of a charge-scaling D/A converter. Two areas of importance in the speed criterion are slew rate and settling time.
5.2.2.1 Slew Rate

Slew rate directly relates the speed of the D/A to the speed of the OTA. For testing slew rate, the input digital word is changed from all zeros to all ones. This dramatic step change causes the DAC to respond to the full-scale reference voltage. Slew rate is defined as the slope of the transfer from 10% of the output signal to 90% of the output signal and was shown in simulation to be 1.278V/µs.

5.2.2.2 Settling Time

Settling time is also related to the OTA and only becomes a serious problem as the LSB frequency increases. Settling time is the amount of time necessary for the output waveform to settle to a specified value within a certain tolerance. This specification is measured by, again, changing the digital word from all zeros to all ones. Assuming the OTA is properly compensated, the settling time should be very small because the OTA is stable.

5.3 Simulation Results

5.3.1 Operation

Simulations for the digital-to-analog converter were performed in the Cadence Affirma Analog Design Environment. Each MOSFET in the design uses the NCSU Kit with AMI 0.5 μm CMOS process models. The setup listed in Table 5.1 below describes the inputs used. The input offset voltage was set to zero for a

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Supply ($V_{DD}, V_{SS}$)</td>
<td>0.75V, -0.75V</td>
</tr>
<tr>
<td>Common-mode Voltage ($V_{cm}$)</td>
<td>0V</td>
</tr>
<tr>
<td>Bias Current ($I_{bias}$)</td>
<td>20µA</td>
</tr>
</tbody>
</table>

Table 5.1: Digital-to-Analog Converter Simulation & Experimental Setup
5.3.2 Accuracy Analysis

Each of the errors associated with the digital-to-analog converter and listed above were analyzed using the Matlab processing environment. Code for error calculation can be viewed in Appendix C. The load capacitance was chosen as 1pF and several reference voltage values were chosen. Initially, the reference voltage chosen was equal to the power rails for the converter (i.e. $V_{DD}$ and $V_{SS}$). The output curve versus the ideal curve is shown in Figure 5.5(b) for a reference of 1.5V. Due to the large errors at the first and last code transitions, the reference voltage was lowered. This allowed the D/A converter more headroom for operating within the voltage rails. Figure 5.5(a) demonstrates the DAC’s conversion abilities using a 1.25V reference voltage.

Figure 5.5: DAC Simulation Output Voltage Curve for $V_{ref} = 1.25, 1.5V$
5.3.2.1 Differential and Integral Nonlinearity

Code analysis of the simulation outputs indicate errors which are slightly greater than expected. The maximum DNL and INL errors are typically used to characterize a digital-to-analog converter and can be found in the following section. Figure 5.6 is a plot of the DNL and INL curves for reference voltages of 1.25V and 1.5V. It is evident from the plots that the maximum INL error is quite high for a reference voltage of 1.5V.

5.3.2.2 DAC Simulation Accuracy Summary

Each error associated with the accuracy of the DAC is shown in Table 5.2. The maximum DNL and INL errors are typically less than plus and minus $\frac{1}{2}$ LSB. Transient analysis of the low-voltage DAC is shown in Figure 5.7. The digital inputs to the DAC were changed from all zeros to all ones and the amount of time necessary for the DAC to settle to its final value was measured. The measurement
\[ V_{ref} = 1.25V \] \[ V_{ref} = 1.5V \]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>6 bits</td>
<td>6 bits</td>
</tr>
<tr>
<td>Max. INL Error (LSBs)</td>
<td>0.111</td>
<td>1.0413</td>
</tr>
<tr>
<td>Max. DNL Error (LSBs)</td>
<td>0.0272</td>
<td>0.488</td>
</tr>
<tr>
<td>Offset Error (mV)</td>
<td>-5</td>
<td>56</td>
</tr>
<tr>
<td>Gain Error (mV/LSB)</td>
<td>-0.62</td>
<td>1.113</td>
</tr>
<tr>
<td>Settling time (ns)</td>
<td>340</td>
<td>410</td>
</tr>
<tr>
<td>Static Power ((\mu)W)</td>
<td>809</td>
<td>809</td>
</tr>
</tbody>
</table>

Table 5.2: DAC Simulation Results

was made at 99.6% (8 bits) of full scale input pulses for reference voltages of 1.25V and 1.5V.

5.3.3 Implemented Silicon Area

Once again, silicon area of the device is very important. For a D/A to be effective, it must be accurate, fast, and compact. This is because new portable technologies are shrinking in total size. For example, an MP3 player, which requires a DAC to convert the digital code to analog audio, has become small enough to fit in a shirt pocket. Thus, the microprocessor used in the design must be small and this leads to the requirement of a small DAC. Figure 5.8 shows the implemented silicon layout for the 6-Bit low-voltage DAC that employs QFG transistors and its total area is 0.507 \(mm^2\).

5.4 Experimental Results

5.4.1 Operation

Experimental analysis of the low-voltage, 6-bit digital-to-analog converter was performed in the lab using HP function generators, programmable power supplies, and digital multimeters. The autozeroing clock was pulsed at a very low
frequency (250mHz) and each bit sequence was changed manually. This allowed the testing of each word analog output as well as offset voltage. However, speed measurements were made by changing the input word from all zeros to all ones using a square wave input signal. The setup parameters listed in Table 5.1 were used in the laboratory setup as well.

5.4.2 Accuracy Analysis

The analog output voltage corresponding to each digital word input was entered into Microsoft Excel for post processing. The data was then stored in text files for easy entry into the Matlab processing environment. Once loaded, the output voltage levels for reference voltages of 1.25V and 1.5V were analyzed for accuracy.

As with the simulation response, the initial experimental setup used a reference voltage of 1.5V. Matlab analysis of the output signals indicated poor outer code values as indicated in Figure 5.9(b). Thus, the digital-to-analog converter
needed more room within the power rails to operate effectively. The second test in the lab used a reference voltage of 1.25V, which resulted in far more accurate results. This is apparent in Figure 5.9(a).

5.4.2.1 Differential and Integral Nonlinearity

DNL and INL errors were calculated for each transition of the 6-bit DAC. The results indicate a poor response from the D/A when using a reference voltage of 1.5V. This is evident in Figure 5.10 where the results for the 1.5V reference are consistent with that of the simulation.

5.4.2.2 DAC Experimental Accuracy Summary

A summary of the fabricated DAC accuracy is shown in Table 5.3. The table indicates accuracy values that are slightly better than that of the simulation response when the reference voltage is 1.25V.
The digital-to-analog converter did perform as expected when compared to the simulation results. Initially, the design included unit capacitance sizes of 5pF. However, each of the proposed quasi-floating gate designs were required to be included on a single chip. This posed a problem in terms of space for including the DAC with the amplifier and sample and hold. Thus, the decision was made to decrease the capacitance sizes in order to allow all three circuits to be fabricated.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>$V_{ref} = 1.25V$</th>
<th>$V_{ref} = 1.5V$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>6 bits</td>
<td>6 bits</td>
</tr>
<tr>
<td>Max. INL Error (LSBs)</td>
<td>0.2572</td>
<td>2.0368</td>
</tr>
<tr>
<td>Max. DNL Error (LSBs)</td>
<td>0.34912</td>
<td>0.63093</td>
</tr>
<tr>
<td>Offset Error (mV)</td>
<td>-8.8</td>
<td>2.729</td>
</tr>
<tr>
<td>Gain Error (mV/LSB)</td>
<td>-8.8</td>
<td>104.3</td>
</tr>
<tr>
<td>Settling Time (ns)</td>
<td>400</td>
<td>500</td>
</tr>
<tr>
<td>Static Power ($\mu$W)</td>
<td>765</td>
<td>769</td>
</tr>
</tbody>
</table>

Table 5.3: DAC Simulation Results
Figure 5.10: 6-Bit DAC Simulation DNL and INL Curves

on the same IC. This capacitance reduction could cause the inaccuracies due to poor matching. Table 5.4 lists the summary for the 6-Bit charge-scaling digital-to-analog converter implemented with QFG transistors for a reference voltage of 1.25V.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Simulation</th>
<th>Experimental</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>6 bits</td>
<td>6 bits</td>
</tr>
<tr>
<td>Max. INL Error (LSBs)</td>
<td>0.111</td>
<td>0.2572</td>
</tr>
<tr>
<td>Max. DNL Error (LSBs)</td>
<td>0.0272</td>
<td>0.34912</td>
</tr>
<tr>
<td>Offset Error (mV)</td>
<td>-5</td>
<td>-8.8</td>
</tr>
<tr>
<td>Gain Error (mV/LSB)</td>
<td>-0.62</td>
<td>-8.8</td>
</tr>
<tr>
<td>Settling time (ns)</td>
<td>340</td>
<td>400</td>
</tr>
<tr>
<td>Static Power (µW)</td>
<td>809</td>
<td>765</td>
</tr>
</tbody>
</table>

Table 5.4: DAC Results Summary for $V_{ref} = 1.25V$
6 FUTURE RESEARCH

As with any design, hindsight and analysis of the proposed circuit tend to indicate procedures and considerations that could yield better results. Invariably, these design considerations should have been considered during initial design but were left out due to time constraints, silicon area, or other relevant factors. This section will discuss several concerns important for future research.

6.1 The QFG Diode

First and foremost, the question arises regarding the special case when the QFG biasing diodes become forward biased. Upon initial inspection, the conclusion was reached that the diodes cannot become forward biased under a closed-loop system. This is because the amplifier is trying to maintain a zero voltage drop at the input terminals. However, a problem can occur when the input signal is an extremely fast changing signal. That is, if a very fast input pulse is sent to the amplifier inputs, the output will be slew-rate limited. Thus, the input voltage differential will experience a sudden deviation from the nominal zero Volts. This deviation, in turn, could cause the QFG biasing diodes to become forward biased. Upon simulation analysis, the change of voltage at the input terminal was not enough to turn the diode on. In order to relieve this problem if it were to occur, two back-to-back diodes could be used to bias the QFG transistors instead of single diodes.

6.2 Design Considerations

One sounding theme throughout the discussion of this paper has been the low open-loop gain of the operational transconductance amplifier. This created accuracy issues regarding the programmable gain amplifier as well as the digital-
to-analog converter. The recommendation for this inadequacy is to design the OTA with at least 60dB open-loop gain. This makes the design more applicable to current industry standard circuitry. In redesigning the OTA, the stability must be maintained as well as the speed. Also, a low-voltage/low-power design encourages the designer to forego cascoding and keeping the current biasing at a relatively low level.

Additional design considerations for the digital-to-analog converter can be considered small but are quite necessary. First and foremost, the DAC presented in this paper was demonstrated with a resolution of 6 bits. This was just to prove the low-voltage application of the QFG design. However, to be a useful industry design, the D/A converter needs a resolution of 8 bits or greater. In many audio applications, 8 bits of resolution is the minimum. Also, the original unit capacitance size for the DAC was set to 5pF. This posed a problem in layout due to increased area. Thus, to be able to include each QFG design on one IC, the unit capacitance was lowered to 1pF. The original 5pF capacitance could offer improved storage capabilities and less leakage. However, larger capacitance values require more time to charge. For a more robust design, capacitance sizes are typically sized based on the maximum thermal noise allowed for the circuit accuracy, which was a design consideration not used in this thesis.

6.3 Layout Issues

The final recommendation for future research is in regard to the layout of the QFG circuits. Transistor matching was performed using interdigitation and common-centroid layout techniques. However, the capacitor arrays were not connected in these configurations. This could provide for better accuracy by increasing the matching characteristics. Also, the resistors used in the CMFB circuit and autozeroing circuit were not matched other than unit sizes. In addition, the DAC layout was not rectangular, but this is a minor inconvenience. One
improvement could be made with regards to the QFG transistor layout. The proposed layout is shown in Fig. 1.2 for a 2-input QFG transistor. In this layout, the signals are capacitively coupled to the gate of the transistor by utilizing the poly I layer of the input transistor as the bottom plate of the capacitors. However, during layout, the QFG implementation was rushed and the connections were made using a metal layer from a separate poly I capacitance bottom plate and the poly I used for the transistor gate. Above all layout considerations, this should have first priority. The goal of this research was not compromised under the current layout scheme but results could show more accuracy if the proposed layout had been implemented in full.
APPENDICES
APPENDIX A: Design Calculations

**Theoretical Transistor Design Calculations**

**Given data values**

\[ I_{\text{bias}} = 50 \times 10^{-6} \quad V_{DD} = 0.75 \quad V_{SS} = -V_{DD} \quad A_v = 0.20 \]

\[ L = 1 \times 10^{-6} \quad K_{P} = 4 \times 10^{-6} \]

**Current Mirror Transistors**

\[ W_1 = \frac{2I_{\text{bias}}L}{K_{P}(A_v)^2} \quad W_1 = 0.25 \times 10^{-5} \quad W_1 = 60 \times 10^{-6} \quad W_3 = W_1 \]

\[ K = 10 \quad W_2 = K \cdot W_1 \quad W_4 = W_2 \quad W_5 = 2 \cdot W_1 \quad W_5 = 1.2 \times 10^{-4} \]

\[ W_7 = \frac{W_1}{4} \quad W_7 = 1.5 \times 10^{-5} \quad W_8 = W_7 \quad W_6 = K \cdot W_7 \quad W_9 = W_6 \]

\[ W_{13} = W_7 \quad W_{14} = W_{13} \quad W_{10} = 3 \cdot W_1 \quad W_{10} = 1.8 \times 10^{-4} \]

**Differential Pair Transistors (designed large for more gain and better matching)**

\[ W_{1A} = 200 \times 10^{-6} \quad W_{2A} = W_{1A} \quad W_{11} = W_{1A} \quad W_{12} = W_{11} \]

\[ W_{1B} = 2 \cdot W_{1A} \quad W_{2B} = W_{1B} \quad W_{1B} = 4 \times 10^{-4} \]

**QFG Biasing Transistors**

\[ W_{Q1} = W_7 \quad W_{Q2} = W_{Q1} \]
APPENDIX B: Theoretical Analysis

**Theoretical Analysis Calculations**

**Transistor, Resistor, and Capacitor Sizes**

\[ W_{10} = 180 \times 10^{-6} \quad L = 1 \times 10^{-6} \quad R_1 = 400 \times 10^{3} \quad R_2 = 100 \times 10^{3} \quad R_C = 1 \times 10^{3} \]

\[ C_{AZ} = 10 \times 10^{-12} \quad C_C = 0.75 \times 10^{-12} \quad K_{P_N} = 120 \times 10^{-6} \quad K_{P_P} = 40 \times 10^{-6} \quad C_L = 1 \times 10^{-12} \]

**Given data values**

\[ I_{bias} = 20 \times 10^{-6} \quad V_{DD} = 0.75 \quad V_{SS} = -V_{DD} \quad \Delta V = 0.20 \]

**Current Calculation from operating point analysis simulation**

\[ I_{D1A} = 9.064 \times 10^{-6} \quad I_{D2A} = 9.064 \times 10^{-6} \quad I_{D7} = 27.18 \times 10^{-6} \]

\[ I_{D8} = 27.18 \times 10^{-6} \quad I_{D4} = 206.8 \times 10^{-6} \quad I_{D9} = 204.6 \times 10^{-6} \quad I_{D1B} = 18.11 \times 10^{-6} \]

\[ I_{D2B} = 18.11 \times 10^{-6} \quad I_{D2} = 206.8 \times 10^{-6} \quad I_{D6} = 204.6 \times 10^{-6} \]

**Transconductance Calculation from simulation**

\[ g_{m2A} = 159.7 \times 10^{-6} \quad g_{m1A} = g_{m2A} \quad g_{m8} = 253.2 \times 10^{-6} \]

\[ g_{m7} = g_{m8} \quad g_{m4} = 2.642 \times 10^{-3} \quad g_{m9} = 2.133 \times 10^{-3} \quad g_{m1B} = 3 \times 10^{-6} \quad g_{m2B} = g_{m1B} \]
Drain Resistance Calculations from simulation

\[ e_{ds2A} := 39.98 \times 10^{-6} \quad e_{ds8} := 2.227 \times 10^{-6} \quad e_{ds4} := 44.011 \times 10^{-6} \quad e_{ds9} := 18.69 \times 10^{-6} \]

\[ e_{ds1B} := 5.235 \times 10^{-6} \]

\[ r_{o2A} := \frac{1}{e_{ds2A}} \quad r_{o8} := \frac{1}{e_{ds8}} \quad r_{o4} := \frac{1}{e_{ds4}} \quad r_{o9} := \frac{1}{e_{ds9}} \quad r_{o1B} := \frac{1}{e_{ds1B}} \]

\[ r_{o2A} = 2.301 \times 10^4 \quad r_{o8} = 4.49 \times 10^5 \quad r_{o4} = 2.727 \times 10^4 \quad r_{o9} = 5.35 \times 10^4 \quad r_{o1B} = 1.91 \times 10^5 \]

Parasitic Capacitance Calculations

\[ CGDO_p := 2.88 \times 10^{-10} \quad CGDO_n := 2.12 \times 10^{-10} \quad C_{ox} = 2.5 \times 10^{-15} \frac{10^{-15}}{(10^{-6})^2} \]

\[ C_{gd4} = CGDO_p \cdot W_4 \quad C_{gd9} = CGDO_n \cdot W_9 \]

\[ C_{gd2A} = CGDO_p \cdot W_{2A} \quad C_{gd8} = CGDO_n \cdot W_8 \]

\[ C_{gs9} = \frac{2}{3} \cdot W_9 \cdot L \cdot C_{ox} \quad C_{gs9} = 2.5 \times 10^{-13} \]

Pole analysis Resistance Calculations

\[ R_{out} := \left[ r_{o4}^{-1} + r_{o9}^{-1} + \left(2 \cdot R_1\right)^{-1}\right]^{-1} \quad R_{out} = 1.564 \times 10^4 \]

\[ R_{in} := \left( r_{o2A}^{-1} + r_{o8}^{-1} + r_{o1B}^{-1}\right)^{-1} \quad R_{in} = 2.108 \times 10^4 \]

Open-Loop Gain

\[ A_2 := e_{m9} \cdot R_{out} \quad A_2 = 23.254 \]

\[ A_D := e_{m2A} \cdot R_{in} \quad A_D = 3.366 \]

\[ A_{vo1} := A_D \cdot A_2 \quad A_{vo1} = 112.277 \quad A_{OL} := 2 \cdot A_{vo1} \quad A_{OL} = 224.555 \quad 20 \cdot \log(A_{OL}) = 47.026 \]
AC Frequency Analysis

\[ C_{p1} = C_{gd2A} + C_{gd3} + C_C \left(1 + A_2\right) + C_{gs} + C_{gd2} \left(1 + A_2\right) \]
\[ C_{p1} = 2.717 \times 10^{-11} \]

\[ C_{p2} = C_C \left(1 + \frac{1}{A_2}\right) + C_L \]
\[ C_{p2} = 1.772 \times 10^{-12} \]

\[ f_{p1} = \frac{1}{2 \pi R_{in} C_{p1}} \]
\[ f_{p1} = 2.779 \times 10^5 \]

\[ f_{p2} = \frac{1}{2 \pi R_{out} C_{p2}} \]
\[ f_{p2} = 5.742 \times 10^6 \]

\[ f_{3dB} := \min\left(f_{p1}, f_{p2}\right) \]
\[ f_{3dB} = 2.779 \times 10^5 \]

Gain Bandwidth Product

\[ GB = A_{vol} f_{3dB} \]
\[ GB = 3.12 \times 10^7 \]

Slew Rate

\[ SR := \frac{2 I_{bias}}{C_{p1}} \cdot 10^{-6} \]
\[ SR = 1.472 \]

Output Voltage Range

\[ V_{omax} = V_{DD} - \Delta V \]
\[ V_{omin} = V_{SS} + \Delta V \]

\[ V_{range} := V_{omax} - V_{omin} \]
\[ V_{range} = 1.1 \]

Static Power Dissipation

\[ I_{D1} = I_{bias} \]
\[ I_{D2} = I_{bias} \frac{W_2}{W_1} \]
\[ I_{D3} = I_{bias} \frac{W_3}{W_1} \]
\[ I_{D4} = I_{bias} \frac{W_4}{W_1} \]

\[ I_{D5} = I_{bias} \frac{W_5}{W_1} \]
\[ I_{D10} = I_{bias} \frac{W_{10}}{W_1} \]

\[ P_{static} := (V_{DD} - V_{SS}) \left(I_{D1} + I_{D2} + I_{D3} + I_{D4} + I_{D5} + I_{D10}\right) \]
\[ P_{static} = 8.1 \times 10^{-4} \]
Programmable Gain Amplifier Analysis

Closed-Loop Gain Analysis

\[ \beta = \begin{pmatrix} 1 \\ \frac{1}{2} \\ \frac{1}{4} \\ \frac{1}{8} \end{pmatrix} \quad A_{OL} = 100.31 \quad A_{CL} = \frac{A_{OL}}{1 + \beta A_{OL}} \quad A_{CL} = \begin{pmatrix} 0.99 \\ 1.961 \\ 3.847 \\ 7.409 \end{pmatrix} \]

Frequency Analysis

\[ C = 1 \times 10^{-12} \quad g_{dsQFG} = 225 \times 10^{-12} \quad R_{QFG} = \frac{1}{g_{dsQFG}} \quad R_{QFG} = 4.444 \times 10^5 \]

\[ R_{leak} = R_{QFG} \]

Input Pole (1) - Highpass Filter

\[ k = \begin{pmatrix} 1 \\ 2 \\ 4 \\ 8 \end{pmatrix} \quad i = 0..3 \quad f_{01} = \frac{1}{2 \pi R_{leak}(C/k)^i} \quad f_0 = \begin{pmatrix} 35.81 \\ 17.905 \\ 8.952 \\ 4.476 \end{pmatrix} \]

Bandwidth Extension Pole (2) - Lowpass Filter

\[ f_{3dB} = 2.779 \times 10^5 \quad f_1 = \left(1 + A_{OL} \beta \right) f_{3dB} \quad f_1 = \begin{pmatrix} 2.815 \times 10^7 \\ 1.422 \times 10^7 \\ 7.247 \times 10^6 \\ 3.762 \times 10^6 \end{pmatrix} \]
function erval = SNherror(data, varargin)
%SNHERROR Calculate hold mode error analysis for a S&H
%erval = SNHERROR(data) will use the information provided
%in data to find the hold mode errors and store them in
%the structure output variable erval. The input data
%matrix must have the following: column 1 - time data,
%column 2 - input data, column 3 - output data, and
%column 4 - sampling clock data.
%

time = data(:,1);
input = data(:,2);
output = data(:,3);
clk = data(:,4);

clock = clk;
clock(clk > 0) = 1;
clockshift = [clock(2:end); clock(1)];
transistion = clock - clockshift;
\n\nclock = clockshift - clockshift;
\n\nk = find(transistion == 1);
l = find(transistion == -1);
k = k(1:end-1);
l = l(2:end);
ideal = input(k);
firstactual = output(k);
lastactual = output(l);

%% Data parsing
holdlength = min(l - k);
holddata = zeros(holdlength,length(k));
holdtime = zeros(holdlength,length(k));
for i=1:length(k)
    holddata(:,i) = output(k(i):k(i)+holdlength-1);
    holdtime(:,i) = time(k(i):k(i)+holdlength-1);
end

%% Hold Mode Error Analysis
sample_error = holddata(1,:)’ - ideal;
droop_pedestal = zeros(holdlength-1,length(k));
for i=2:holdlength
    droop_pedestal(i,:) = holddata(i,:) - holddata(1,:);
end
pedestal = [max(droop_pedestal)]’;
droop = [min(droop_pedestal)]’;

erval.samp_error = sample_error;
erval.droop = droop;
erval.minDroop = max(droop);
erval.avgDroop = mean(droop);
erval.maxDroop = min(droop);
erval.pedestal = pedestal;
erval.minPedestal = min(pedestal);
erval.avgPedestal = mean(pedestal);
erval.maxPedestal = max(pedestal);

% data visualization
figure;
plot(time(k),ideal,'x',time(k),firstactual,'o')
hold on;
plot(time(l),lastactual, '+')
plot(time,input,'--r',time,output,'m')

function [erval]=dacerror(N,vref,lsb_T,isFD,filename)

%DACERROR Function for analyzing CMOS digital-to-analog converter errors.
% [erval]=DACERROR(N,vref,lsb_T,isFD,filename) will return the main errors associated with D/A conversions in the structure variable erval. The inputs used to analyze the data are the number of bits N, voltage reference VREF, least significant bit period, is the design fully-differential, and the filename.
%
% Notes: DACERROR developed from code written by Michael Holmes and Chad Lackey for EE590 D/A and A/D VLSI Design

% Author: Michael Holmes & Chad Lackey
% New Mexico State University
% Klipsch School of ECE
% Created: March 3, 2003
% Revised: March 8, 2003
%Load Data File
if nargin < 5
    [file,path]=uigetfile('*.mat','Open Output File');
    if path~=0
        DATA_STRUCT=load([path,file]);
        FILE_DATA(:,1) = DATA_STRUCT.time;
        FILE_DATA(:,2) = DATA_STRUCT.vout;
    else
        return
    end
else
    DATA_STRUCT = load(filename);
    FILE_DATA(:,1) = DATA_STRUCT.time;
    FILE_DATA(:,2) = DATA_STRUCT.vout;
end

%CREATE IDEAL VECTOR
Decimal=[0:1:(2^N)-1]';
if ~isFD
    Resolution=vref/(2^N);
    Ideal=Resolution*Decimal;
    Ideal_Slope=(vref-Resolution)/((2^N)-1);
else
    Resolution=2*vref/(2^N);
    Ideal = Resolution*Decimal - vref;
    Ideal_Slope=(Ideal(2^N)-Ideal(1))/((2^N)-1);
end
%Allocate Data Vectors
DATA=zeros(2^N,1);
AZtime = 10e-6;
TIME=AZtime + (lsb_T/2)*.8;

%Generate DAC Vectors
tol = 0.05;
for n=1:2^N
    m=find(FILE_DATA(:,1) >= TIME-(tol*(lsb_T/2)) & ...
            FILE_DATA(:,1) <= TIME+(tol*(lsb_T/2)));
    while isempty(m)
        tol = tol + 0.05;
        m=find(FILE_DATA(:,1) >= TIME-(tol*(lsb_T/2)) & ...
                FILE_DATA(:,1) <= TIME+(tol*(lsb_T/2)));
    end
    m = round(mean(m));
    TIME=TIME+(lsb_T/2);
    DATA(n)=FILE_DATA(m,2);
end

%Calculate Error Parameters
OFFSET = DATA(1) - Ideal(1);
%Slope = ((DATA(2^N)-DATA(1))/((2^N)-1));
%Slope = ((DATA(2^N)-DATA(1))/((2^N)-1));
%Slope = ((DATA(2^N)-DATA(1))/((2^N)-1));
%Slope = ((DATA(2^N)-DATA(1))/((2^N)-1));
SLOPE = ((DATA(2^N)-DATA(1))/((2^N)-1));
IdealHeight = Ideal(2) - Ideal(1);
DataHeights = DATA(2:end)-DATA(1:end-1);
\[ \text{DNLdata} = (\text{DataHeights} - \text{IdealHeight})/\text{Resolution}; \]
\[ \text{DNL} = \max(\text{abs(DNLdata)}); \]
%Find Integral Nonlinearity Error
\[ \text{INL} = \max(\text{abs(DATA-((SLOPE*Decimal)+DATA(1)))))/\text{Resolution}; \]
\[ \text{INLdata} = (\text{DATA-((SLOPE*Decimal)+DATA(1))))/\text{Resolution}; \]
%Solve for gain error
\[ \text{GAIN\_ERROR} = \text{Ideal\_Slope}-SLOPE; \]

\text{erval.DNL} = \text{DNLdata};
\text{erval.maxDNL} = \text{DNL};
\text{erval.INL} = \text{INLdata};
\text{erval.maxINL} = \text{INL};
\text{erval.offset} = \text{OFFSET};
\text{erval.gainer} = \text{GAIN\_ERROR};

\text{h} = \text{plot(Decimal, DATA,'o',Decimal,Ideal,'x'); grid on}
\text{set(h,'linewidth',1)}
\text{axis([0 2^N min([DATA;Ideal]) max([DATA;Ideal])])}
\text{set(gca,'fontsize',12,'fontname','ms serif')}
\text{xlabel('Digital Input Code(Decimal)','FontSize',12,...,'FontName','MS Serif')}
\text{ylabel('Vout(V)','FontSize',10,'FontName','arial')}
\text{title(['Simulation vs. Ideal for ',num2str(vref),...,'V Reference Voltage']),'FontSize',12,'FontName','MS Serif')
\text{legend('Simulated', 'Ideal',-1)}
\text{displaytext}=[{'DNL(\text{LSBs})='num2str(DNL)};...
\{{'INL(\text{LSBs})='num2str(INL)};...
\{{'GAIN\_ERROR(V/\text{LSB})='num2str(GAIN\_ERROR)}; ...
{['OFFSET(V)=',num2str(OFFSET)]};
text([5;5;5],[vref-0.125,vref-0.25,vref-0.375,vref-0.5],...
    displaytext,...
    'fontweight','bold',...
    'fontsize',12,'fontname','ms serif');
Figure D.1: QFG Final Chip
Figure D.2: QFG Programmable Gain Inverting Amplifier

Figure D.3: QFG Sample and Hold Circuit
Figure D.4: QFG 6-Bit Digital-to-Analog Converter
REFERENCES


