Ultra Wide Band Sigma-Delta modulator in CMOS090

Master’s thesis
performed in Electronics Systems
by
Fredrik Jonsson

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Linköping, 16th April 2004
Today the frequency spectrum is full of wireless standards. The most common technique being used is the frequency modulation. To take advantage of this and the technology improvement a new wireless communication standard is being developed. This standard is using a low power impulse modulation method, allowing it to overlap with other standards. The proposed standard called IEEE802.15.3a is applied at an Ultra Wide Band and has potential to be used both in interchip and intrasystem communication, since it allows a very high data density.

In this thesis the analog to digital converter is designed, which is one part of a communication system. Although the signal bandwidth is very wide the converter is designed as a Sigma-Delta modulator, which is most suitable for low-speed applications. Its main advantages over high-speed converters are less area and less power consumption. The goal of this project is to investigate if the CMOS090 process technology will be sufficient for reaching a signal-to-noise ratio, SNR, of 30 dB in a signal band of 264 MHz.

The main limiting factor during the design of the modulator is the excess feedback delay. This delay degrades the SNR and can even make the system unstable. At a feedback delay of 83 ps and a sampling frequency of 6.336 GHz, the maximum SNR achieved was 27 dB. At this high frequency the modulator is close to instability. Hence, to ensure stability a maximum sampling frequency of 4.224 GHz is chosen, achieving a SNR of 19 dB.

The effect of the feedback delay can be reduced either by using a different structure or by using compensation methods, either of them would probably allow a SNR above 30 dB.
Abstract

Today the frequency spectrum is full of wireless standards. The most common technique being used is the frequency modulation. To take advantage of this and the technology improvement a new wireless communication standard is being developed. This standard is using a low power impulse modulation method, allowing it to overlap with other standards. The proposed standard called IEEE802.15.3a is applied at an Ultra Wide Band and has potential to be used both in interchip and intrasystem communication, since it allows a very high data density.

In this thesis the analog to digital converter is designed, which is one part of a communication system. Although the signal bandwidth is very wide the converter is designed as a Sigma-Delta modulator, which is most suitable for low-speed applications. Its main advantages over high-speed converters are less area and less power consumption. The goal of this project is to investigate if the CMOS090 process technology will be sufficient for reaching a signal-to-noise ratio, SNR, of 30 dB in a signal band of 264 MHz.

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The effect of the feedback delay can be reduced either by using a different structure or by using compensation methods, either of them would probably allow a SNR above 30 dB.

Keywords: Sigma-Delta modulator, Ultra Wide Band, UWB, Excess feedback delay, CMOS090
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One of my aims in life has been to receive a Master’s of Science degree and this report is the final step to reach it.

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Chapter 1

Introduction

1.1 Introduction

This chapter introduces the reader to the project. First some background knowledge and the goal is given, followed by a deeper insight in wireless communication. Finally the chapter ends by showing the organization of the report.

1.2 Background and goal of project

Mankind has always had a desire for communication. In early days smoke signals were used in a communication system, but today electromechanical signals are used instead. In 1901, Marconi was the first person to send a radio message over the Atlantic Ocean. During the 20th century this radio transmission system has improved rapidly and is now much faster, more reliable and reaches further distances. The fast development is mainly due to the discovery of the transistor, allowing production of fast integrated circuits. This thesis that has taken place at Philips Research in Eindhoven is describing the development of one part in a top of the line communication system.

Due to increasing demands from consumers and improved technology a new wireless communication standard is being developed. The standard is called IEEE802.15.3a and is applied at an Ultra Wide Band, UWB. It has potential to be used both in chip-to-chip communication and short distance communication (10 m). Compared to WLAN and BlueTooth the data density can be 10 to 50 times higher [5], which would offer new possibilities in applications. One can imagine a complete wireless house, where the only cables are supply cables.

In this thesis the analog to digital converter, which is one block in a communication system, will be developed. The goal is to reach a
Introduction

The signal-to-noise ratio, SNR, of around 30 dB, meaning 5 bits resolution in a CMOS technology using a Sigma-Delta oversampling structure. This SNR is quite low compared to a 44 kHz 16 bit audio SNR of about 96 dB, but on the other hand the bandwidth is 12000 times higher. Due to the extremely high bandwidth a simple, fast, and power efficient structure is required. The state of the art CMOS090 process technology is chosen, the fastest CMOS process available. Although the signal band is much larger in the UWB case, the lower SNR is relaxing the required speed of the modulator. For a second-order structure this modulator needs to be about 190 times faster than the audio converter. Will this be possible? This question will be answered in this report. The given specification is summarized in table 1.1.

<table>
<thead>
<tr>
<th>Technology</th>
<th>CMOS090</th>
</tr>
</thead>
<tbody>
<tr>
<td>Structure</td>
<td>Sigma-Delta modulator</td>
</tr>
<tr>
<td>Power supply</td>
<td>1.2 V</td>
</tr>
<tr>
<td>Signal bandwidth</td>
<td>0 - 264 MHz</td>
</tr>
<tr>
<td>Nyquist frequency</td>
<td>528 MHz</td>
</tr>
<tr>
<td>SNR</td>
<td>∼ 30 dB</td>
</tr>
</tbody>
</table>

Table 1.1: Specification of the Sigma-Delta modulator for the proposed UWB standard

1.3 Wireless communication

1.3.1 Receiver architecture

In order to communicate both a transmitter and a receiver are required. These are built of more or less the same parts, but they are placed in reversed order. Here the receiver will be studied, shown in figure 1.1. Ideally the signal created by the antenna could be fed directly to the analog to digital (a/d) converter and then processed by a digital signal processor (DSP), but the power and frequency is too high (>100 dB and >1 GHz) according to [2].

To reduce the power and filter out-of-band noise a preselection filter is placed after the antenna and outputs a quite weak signal (µV), which is amplified by a low-noise amplifier. In order to mix the signal to an intermediate frequency (IF) without imaging a bandpass image rejection filter is applied before the mixer. The mixer is followed by an IF filter that is making the power appropriate to the a/d converter and is followed by a steeper filtering of the out-of-band noise. To relax the requirements of the a/d converter an additional mixer is applied to mix the signal to the baseband. Here the receiver is of heterodyne type, which has two phase quadrature signal paths, 90 degrees phase-shifted
1.3. Wireless communication

![Diagram of a Heterodyne quadrature receiver structure](image)

Figure 1.1: Heterodyne quadrature receiver structure

...to each other. The analog signals are then transferred to the digital domain by a continuous-time Sigma-Delta modulator. If a discrete-time Sigma-Delta modulator would have been used then a lowpass (LP) filter had been required to avoid aliasing, which will be shown in chapter 2 and 3. Finally a DSP can do the data-processing.

### 1.3.2 Radio frequencies

To avoid overlapping bands the radio frequency range is divided into different bands, where standards are settled to ensure compatibility. In figure 1.2 well known bands are shown together with the Ultra Wide Band, which this project is aiming at.

<table>
<thead>
<tr>
<th>RADIO FREQUENCIES</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 kHz</td>
</tr>
<tr>
<td>AM</td>
</tr>
</tbody>
</table>

Figure 1.2: Frequency bands used for transmission of radiowaves

### 1.3.3 Ultra Wide Band

The rising demands for wireless communication put higher demands on the technology development. More data needs to be transmitted in the same time and the existing transmission standards have a limited data rate. Due to technology improvements higher transmission...
frequencies are allowed. As a result a new standard is being developed. The proposed standard is called IEEE802.15.3a and is aiming at a new frequency band, called Ultra Wide Band, UWB. The band has a frequency range between 3.1 and 10.6 gigahertz. It will be divided into sub bands of 528 MHz, and frequency hopping techniques will be used to jump between the bands. An UWB is defined if the following definition is satisfied,

\[ f_b > 0.25f_c \]  \hspace{1cm} (1.1)

where \( f_b \) is the signal frequency and \( f_c \) is the center frequency.

In this high frequency range each part typically is mixed down to the baseband to relax the requirements on the analog to digital converter, using the receiver structure shown in figure 1.1.

The UWB standard is different from other typical modern communication standards where signals are transmitted in a Narrow Band (NB). In the NB the data is transmitted using a frequency modulation method, but in the UWB case an impulse modulation method is used. By utilizing this difference the UWB is allowed to overlap with NB standards if the FCC regulations are fulfilled. The FCC organization is setting the rules for radio communication in USA. In Europe this organization is called CEPT. In order to fulfill the regulations from FCC the power of the signals in the UWB have to be less than -41.25 dBm/MHz. Since the energy of the UWB signal is spread over a wide frequency range, there will be a negligible disturbance to a narrow band standard overlapping with the UWB. In the NB case all energy are distributed in a small frequency range, making it impossible to overlap with other NB standards without disturbing each other. In figure 1.2 it is shown how one of the WLAN standards is overlapping with the UWB.

A calculation of the total energy in the UWB is resulting in a higher data density compared to other existing standards. In the UWB a data density of 1000 kbps/m\(^2\) can be transferred compared to other existing standards, where the maximum density is less than 100 kbps/m\(^2\). This high data density makes the UWB interesting for interchip and intrasystem communication.

In table 1.2 the specification of proposed UWB standard is summarized.

<table>
<thead>
<tr>
<th>Standard</th>
<th>IEEE802.15.3a</th>
</tr>
</thead>
<tbody>
<tr>
<td>UWB</td>
<td>3.1 - 10.6 GHz</td>
</tr>
<tr>
<td>Subbands</td>
<td>528 MHz</td>
</tr>
<tr>
<td>Modulation</td>
<td>Impulse</td>
</tr>
<tr>
<td>Max signal power</td>
<td>-41.25 dBm/MHz</td>
</tr>
<tr>
<td>Data density</td>
<td>(~1000) kbps/m(^2)</td>
</tr>
</tbody>
</table>

Table 1.2: Specification of the proposed UWB standard
1.4 Organization of the report

In this section each chapter in the report is briefly described. For those who are already familiar with the theory of data conversion and Sigma-Delta modulation, chapter 2 and 3 can be skipped.

Chapter 2

In this chapter the basic data conversion theory is introduced. Starting with the sampling theory it continues with describing an ideal converter and then the quantization error. Finally the chapter ends with showing high-speed converter solutions and their drawbacks.

Chapter 3

In this chapter the Sigma-Delta modulation is described. The structure is analyzed and the main ideas are described. By applying some of the knowledge from chapter 2 the advantages of the oversampling converter can be shown. Also non-idealities, as excess feedback delay and clock jitter are discussed, where the feedback delay is the main problem in this project.

Chapter 4

A high-level design of the converter is discussed in this chapter. First, the optimal coefficients are chosen for the proposed structure. Then the performance is estimated for different sampling frequencies and different excess feedback delays. Finally the high-level structure is specified.

Chapter 5

In chapter 4 different estimations are made for different sampling frequencies. It is assumed that the feedback delay will be important in the design, hence the design at transistor-level is in this chapter starting with the quantizer and the DAC. These blocks are in the feedback loop and are contributing to the total excess feedback delay. The design of these blocks is focused on high-speed.

Chapter 6

In chapter 4 optimal coefficients were calculated, which gives an optimal loop filter performance. This performance is mapped to the loop filter at transistor-level. The loop filter includes the integrators and the feedforward coefficients.
Chapter 7
In this chapter the simulation results are presented and analyzed for the complete Sigma-Delta modulator. Also some layout considerations are given, although the system is not implemented in layout.

Chapter 8
Finally the conclusions are drawn in this chapter, where also further improvements are discussed.
Chapter 2

Theory of data conversion

2.1 Introduction

In this chapter the basic knowledge of data conversion is introduced. There are two main types of converters, the Nyquist-rate converter and the oversampling converter. The Sigma-Delta oversampling converter (Sigma-Delta modulator) will be discussed in detail in the next chapter.

The theory of sampling will be discussed first. Then the behavior of an ideal converter is described, where it is shown that in an analog to digital converter an error called a quantization error is created. This error is then described in detail. Finally, some high-speed converter solutions are shown and their drawbacks compared to a Sigma-Delta modulator are given.

A more detailed description of the data conversion can be found in [8], where most of the following knowledge is discussed.

2.2 Sampling

In an analog to digital converter the discrete-time signal is obtained after sampling the continuous-time signal in known time steps. Mostly the time step is constant meaning a uniform sampling.

\[ x[n] = x(t)|_{t=nT}, n = \ldots, -2, -1, 0, -1, -2, \ldots \]  

(2.1)

The time step \( T \) between the samples is called a sampling period and the sampling frequency \( f_s \) is the inverse of a sampling period.

\[ f_s = \frac{1}{T} \]  

(2.2)
After sampling, the spectrum can be described by Poisson’s summation formula,

\[ x[\Omega] = \frac{1}{T} \sum_{k=-\infty}^{\infty} \left( \frac{\Omega - 2\pi k}{T} \right) \]  

(2.3)

where \( \Omega \) is the normalized frequency. In figure 2.2(b) (on the last page in this chapter) it is shown how the signal spectrum is copied to a periodical spectrum.

The sampling theorem says that by sampling with a sampling frequency equal to the Nyquist-frequency, that is two times higher than the signal bandwidth, the signal can be perfectly reconstructed. In reality the signal bandwidth, is not completely limited and frequencies outside the signal band exist. After sampling, signal bands will overlap and hence add distortion to the sampled signal, this is also called aliasing. An example is given in figure 2.2, where the input signal spectrum has some energy outside the signal band. This energy is after sampling fed into the signal band. After reconstructing by the pulse modulator, \( P(\omega) \), a signal spectrum, \( X_r(\omega) \), is created, which is not equal to \( X(\omega) \). To avoid this, the signal first has to be filtered through an anti-aliasing filter. A filter always has a limited steepness and that is why most of the Nyquist-rate converters are operating at a somewhat higher frequency than the Nyquist frequency.

### 2.3 Ideal converter

An ideal digital to analog (D/A) converter can be described by the following equation:

\[ V_{out} = V_{ref} \cdot (b_1 \cdot 2^{-1} + b_2 \cdot 2^{-2} + \cdots + b_N \cdot 2^{-N}) \]  

(2.4)

The output voltage is perfectly constructed in such a way that every bit, \( b_i \), contributes with a scaled version of the reference voltage. The least significant bit voltage is given by the reference voltage, \( V_{ref} \), and the number of bits, \( N \).

\[ V_{LSB} = \frac{V_{ref}}{2^N} \]  

(2.5)

A maximum output value of \( V_{ref} - V_{LSB} \) can be reached.

Although the output value in the D/A converter is perfectly defined, this is not the case in the analog to digital (A/D) converter. The output is here described by the following equation:

\[ V_{ref} \cdot (b_1 \cdot 2^{-1} + b_2 \cdot 2^{-2} + \cdots + b_N \cdot 2^{-N}) = V_{in} \pm V_x \]  

(2.6)

\[ -V_{LSB}/2 \leq V_x < V_{LSB}/2 \]  

(2.7)
Now a range of valid input values are producing the same digital word. This is called a quantization error and it will be discussed in the next section.

### 2.4 Quantization noise

The quantized signal, \( x_Q[n] \) can be described as the sum of the correct signal, \( x[n] \), and the quantization error, \( e_Q[n] \), shown in figure 2.1(a). Here \( \Delta \) is equal to \( V_{\text{LSB}} \).

\[
x_Q[n] = x[n] + e_Q[n] \quad (2.8)
\]

A more useful equation is given when expressing the quantization error as a function of the correct signal, shown in figure 2.1(b).

\[
e_Q[n] = x_Q[n] - x[n] \quad (2.9)
\]

![Figure 2.1: (a) Quantized signal as a function of the correct signal, (b) Quantization error as a function of the correct signal](image)

If we assume that the quantization error can be described as white noise, meaning that the quantization error is uniformly distributed between \( \pm V_{\text{LSB}}/2 \) then the noise power can be calculated as:

\[
P_e = \int_{-\infty}^{\infty} (x_Q - x)^2 f_e(x) \, dx = \frac{1}{V_{\text{LSB}}} \int_{-V_{\text{LSB}}/2}^{V_{\text{LSB}}/2} x^2 \, dx = \frac{V_{\text{LSB}}^2}{12} \quad (2.10)
\]

The signal-to-noise ratio, SNR, is defined as the ratio between the maximum input signal power and the noise power. Here the input signal is assumed to be sinusoidal, with a amplitude \( A \), to allow a simplified description.

\[
\text{SNR}_{\text{dB}} = 10 \cdot \log\left(\frac{\text{maximal sinus power}}{\text{noise power}}\right) = 10 \cdot \log\left(\frac{P_s}{P_e}\right) \quad (2.11)
\]
\[ P_s = \left( \frac{A}{\sqrt{2}} \right)^2 = \left( \frac{V_{\text{ref}}}{2\sqrt{2}} \right)^2 = \frac{V_{\text{LSB}}^2 2^{2N}}{8} \]  

(2.12)

\[ SNR_{dB} = 10 \cdot \log \left( \frac{3}{2} \cdot 2^{2N} \right) = 1.76 + 6.02N \text{ dB} \]  

(2.13)

This result shows that by increasing the number of bits the SNR can be increased by 6 dB/bit. Later on it will be shown that by using oversampling converters the \( SNR_{dB} \) is also including a second variable, the oversampling ratio, OSR. Higher SNR can then be achieved without increasing the number of bits.

### 2.5 A/D converters for high speed

Although there exist high-speed solutions, the oversampling converter is chosen in this project. The oversampling ratio is limited because of the limited switching frequency of the process technology, but together with noise shaping it can compete with other A/D converters through its advantages. In chapter 3, the Sigma-Delta modulator is described.

Just to get a brief insight to what the alternatives are, some of the high-speed converters are shortly described below.

Well known high-speed converters are: flash, two-step, interpolating, folding, pipelined and time-interleaved converters. They are reported in detail in [4].

The flash converter is using \( 2^N \) parallel comparators, which makes it very fast, but also extremely power consuming. Another popular converter is the two-step converter. As the name reveals, the parallel structure is divided into two. It consumes less power and area than the flash converter, but has a larger delay. The number of comparators can here be expressed by \( 2^{N+1} \). The high capacitive load at the input of a flash converter can be reduce by using an interpolating converter, which has a slightly lower power consumption. In the folding converter both folding and interpolation are used. The folding converter is similar to the two-step structure, hence both input capacitance and power consumption are reduced. Another converter is the pipeline converter, which in contrast to the two-step converter is not idling when the first stage has completed its work. This is good when a small area is required. The last converter is the time-interleave converter. This converter is operating in parallel, hence a very high speed can be reached. Since this requires very well timing, the requirements on the matching is extremely high.

Since a Sigma-Delta modulator only has a single path, the power consumption is low. Also the capacitance load at the input can be kept low and the timing is not crucial. Due to the feedback structure noise and distortion are filtered and hence the requirements on the circuitry are relaxed. This makes matching and accuracy of components less
critical, allowing a cheap and small, low power consuming integrated design, which is suitable for this project.
Figure 2.2: (a) Input signal spectrum, (b) Sampled signal spectrum \([\Omega]\), (c) Sampled signal spectrum \((\omega T)\), (d) Pulse modulator spectrum, (e) Reconstructed signal spectrum
Chapter 3

Theory of Sigma-Delta modulation

3.1 Introduction

Today the focus on reaching a high signal-to-noise ratio is common in analog to digital design. Here the oversampling converter, especially the Sigma-Delta modulator is playing an important role. They have several advantages; Firstly, such a converter relaxes the accuracy of the analog circuitry, which is being even more important now when low supply voltages are used leading to difficulties in designing complex structures. Secondly, the anti-aliasing filter, which is required to filter noise at frequencies higher than the signal band, is becoming less critical as the oversampling ratio is relaxing the order of the filter. Finally, the power consumption is reduced with respect to flash-like converters, as only one quantizer is needed. This chapter will discuss the theory of the Sigma-Delta modulation and it will be shown why the structure has all these advantages.

The chapter starts with showing the Sigma-Delta modulator system, including its internal structure. Then its key-ideas, oversampling and noise shaping is described and SNR estimations are made. The chapter continues with transferring the discrete-time modulator into a continuous-time modulator and it is explained why. Then the loop filter structure is shown. Finally, the chapter ends with showing the non-idealities of the Sigma-Delta modulator. The non-idealities included are: thermal noise, flicker noise, distortion, excess feedback delay and clock jitter.
3.2 Structure

In figure 3.1 the architecture of the Sigma-Delta modulator system is shown. There are two main blocks. The first block is the analog Sigma-Delta modulator, which outputs a bit stream at an oversampled frequency. The second block is the digital decimation filter, where out-of-band noise is filtered by a lowpass filter and where the oversampled signal is down-sampled to the Nyquist-frequency. In this project only the analog part is designed and the digital decimation filter is assumed not to be a speed-limiting factor.

![Diagram of Sigma-Delta modulator system](image)

Figure 3.1: Architecture of a Sigma-Delta modulator system

Figure 3.2: Structure of a Sigma-Delta modulator

First, the signal is sampled and held at the oversampling frequency, subtracted with the feedback voltage and then fed to the loop filter. In a discrete-time modulator this first part is often realized as a switched-capacitor circuitry. The loop filter is then filtering the signal before it reaches the quantizer. Here the analog signal is converted to a digital signal by a comparator, which compares the input voltage with a reference voltage and outputs a digital representation. For a one-bit
quantizer this is a single bit stream. In the feedback loop the DAC is converting the bit stream to an analog reference signal, which creates the feedback voltage. If we assume a zero feedback delay the input to the filter will be the difference between the input signal and the output signal, equal to the error created by the modulator. Hence, only the error is filtered.

There exist several Sigma-Delta structures; Different filters to control the shape of the noise transfer function, multi-bit quantizer to lower the quantization error, continuous- and discrete-time modulators. When increasing the order of the loop filter and the number of bits of the quantizer a higher SNR can be reached, but there are trade-offs. High-order filters are more complex and can have stability problems, and at low OSR high-order filters do not improve the SNR. A multi-bit quantizer increases the complexity of the circuitry and increases non-linearity, but reduces the amount of idle tones and the large amount of out-of-band quantization noise. In this project the one-bit quantizer is chosen, hence only this structure is discussed further on.

3.3 Oversampling

In this section the advantage of sampling at higher frequencies than the Nyquist frequency is described. We will see that by using oversampling the quantization noise is spread over a larger frequency range, and thereby increases the SNR by 3 dB for every doubling of sampling frequency. To obtain an even higher increase a feedback loop can be used and this is described in the next section.

The oversampling ratio is defined by the ratio of the sampling frequency, \( f_s \) and the Nyquist frequency, \( 2f_b \):

\[
OSR = \frac{f_s}{2f_b}
\]  

(3.1)

Due to oversampling the spectral density of the noise power is spread over half of the oversampling frequency range, \( \pm f_s/2 \), shown in figure 3.3 Noise outside the signal frequency band, \( f_b \), will be attenuated by the low pass filter in the decimation filter following the Sigma-Delta modulator. Integrating the noise power, found in equation 2.10, over the signal band yields,

\[
P_n = \int_{-f_b}^{f_b} S_e^2 \cdot |N_{TF}(z)|^2 \, df = \frac{2f_b}{f_s} P_e \\
= \frac{2f_b V^2_{LSB}}{f_s} = \frac{V^2_{LSB}}{12} \frac{1}{OSR}
\]  

(3.2)

where \( N_{TF}(z) \) is the noise transfer function equal to \( 1/\sqrt{OSR} \). If the result is compared with the quantization noise power, \( P_e \), in equation
the noise power, $P_n$, resulting from the oversampling converter is reduced by $1/\text{OSR}$. The SNR can now be described using the input power found in equation [2.12] as:

$$SNR_{dB} = 10 \cdot \log \left( \frac{3}{2} \cdot 2^{2N} \cdot \text{OSR} \right)$$

$$= 1.76 + 6.02N + 10 \cdot \log(\text{OSR}) \text{ dB}$$

(3.3)

The SNR will still increase by 6 dB per extra bit, but here also the OSR is a variable. For each doubling of sampling frequency the SNR is increased by 3 dB.

### 3.4 Noise shaping

In this section noise shaping by using a feedback loop will be described. Here the spectral density of the quantization noise is filtered, or "shaped" up in frequency by the loop filter, as shown in figure 3.4.

In figure 3.5 a discrete-time model of the modulator is shown. The signal transfer function, $S_{TF}$ and the noise transfer function, $N_{TF}$ is derived from the model in figure 3.5, assuming the quantizer to introduce an error, $N(z)$.

$$S_{TF}(z) = \frac{Y(z)}{U(z)} = \frac{H(z)}{1 + H(z)}$$

(3.4)

$$N_{TF}(z) = \frac{Y(z)}{N(z)} = \frac{1}{1 + H(z)}$$

(3.5)

The output is then described by the sum of the input signal and the error signal filtered through its respectively transfer function.

$$Y(z) = S_{TF}(z)U(z) + N_{TF}(z)N(z)$$

(3.6)
Figure 3.4: Quantization spectral density shaped by the loop filter, called noise shaping

Figure 3.5: Model of the discrete-time Sigma-Delta modulator

The model 3.5 can be linearised in order to make calculations simpler and is shown in figure 3.6. The quantizer is modeled as a constant gain, where a noise, $N(z)$, is added to the signal. The DAC is modeled as a constant gain.

Figure 3.6: Linearised model of a discrete-time Sigma-Delta modulator

Now the output can be described by:

$$Y(z) = \frac{cH(z)}{1 + cdH(z)} U(z) + \frac{1}{1 + cdH(z)} N(z) \quad (3.7)$$

If the effect is studied for relatively low frequencies the approximation $cdH(z) \gg 1$ is valid, because $H(z)$ is a lowpass filter, yielding the
following equation.

\[ Y(z) = \frac{1}{d} U(z) + \frac{1}{c d H(z)} N(z) \]  

(3.8)

Here the output is a scaled version of the input voltage. The noise is shaped up in frequency, since the transfer function is the inverse of \( H(z) \) equal to a high-pass filter.

Due to the feedback loop it is now possible to control the error. An ideal first-order noise shaping is equal to a first-order high-pass filter with a zero at dc in the noise transfer function, letting \( H(z) \) to be a discrete-time integrator.

\[ H(z) = \frac{1}{z - 1} \]  

(3.9)

The signal and noise transfer function can now be described as:

\[ S_{TF}(z) = z^{-1}, \quad N_{TF}(z) = 1 - z^{-1} \]  

(3.10)

Here the noise power, \( P_n \), can be calculated by filtering the quantization error, derived in chapter 2, through the noise transfer function, \( N_{TF}(z) \).

\[
P_n = \int_{-f_b}^{f_b} P_e \cdot |N_{TF}(z)|^2 \, df = \int_{-f_b}^{f_b} \frac{P_e}{f_s} \cdot |2 - 2z^{-1}|^2 \, df
\]

\[
= \frac{4P_e}{f_s} \int_{-f_b}^{f_b} 2 \sin\left(\frac{\pi f}{2f_s}\right)^2 \, df = \left(\frac{f_b}{f_s} \ll 1\right)\left(\frac{f_b}{f_s}\right)^3
\]

\[
\approx \frac{8P_e}{f_s} \int_{-f_b}^{f_b} \frac{\pi f}{2f_s} \, df = \frac{P_e \cdot \pi^2}{12} \left(\frac{2f_b}{f_s}\right)^3
\]

\[
= \frac{P_e \cdot \pi^2}{3} \left(\frac{1}{OSR}\right)^3 = \frac{V_{LSB}^2 \pi^2}{12} \left(\frac{1}{OSR}\right)^3
\]

Recalling the expression for the input power in equation 2.12 a SNR equation can be derived. Each doubling of the sampling frequency now increases the SNR by 9 dB according to \[4\]

\[
SNR_{dB} = 10 \cdot \log\left(\frac{3}{2} \cdot 2^{2N} \cdot \frac{3}{\pi^2} \cdot (OSR)^3\right)
\]

\[
= 1.76 + 6.02N - 5.17 + 30 \cdot \log(OSR) \text{ dB}
\]

A second-order Sigma-Delta modulator can be described as two first-order filters in series, yielding the following transfer function.

\[ H(z) = \frac{1}{(z - 1)^2} \]  

(3.12)
Also in this case the SNR is derived by similar calculations as in equation 3.11 and 2.11, which yields:

$$SNR_{dB} = 1.76 + 6.02N - 12.9 + 50 \cdot \log(OSR) \text{ dB} \quad (3.13)$$

Here a doubling of the sampling frequency increases the SNR by 15 dB. Note that the subtraction term in the equation is increasing with increased loop filter order, making a high-order less profitable at low OSR.

### 3.5 More accurate SNR estimation

The SNR estimation of the second-order Sigma-Delta modulator in equation 3.13 given in [4] is an overestimation and is not possible to reach in reality. It does not consider stability and limiting speed of integrators. Also the approximation $f_b << f_s$ is made, which is only partly true in this project since a rather low oversampling ratio will be used. In [10] optimal coefficients are used to ensure stability without the previous approximation. Here the SNR for a second-order one-bit Sigma-Delta modulator is expressed as:

$$SNR_{dB} = -19.4 + 50 \cdot \log(OSR) \text{ dB} \quad (3.14)$$

This means that equation 3.13 is overestimating the SNR by 14.3 dB.

### 3.6 Continuous-time Sigma-Delta modulator

The above described functionality is a discrete-time Sigma-Delta modulator, where the input signal is sampled and filtered through a switched-capacitor filter, quantized and then fed back to the filter. There exist another type of Sigma-Delta modulator and that is the continuous-time version. (See figure 3.7). Here the sampling is performed directly in front of the quantizer. The biggest difference is that the input signal is not directly sampled and therefore an anti-aliasing filter is not required. This filter can be very large for a steep roll-off when the sampling frequency or the oversampling ratio is low. Another advantage of a continuous-time Sigma-Delta modulator is less power consumption, which in a discrete-time Sigma-Delta modulator is increasing with the sampling frequency, leading to a very high power consumption at high sampling frequencies, due to the switch-capacitors circuitry. In the continuous-time Sigma-Delta modulator the power consumption is more determined by the SNR than by the sampling frequency, since
Chapter 3. Theory of Sigma-Delta modulation

Non-idealities often can be overcome by increasing the power consumption. In this project the sampling frequency is very high, but the OSR will be quite low and therefore a continuous-time Sigma-Delta modulator is preferable.

In this section the discrete-time Sigma-Delta modulator will be converted into a continuous-time Sigma-Delta modulator.

### 3.6.1 Linearised model

Although the model of the continuous-time Sigma-Delta modulator in figure 3.7 is different from the discrete-time model in figure 3.5, the linear model of the continuous Sigma-Delta modulator in figure 3.8 is equal to the linear model of the discrete-time Sigma-Delta modulator in figure 3.6. This allows us to map the discrete-time modulator to a continuous-time modulator and still get the same output.

![Figure 3.7: Model of a continuous-time Sigma-Delta modulator](image1)

![Figure 3.8: Linearised model of a continuous-time Sigma-Delta modulator](image2)

### 3.6.2 Non-linear model

In the linear model the quantizer and the DAC were described by only a constant gain factor. This is not true in reality, since both are introducing a phase-shift. The quantizer can be described by a gain, k, multiplied by an exponential term, which is introducing a phase-shift.
3.6. Continuous-time Sigma-Delta modulator

The phase-shift is due to the delay of the quantizer. In section 3.9, the total delay of the feedback loop, (including the quantizer delay), called the excess feedback delay, is derived. This is a non-ideality of the Sigma-Delta modulator and is specially important in this project. The transfer function of the quantizer can be expressed in the frequency-domain as:

\[ H_q(s) = k e^{s\theta} \]  

(3.15)

The DAC is ideally creating a perfectly rectangular pulse of magnitude 1 that last from \( \alpha \) to \( \beta \),

\[ h_{DAC}(t) = \begin{cases} 1 & \alpha \leq t < \beta, \ 0 \leq \alpha < \beta \leq 1 \\ 0 & \text{otherwise} \end{cases} \]  

(3.16)

which in the frequency-domain is equal to:

\[ H_{DAC}(s) = \frac{e^{-\alpha s} - e^{-\beta s}}{s} \]  

(3.17)

Here the delay is already included in the quantizer, hence the pulse is starting from \( \alpha = 0 \) and lasting to \( \beta = T_s \), yielding following equation:

\[ H_{DAC}(s) = \frac{1 - e^{-sT_s}}{s} \]  

(3.18)

This DAC is of the non-return-to-zero (NRZ) type, since it keeps its value through the whole sampling period. Another type is called return-to-zero (RZ), and then the \( T_s \) should be replaced by for example \( T_s/2 \). In the RZ case, asymmetry of DAC pulses due to the limiting rise-time are reduced. In an one-bit NRZ Sigma-Delta modulator the second bit of the bit stream "11" does not have any rise-time, since it holds the value of the feedback voltage. This gives rise to asymmetry in the feedback loop. In this project a low SNR is required and hence the asymmetry can be neglected, allowing a simpler design.

A second-order loop filter is containing two ideal integrators in series, with the unit-gain frequencies, \( w_{u1} \) and \( w_{u2} \) respectively.

\[ H_f(s) = \frac{w_{u1}w_{u2}}{s^2} \]  

(3.19)
The signal transfer function and the noise transfer function can from figure 3.9 be calculated by using the same method as in equation 3.4 and 3.5 to:

\[ S_{TF}(s) = \frac{H_f(s)H_q(s)}{1 + H_f(s)H_q(s)H_{DAC}(s)} \quad (3.20) \]

\[ N_{TF}(s) = \frac{1}{1 + H_f(s)H_q(s)H_{DAC}(s)} \quad (3.21) \]

The output at low frequencies is now described as:

\[ Y(s) \approx \frac{1}{H_{DAC}(s)} \cdot U(s) + \frac{1}{H_f(s)H_q(s)H_{DAC}(s)} \cdot N(s) \quad (3.22) \]

The position of the poles is now given by,

\[ 1 + ke^{s\theta} \left(1 - e^{-sT_s}\right) \left(\frac{w_{u1}w_{u2}}{s^2}\right) = 0 \quad (3.23) \]

which describes the characteristics of the Sigma-Delta modulator. Due to the exponential terms there exist no analytic solution. This is the reason why most analysis are done with the linear model, although in stability analysis the non-linear model still have to be used.

### 3.7 Feedforward compensation

![Block diagram of a second-order loop filter including feedforward coefficients](image)

In this section the loop filter structure is described. In figure 3.10 a second-order loop filter is shown, where \( H_1 \) and \( H_2 \) are integrators. To ensure stability in the loop filter feedforward coefficients, \( a_1 \) and \( a_2 \), are included. They will introduce zeros in the signal transfer function, making the roll-off first-order at high frequencies. Ideally this would mean a phase-shift of 90 degrees at the unity-gain frequency, but in reality it is lower. The phase-margin, \( \phi_m \) is defined as:

\[ \phi_m = 180 + \arg\left(\frac{X(s)}{E(s)}\right) \quad (3.24) \]
Although the phase-margin is ensuring a stable loop filter it does not tell if the complete modulator is stable. If the feedback was ideal it would have been the case, but this is not true. Due to the exponential terms describing the quantizer and DAC in equation 3.15 and 3.18 an analytical expression cannot be derived. To analyze the stability a root locus method can be applied.

In a second-order loop filter one zero is introduced. The loop filter transfer function will change to:

$$H_f(s) = \frac{a_1 w_u1}{s} + \frac{a_2 w_u1 w_u2}{s^2} = \frac{w_u1(a_2 w_u2 + a_1 s)}{s^2} \quad (3.25)$$

Here it can be seen that at low frequencies the roll-off is second-order and at high frequencies first-order, due to the poles and the zero placement. The placement of the zero is determined by the ratio of the both coefficients.

$$w_z = -\frac{a_2}{a_1} \cdot w_u2 \quad (3.26)$$

If the zero is placed higher in frequency, meaning a larger ratio between $a_2$ and $a_1$, the noise-shaping will be second-order for a larger frequency range, but the phase-margin will be lower.

### 3.8 Noise and distortion

Until now only quantization noise has been taken into account when estimating the SNR, but there are other noise sources to be aware of. Actually every transistor is a noise source creating a noise called circuit noise. This noise is mainly due to flicker and thermal noise in a CMOS transistor (see [4]).

The flicker noise is modeled as a voltage source in series with the gate,

$$V_g(f)^2 = \frac{K_f}{WLC_{ox}f} \quad (3.27)$$

where $K_f$ is a process dependent parameter and $C_{ox}$ is the gate capacitance.

The thermal noise is modeled as a current source between drain and source of the transistor. In the linear region it is expressed as:

$$I_d(f)^2 = \frac{4k_BT}{r_{ds}} \quad (3.28)$$

and in saturation it is expressed as,

$$I_d(f)^2 = 4k_BT\gamma g_m \quad (3.29)$$

where the correction factor, $\gamma$ in submicron transistors is equal to 1.3. In order to make the analysis of the circuit noise simpler the output
current source is referred to an equivalent input voltage source, by using the relation, \( I_d(f) = g_m V_{gs}(f) \). This gives the following equation for the thermal noise in saturation,

\[
V_g(f)^2 = 4k_B T \gamma \frac{1}{g_m}
\]  

(3.30)

allowing to model the thermal and flicker noise as a single noise source.

Also non-linearity is a noise source, hence it gives rise to distortion. Although a differential structure reduces even harmonic distortions, shown in appendix A, the third harmonic distortion can be significant. The non-linearity is mainly due to the non-linearity of the transconductance, \( g_m \), of the input transistor in the integrators.

To achieve a maximum performance of the Sigma-Delta modulator it is common to design the circuit noise and the distortion less contributing than the quantization noise, which would preserved the validity of the previously SNR calculations. The flicker noise can be limited by increasing the area, \( W L \), of the transistors, the thermal noise can be limited by increasing the transconductance, \( g_m \), and the distortion can be limited by a low input swing. Making the distortion contradictory to the circuit noise, since this type of noise can be limited by having a large input swing.

3.9 Excess feedback loop-delay

The ideal Sigma-Delta modulator has a zero delay from the time the quantizer is sampling a signal to the time when the signal is seen on the output of the DAC. At low sampling frequencies using relatively fast circuits this approximation can be made, but not at high sampling frequencies when the excess feedback loop-delay, \( t_d \), is exceeding a significant part of one sampling period. At these large delays the SNR degrades a lot and the system could be unstable, caused by the extra order introduced in the loop filter reported in [9]. There are two options here, either not to care about it and lose some performance or to use special compensation methods. In [3] and [9] two compensation structures are reported, one-delay and multi-feedback respectively. These structures improve the stability and the SNR of the modulator. In this section the effect of the feedback delay is briefly discussed.

Due to the feedback delay the DAC pulse is shifted in time, shown in figure 3.11, and is described as,

\[
h_{DAC,(t_d,1+t_d)}(t) = h_{DAC,(t_d,1)}(t) + h_{DAC,(0,t_d)}(t - T_s)
\]  

(3.31)

which can be transformed to the frequency-domain by using equation 3.17

\[
H_{DAC,(t_d,1+t_d)}(s) = \frac{1 - e^{-sT_s}}{s} e^{-st_d}
\]  

(3.32)
3.10 Clock jitter

Another non-ideality that is limiting the SNR of the Sigma-Delta modulator is clock jitter, which is the same as statistical variations in sampling moments. Since the sampling is taking place just before the quantizer in the continuous-time modulator, the clock jitter disturbs the sum of the input signal and the quantization noise, compared with a discrete-time modulator where it only disturbs the input signal. A continuous-time modulator is hence more sensitive to clock jitter than the discrete-time counterpart (see [6]). Since the sampling is taking place outside the loop the clock jitter from the sampler is not filtered by the loop. A calculation of the SNR caused by the clock jitter is shown in the following equation, (see [2])

\[
\text{SNR} = 10 \log \left( \frac{1}{16 \cdot \text{OSR} \cdot f_b^2 \sigma_j^2} \right)
\]  \hspace{1cm} (3.34)

where the clock jitter standard deviation, \( \sigma_j \), is in the picosecond range and is dependent on the performance of the clock oscillator circuitry. If the substrate noise is high the value can go up to several tens of picoseconds. The crystal itself is not contributing to the clock jitter.

Figure 3.11: NRZ-DAC (a) Ideal DAC pulse, (b) Delayed DAC pulse

Here the phase-shift \( \theta \) cause by the quantizer, described in section 3.6.2, is included in the feedback delay, \( t_f \). The loop characteristic is now changed to:

\[
1 + ke^{st_f} \left( \frac{1 - e^{-sT_s}}{s} \right) \left( \frac{w_{u1}w_{u2}}{s^2} \right) = 0
\]  \hspace{1cm} (3.33)
Chapter 4

High-level design

4.1 Introduction

In this chapter a high-level simulation is estimating the performance of the Sigma-Delta modulator. With given coefficients internal signals and output bit streams can be simulated, to allow a comparison between the high-level model and the transistor-level model, and to estimate the signal-to-noise ratio. Here the high-level simulation tools are only simulating some of the non-idealities in the Sigma-Delta modulator, such as the quantization noise and the excess feedback delay. This could give an overestimation of the SNR unless the converter is designed in such a way that the quantization noise limits the performance. The tools applied in the high-level simulations are Signify™, MATLAB® and Cadence®.

As described in chapter 3 there are several Sigma-Delta structures to choose from. To reach a high SNR a high-order, multi-bit structure, can be used. In this project a quite low SNR of 30 dB is required and hence a low OSR. At low OSR the SNR does not profit from a high-order structure. Also the capacitive load in the very time-critical comparator has to be low, this load is increasing with increasing circuit complexity and it is very critical for high speed. Therefore a simple structure is chosen with sufficiently high oversampling-ratio. The upper speed-limit is determined by the process technology. In the following analysis the feedback delay is assumed to be a limiting factor, since experience tells us that the speed of the CMOS090 transistors will be critical for reaching a sampling frequency in the gigahertz range.

In the following section the optimal coefficients for the Sigma-Delta modulator are calculated to make a performance estimation in section 4.3 possible. Some of the coefficients used are determined in simulations later in the report. In section 4.3 the performance is analyzed for
different sampling frequencies. First the maximum possible signal-to-noise ratios for three different sampling frequencies are given, then the impact of excess feedback delay is shown. This is followed by section 4.4 where the structure of each block in the modulator is chosen.

4.2 Determine coefficients

In chapter 3 it was shown that there are some coefficients in the modulator that have to be specified. Also several others exist. They are; Input signal amplitude, limiting levels in the integrators, feedforward coefficients and unity-gain frequencies of the integrators. Usually the input signal amplitude is specified in the project specification, but since the UWB communication standard is not settled yet it was chosen during the design. Since limiting levels and feedforward coefficients are based on experience and calculations, and optimized in simulations they are determined in chapter 6 where the loop filter is designed at transistor-level. In table 4.1 the chosen coefficients are summarized.

<table>
<thead>
<tr>
<th>Input signal amplitude, $\hat{v}_{in}$</th>
<th>0.3 V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Limiting level, $l_1$</td>
<td>0.4 V</td>
</tr>
<tr>
<td>Limiting level, $l_2$</td>
<td>0.4 V</td>
</tr>
<tr>
<td>Feedforward coefficient, $a_1$</td>
<td>1</td>
</tr>
<tr>
<td>Feedforward coefficient, $a_2$</td>
<td>1.4</td>
</tr>
</tbody>
</table>

Table 4.1: Modulator coefficients

The optimal unity-gain frequencies are determined by the sampling frequency and the signal bandwidth. In chapter 1 the signal bandwidth was specified to 264 MHz. Three different sampling frequencies have been chosen since we do not know the minimum feedback delay and its effect on the SNR. The zero-delay single feedback second-order modulator was chosen, hence the optimal unity-gain frequencies are not affected by the feedback delay. To calculate the optimal unity-gain frequencies of the integrators a high-level simulation tool is used. In table 4.2 the unity-gain frequencies are shown. Using these unity-gain frequencies together with the other coefficients, in table 4.1 a high-level structure can be mapped to a transistor-level structure. An optimal bit
stream output from the high-level simulations would be a bit stream output as the one shown in figure 4.1 where a zero feedback delay is applied. This ideal output will change due to the non-idealities in the Sigma-Delta modulator. One of the non-idealities is limited DC-gain of the integrators, which is limiting the low frequency noise-shaping, another non-ideality is the excess feedback delay that gives the flat curve at higher frequencies an overshoot that is moving closer to the signal frequency band with increasing delay.

Figure 4.1: Fourier transform of a bit stream output from a Sigma-Delta modulator with optimum coefficients sampled at 6.336 GHz and with a zero feedback delay

4.3 Performance estimation

In order to aim at a SNR of 30 dB a high OSR is not needed. Oversampling ratios between 8 and 16 will be studied. Here a third-order Sigma-Delta modulator does not gain over the second-order Sigma-Delta modulator, that is why the latter one was chosen. In table 4.3 the ideal SNR results are shown for different oversampling ratios. At a sampling frequency of 6.336 GHz the required SNR of 30 dB can be reached, but this is not including the feedback delay which is assumed to be significant.

<table>
<thead>
<tr>
<th>Frequency</th>
<th>Period</th>
<th>OSR</th>
<th>$\text{SNR}_{\text{max}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>8.448 GHz</td>
<td>118 ps</td>
<td>16</td>
<td>41 dB</td>
</tr>
<tr>
<td>6.336 GHz</td>
<td>158 ps</td>
<td>12</td>
<td>36 dB</td>
</tr>
<tr>
<td>4.224 GHz</td>
<td>236 ps</td>
<td>8</td>
<td>25 dB</td>
</tr>
</tbody>
</table>

Table 4.3: SNR of second-order Sigma-Delta modulator
In table 4.4 the effect of feedback delay is shown. A delay of 2/3 of a sampling period, 105 ps, at 6.336 GHz give rise to a SNR drop of 12 dB and would at this frequency limit the SNR to 24 dB. To reach the required SNR of 30 dB a maximum delay of 40 ps is allowed. At a frequency of 8.448 GHz the maximum delay is 59 ps. Since a delay at 2/3 of a sampling period is very close to instability the following analysis will assume a limiting delay of a half sampling period. In [9] it was reported that the limit for stability is 38 % of one sampling period in a second-order continuous-time Sigma-Delta modulator, but in high-level simulations using Signify™ the tendency of instability came at larger delays.

<table>
<thead>
<tr>
<th>Delay</th>
<th>SNR change</th>
</tr>
</thead>
<tbody>
<tr>
<td>T</td>
<td>Instable</td>
</tr>
<tr>
<td>2T/3</td>
<td>-12 dB</td>
</tr>
<tr>
<td>T/2</td>
<td>-11 dB</td>
</tr>
<tr>
<td>T/3</td>
<td>-9 dB</td>
</tr>
<tr>
<td>T/4</td>
<td>-6 dB</td>
</tr>
<tr>
<td>T/5</td>
<td>-3 dB</td>
</tr>
</tbody>
</table>

Table 4.4: SNR decrease for different delays, where T is the sampling period

In table 4.5 the maximum SNR at different delays is summarized. Only the stable delays are shown.

<table>
<thead>
<tr>
<th>(a) SNR_{\text{max}}</th>
<th>Delay</th>
</tr>
</thead>
<tbody>
<tr>
<td>30 dB</td>
<td>59 ps</td>
</tr>
<tr>
<td>32 dB</td>
<td>39 ps</td>
</tr>
<tr>
<td>35 dB</td>
<td>29 ps</td>
</tr>
<tr>
<td>38 dB</td>
<td>24 ps</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>(b) SNR_{\text{max}}</th>
<th>Delay</th>
</tr>
</thead>
<tbody>
<tr>
<td>25 dB</td>
<td>79 ps</td>
</tr>
<tr>
<td>27 dB</td>
<td>53 ps</td>
</tr>
<tr>
<td>30 dB</td>
<td>39 ps</td>
</tr>
<tr>
<td>33 dB</td>
<td>32 ps</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>(c) SNR_{\text{max}}</th>
<th>Delay</th>
</tr>
</thead>
<tbody>
<tr>
<td>14 dB</td>
<td>118 ps</td>
</tr>
<tr>
<td>16 dB</td>
<td>79 ps</td>
</tr>
<tr>
<td>19 dB</td>
<td>59 ps</td>
</tr>
<tr>
<td>22 dB</td>
<td>47 ps</td>
</tr>
</tbody>
</table>

Table 4.5: Maximum SNR for different delays at (a) 8.448 GHz, (b) 6.336 GHz, (c) 4.224 GHz

From table 4.5 it can be concluded that to reach 30 dB of SNR the worst case solution would be to design a structure where the sampling frequency is 8.448 GHz and the delay is not exceeding 59 ps. The best solution would be to design a structure where the sampling frequency is 6.336 GHz and the delay is not exceeding 39 ps. If the delay is larger than 59 ps the required SNR is no longer possible to reach. What are the alternatives then?
The problem occurring when having a large delay close to one sampling period is that our zero-delay model is not valid anymore. To allow a large delay the model must be restated for example by using a compensation method discussed in chapter 3, but there are problems with these methods such as sensitivity to mismatches. The other solution is to lower the requirements and focus on trying to maximize the SNR for a zero-delay Sigma-Delta modulator. If the second approach is chosen the delay will determine the suitable sampling frequency. If the delay is 79 ps a sampling frequency of 6.336 GHz would be preferable, or if it is 118 ps the choice would be a sampling frequency of 4.224 GHz to preserve stability. Now the maximum SNR will be 25 dB or 14 dB respectively, a lot lower than the required SNR. Although the second approach is not reaching the requirement in the specification it has been chosen in this project.

Hence, our focus will be to limit the feedback delay. In chapter 5 the feedback loop, which is containing the quantizer and the DAC, is designed at transistor-level and is optimized for high speed. Since the loop filter is not included in the feedback loop it does not affect the feedback delay. It is instead designed to achieve sufficient SNR at a low power consumption.

4.4 Building blocks

In this section all the building blocks of the Sigma-Delta modulator are chosen. They are: The integrators, the feedforward coefficients, the quantizer, the DAC and the common-mode feedback. Here the focus is on high-speed and low power consumption with low noise and linearity requirements.

A fully differential solution is chosen, since this solution reduces even harmonic distortion and common-mode noise, and increase the maximum achievable voltage swings. The only drawbacks are increased power consumption and area, but those can be suppressed due to the lower noise (see [7]).

4.4.1 Integrator

To realize the integrator at transistor-level several alternatives exist, although the only existing integrating component on-chip is the capacitor. Figure 4.2 shows three different alternatives which will be discussed. They are: the opamp-RC integrator, the OTA-RC integrator and the $G_m$-C integrator.

The opamp-RC integrator shown in figure 4.2(a) has the advantage of high linearity if linear resistors exist. The drawback of this structure is that it requires low output impedance due to the resistive load at
the output when cascading several integrators. This would require a two stage opamp, which uses two Miller capacitances when connected differentially, to ensure stability.

The second solution is a transconductance-C integrator shown in figure 4.2(c), where the transconductance is simply a differential pair. This would be least power consuming and also the fastest choice. The drawback is nonlinearity, due to the nonlinearity of the CMOS transistors. The linearity could be improved by degeneration, done by inserting resistances at the sources of the differential pair. A $g_m$-cell with degeneration is shown in figure 4.3.

Figure 4.2: (a) Opamp-RC integrator, (b) OTA-RC integrator, (c) $G_m$-C integrator

Figure 4.3: $g_m$-cell with degeneration
The third and last one is a combination of the two first solutions shown in figure 4.2(b). This structure uses an opamp-RC integrator at the input and transconductance-C integrators internally. A single stage opamp (OTA) can be used, because of the capacitive load at the output. The drawback is noise and power, because of the large resistance, \( R \), or transconductance, \( G_m \), required to have a low input impedance. \( (G_mR >> 1) \).

In this project speed is more important than linearity, therefore the \( G_m \)-C integrator in figure 4.2(c) is most suitable.

### 4.4.2 Feedforward coefficients

Also the feedforward coefficients are implemented as a differential pair. Their inputs are the voltages over the integration capacitance, \( C_1 \) and \( C_2 \), and they output a scaled current, according to the optimal feedforward ratio, \( a_2/a_1 \), fed by the quantizer.

The feedforward stages are inside the Sigma-Delta loop, where the noise and the distortion are second-order filtered. Simulations will show whether linearity compensation, using degeneration, is needed.

### 4.4.3 Quantizer

The loop filter including the integrators and the feedforward coefficients is followed by the quantizer. It is built of a comparator using a clocked-latch structure and two d flip-flops, one for each output node. The d flip-flop is built in a true-single phase clocked (TSPC) logic for high-speed decisions.

### 4.4.4 DAC

A non-return-to-zero, NRZ, DAC structure is chosen, since the low SNR will not benefit remarkably from a RZ structure. This means that the DAC should output a pulse during the complete sampling period and therefore it does not need an extra clock. The bit steam output of the d flip-flop should be seen directly on the current output of the DAC, hence the DAC is realized as a differential pair that is working as a switch. Since this block is outside the loop noise and distortion are directly seen at the output of the modulator.

### 4.4.5 CMFB

In a fully differential structure, as the one chosen in this project, a common-mode feedback structure has to be implemented to control the common-mode level. In this design the CMFB is included in the integrators.
4.4.6 Complete system

In figure 4.4 the complete Sigma-Delta structure is shown.

Figure 4.4: The Sigma-Delta structure.

The following chapters will describe the design of each of the blocks at transistor level.
Chapter 5

Quantizer and DAC design

5.1 Introduction

The design at transistor-level design is starting in this chapter. The tools being used are Promost\textsuperscript{TM}, MATLAB\textsuperscript{®} and Cadence\textsuperscript{®}.

This chapter is describing the design of the quantizer and the DAC. The design is divided into blocks shown in figure[5.1] starting with the comparator and followed by the d flip-flop. The DAC is included in the end of the chapter to allow a simulation of the complete feedback delay. Last, the effect of the clock jitter is analyzed.

The high-level simulations indicated that the feedback delay is very critical for the SNR at the proposed high sampling frequencies. Due to the low SNR requirement the following design is focusing more on speed than on linearity. Often linearity compensation structures degrade the speed and they are avoided if possible.

Figure 5.1: Structure of the quantizer
5.2 Comparator

One of the most critical blocks for high-speed is the comparator. This block compares two signals and outputs a high or low value according to the sign of the difference between the two input signals. In a latch-type of comparator, a switch is included between the output nodes of the comparator, which then acts both as a reset-switch and a sampling-switch. A maximum speed is hereby determined by two factors; decision-time, and reset-time. In the next section the structure is described in detail.

5.2.1 Structure

In a simple latched comparator, as the one shown in figure 5.2, a current is pulled from the input nodes by the feedforward coefficients (designed in chapter 6). Transistor M1 and M2 are hence supplying both current to the comparator and to the feedforward coefficients. To shield the input from the output, cascaded transistors M3 and M4 are used. In the bottom two latch connected transistors, M5 and M6, are situated, which are of n-type for an improvement of speed. Between the output nodes a transmission gate is connected, which gates are clocked. When the clock is high the comparator is in reset-mode and the value of the output node will discharge to the common-mode output level. When the clock is low the latch is active and makes a decision. Transistor M7 and M8 are diode-connected to the output nodes in order to limit the output swing.

During the decision one of the output nodes goes to a high value and the other one goes to a low value. When one of transistor M5 or M6 reaches cut-off voltage the complete supply voltage drop would be over that transistor, but here transistor M7 and M8 are included that limits the output swing. When the voltage of one output node is increasing one of transistor M7 or M8 opens and starts to pull current, hence limits the voltage swing to be less than the supply voltage. It is important to limit the output swing, because otherwise the current sources, M1 and M2, would not be in saturation and this would influence both the comparator and the feedforward coefficients.

5.2.2 Optimize for high-speed

In order to reach high-speed the decision-time must be minimized to reduce delay, and the reset-time must be minimized to increase sampling frequency. We will see that those two factors contradict to each other. Limiting the decision-time means reducing capacitance and increasing transconductance, and limiting the reset-time means increasing transistor width and thereby increasing capacitance. Although they
5.2. Comparator

Figure 5.2: The biasing-levels and the output voltage swing (left). The schematic of the comparator (middle). The voltage change during the decision- and the reset-time. Clk2 controls the d flip-flops which is the following stages.

seem to be contradictory this is not completely true. In the latch the decision-time is dependent on the capacitive load from every transistor connected to the output node and the transconductance of the latch transistors, but the reset-time is determined by the resistance of the transmission gate connected between the output nodes. This resistance have to be sufficient low to discharge the output nodes to their dc-level during a half clock period. The design can now be divided into two parts. A chosen sampling frequency, $f_s$, that determines the minimum width of the transmission gate and a minimum delay that is determined by the transconductance of the latch transistor and the capacitive load at the output nodes. Although they are not independent of each other the analysis starts with the decision-time.

**Decision-time**

As mentioned the decision-time is determined by the transconductance, $g_{m5}$, of the latch transistors, M5 and M6, and by the capacitive load, $C_{out}$ at the output nodes. To analyze the descision an unity-gain frequency for a single transistor is derived in appendix A.2

$$f_u = \frac{g_{m5}}{2\pi \cdot C_{outm}}$$  \hspace{1cm} (5.1)

where the capacitive load, $C_{outm}$, is determined by transistor Mnp1, Mpp1, M3, M5, M6, M7, M8 and the load shown in figure 5.3. This
yields a total capacitance at output node m of:

\[ C_{\text{outm}} = C_{DB,M5} + 2 \cdot C_{DG,M5} + C_{GS,M6} + C_{GB,M6} \]
\[ + C_{DB,M3} + C_{DG,M3} + C_{DB,Mnp1} + 2 \cdot C_{DG,Mnp1} \]
\[ + C_{SB,Mpp1} + 2 \cdot C_{SG;Mpp1} + C_{GS,M7} + C_{GB,M7} + C_{LOAD} \]

Due to the Miller effect \( C_{DG,M5}, C_{SG,Mpp1} \) and \( C_{DG,Mpp1} \) are doubled.

This result gives us a ratio to optimize, high transconductance at the same time as low capacitive load.

First, scaling can be used to reduce the effect from the load capacitance, which is determined on the following d flip-flop stage. By scaling up the supply current and transistor widths in the comparator the speed remains the same, since the capacitance and the transconductance are both proportional to the width of the transistors (\( \sim W \)). Using this, the load capacitance, \( C_{LOAD} \) (capacitance from the next stage), can be neglected after a certain scaling, since this capacitance is not scaled with the comparator. Secondly, optimization of transistor width and biasing levels is maximizing the \( g_m/C \) ratio, shown in equation 5.3. The \( g_m/C \) ratio is proportional to:

\[ \frac{g_m}{C_{\text{outm}}} \sim \frac{W_5 V_{GT5}}{W_3 + W_5 + W_7 + W_{np} + W_{pp}} \]

According to this the maximum unity-gain frequency is achieved if the latch transistors width are increased and the common-mode output level is high. At high gate voltages the current equation in saturation is changed from A.4 to a linear dependent current given by,

\[ I_{DS5} = k \frac{W_5}{2L_5} \cdot V_{GT5} = k \frac{W_5}{2L_5} \cdot (V_{GS5} - V_{Tn}) = k \frac{W_5}{2L_5} \cdot (V_{DS5opt} - V_{Tn}) \]
since the current gain is limited due to high-field effects. In newer process technologies this gate voltage is lower, since the minimum length is shrinking. The transconductance is now proportional to the width, since the transconductance is given by equation A.11 and this yields the following relationship:

\[ \frac{g_{m5}}{C_{outm}} \sim \frac{W_5}{W_3 + W_5 + W_7 + W_{np} + W_{pp}} \]  

(5.5)

An even further increase of current would now not speed up the circuit, since it scales every transistor and therefore do not increase the unity-gain frequency according to equation [5.5]. Here only the capacitance from transistor M3 can be limited, through an optimal division of voltage between transistor M1 and M3. Preferably the voltage drop over M1 is minimized and the drop over M3 is maximized. This would also maximize \( V_{GT3} \) due to the saturation requirement, which then gives the minimum width, \( W_3 \). When maximizing \( V_{DS3} \) the minimal voltage swing at the output nodes have to be taken into account. The maximal \( V_{DS3} \) is now given by,

\[ V_{DS3max} = V_{dd} - V_{DS1min} - V_{sw} - V_{DS5opt} \geq V_{GT3max} \]  

(5.6)

where \( V_{dd} \) is the power supply, \( V_{DS1min} \) is the minimal voltage over the current source, \( V_{sw} \) is the minimum voltage swing at the output node and \( V_{DS5opt} \) is the optimal common-mode output voltage derived in equation [5.4]. When minimizing \( V_{DS1min} \) the capacitive load at the output node is increasing and it cannot be too large, hence it will introduce memory effects if it is not reset properly. To choose the output voltage swing, the following stage has to be considered. The d flip-flop is designed in the next section. The last term in equation [5.6] is process dependent and is derived through simulations, where the drain-source current is plotted as a function of \( V_{GS} \). The voltage \( V_{DS3opt} \) is given when the saturation current goes from square rise to linear rise and is derived through simulations.

Here transistor M7 and the transmission gate were ignored, since simulation has shown that transistor M7 is not contributing considerably to the capacitive load and the transmission gate is not limited by the biasing levels but is optimized for a given sampling frequency.

Because of the complex behavior of the CMOS090 transistor these calculations are just approximative and simulations will give the most optimal design.

To calculate the expected decision-time the charging is divided into two parts. First, the current is not limiting and the voltage is rising exponentially. Then, when the current has started to be limiting, the voltage is then rising linearly and this is called slewing. The exponential voltage rise and the time can be modeled by these equations,

\[ \Delta v_{out} = \Delta v_{in} \cdot e^{\frac{t}{\tau}} \]  

(5.7)
\[ t = \tau \cdot \ln\left( \frac{\Delta v_{out}}{\Delta v_{in}} \right) \] (5.8)

where \( \tau \) is the time-constant, \( 2\pi/f_u \), here equal to \( 4C_{out}/g_{m,M5} \). This ratio is four times larger for the latch connected transistors than for a single transistor shown in appendix [A.2] since the capacitance is doubled and the transconductance is halved. \( \Delta v_{in} \) is the voltage difference between the output nodes shortly after reset, equal to \( 2\Delta i/g_{m,M5} \). The equations for the output voltage change and the time during slewing are:

\[ \Delta v_{out} = t \cdot \frac{I_{av}}{C_{outm}} \] (5.9)

\[ t = \frac{C_{out} \cdot \Delta v_{out}}{I_{av}} \] (5.10)

At the moment the circuit is switched from reset-mode to active-mode the comparator acts exponential. When the output node reaches cut-off voltage for either M5 or M6 the comparator enters slewing. This means that the decision has been made and the output no longer is determined by the input. To make a new decision the circuit has to reset.

While the voltage at output node m in figure 5.2 is increasing, the transistor M1 and M3 first enters linear region and the current is starting to decrease. Finally when the voltage is close to \( V_{DD} \), M3 completely turns off. A solution to avoid this is by using diode-connected transistors, M7 and M8, which limit the output voltage. The problem with this solution is the increased capacitive load on the output node and the current leakage, hence it lowers the gain and the speed of the latch. The simulations has shown that the transistor size of the diodes is small and is contributing with a small capacitance. To avoid the leakage the transistor source can be connected to a higher voltage, which is making it to remain in cut-off during reset, but then the diodes must be larger to limit the voltage swing to the same level. In simulations this solution did not improve the results much, that is why the sources of transistor M7 and M8 are still connected to ground. At the falling node the current is staying constant and there will therefore be a faster fall-time.

A typical output of a decision is shown in figure 5.4. First, there is an exponential rise and then after a certain time it starts to rise linearly. This rise is limited by the diodes.

**Reset-time**

The choice of the transmission gate width is much trickier to describe mathematically. Here the width was chosen through simulations. The size is determined on the bias current, the maximal input current swing and the chosen sampling frequency.
Figure 5.4: Comparator response during decision-time. Solid line shows rising node and dashed line shows falling node.

5.3 D flip-flop

The second block is a buffer stage which drives the output and the DAC in the converter. The output should be a full period, meaning that the output keeps its value during the reset of the comparator. This can be made by a regular d flip-flop, but it would be too slow at the proposed high sampling frequencies. A true-single-phase clocked (TSPC), structure is instead used to allow high speeds.

5.3.1 Structure

In figure 5.5 the TSPC d flip-flop structure is shown. It is connected to act as a negative edge-triggered d flip-flop. The structure is built of three stages. The first stage is in fact a clocked inverter, which at the positive edge of the clock is precharging the inverted value of the input, D, at the gate-capacitance of transistor M5. At the negative edge, transistor M2 turns off and the drain keeps its charge at node x. The voltage on node x either opens or closes transistor M5. At the positive edge of the clock, transistor M4 opens and resets node y. When the negative edge arises, transistor M6 opens and then the value of node x determines whether node y should keep its low value or if it should be charged through transistor M6. The third stage is another clocked inverter. During the hold phase when the clock is high, transistor M9 is opened and transistor M7 and M8 are closed holding the precharged value at node z. Once the negative edge arrives a new value is charged to node z, which is the inverted value of node y. The fourth and last
stage is an added inverter to boost the output of node z.

The advantage of this structure is that it is race free, signals cannot propagate through the whole structure during one clock phase and it needs only one clock phase. The drawback is a rather large number of transistors and a high load at the clock compared to other structures. This will not be a problem and therefore this structure is chosen in this project.

![Figure 5.5: The schematic of the TSPC d flip-flop, where φ is equal to clk2](image)

The clock which drives the clocked transistors is a delayed clock compared to the clock which is driving the comparator. The delay between the clocks is given by the required time for a decision in the comparator latch. This can be simulated and optimized for the whole feedback loop.

The common-mode input level at the d flip-flop is situated a bit different from the output of the comparator in order to increase the probability that a decision is made. This will increase the numbers of wrongly taken decisions, which means that the output bits are either 11 or 00, but it will limit the probability for a non-taken decision. Such a decision would degrade the performance much more than a wrongly taken decision, since it easily can be taken care of by the digital signal processor. The choice between 11 or 00 output for a non-taken decision has influence on the DAC, which will be designed in the next section.

In the design phase the structure was designed to have as short delay as possible. Hence, the capacitive load in the signal path was kept low. Only transistor M6 is isolated from the signal path and was therefore made quite large to increase the current through the second stage and hence the speed of the circuit. Also transistor M4 is given a large width compared to the others, since it have to discharge node y very fast.
5.4 DAC

In this section the digital to analog converter will be described. This block feeds the output signal from the Sigma-Delta modulator back to the integrator.

5.4.1 Structure

This structure is made very simple, since the linearity requirements are quite low. In figure 5.6 the DAC is shown, which is just an ordinary gm-cell. It has digital inputs and could therefore be called a switch. Transistor M3 acts as a current source and transistors M1 and M2 are switches. Either the current from M3 goes completely through M1 or M2.

![Figure 5.6: Schematic of the DAC](image)

The outputs are connected to the first integrator outputs, which is supplying the current to the DAC circuit. The DAC contributes to the current through the capacitance connected between the output nodes in figure 5.7. The current through integration capacitance one can be

![Figure 5.7: Principle structure of the first integrator and the DAC](image)
described as,

\[ I_{C_1} = G_m v_{in} \pm \frac{I_{DAC}}{2} \]  

(5.11)

where \( G_m \) is half of the transconductance, \( g_m \), of a single transistor, since the current created is due to the differential input. To avoid overloading the integrators the DAC current should be chosen so that the output from the DAC toggles between \( \pm 2v_{in,max}^{rms} \). This will make a 3 dB drop on the output voltage gain of the complete modulator. Since the DAC output is working in the current domain, the output is restated to toggle between \( \pm 2G_m v_{in,max}^{rms} \). The DAC current source can now be expressed as:

\[ I_{DAC} = 4 \cdot G_m v_{in,max}^{rms} \]  

(5.12)

Since a non-taken decision from the d flip-flop is either 11 or 00, high or low outputs at both the positive and negative output node, the best choice considering the DAC is to make the d flip-flop to take a 11 decision when it cannot determine the difference between the inputs from the comparator. A 00 input to the DAC is cutting off the current source M3 in figure 5.6 which should be avoided.

![Figure 5.8: Switching moment at the outputs of the d flip-flops, B0 and B1](image)

The DAC should be biased so that transistor M1 and M2 both are in saturation during the switching moment, shown in figure 5.8 because simulation showed peaks in the current output when they were below the saturation voltage. The switching voltage is chosen by the following equation,

\[ V_{swl} > V_{DS3} + V_{Tn} \geq 600 \text{ mV} \]  

(5.13)

where transistor M3 is in saturation biased at \( V_{DS3} \) of 300 mV and the threshold voltage of transistor M1, \( V_{Tn} \approx 300 \text{ mV} \).

### 5.5 Clock jitter

In chapter 3 the clock jitter was expressed in equation 3.34. A signal to jitter-noise-ratio was found to be equal to: 37.4 dB, 35.7 dB and
34.4 dB, for 8, 12 and 16 times oversampling respectively, when $\sigma_j = 4.5 \text{ ps}$. This is close to the required SNR, hence a better clock oscillator achieving a lower value of $\sigma_j$ would preferably be used.
Chapter 6

Loop filter

6.1 Introduction

In this chapter the loop filter is designed. It has been shown in chapter 3 that the signal transfer function is a lowpass filter and the noise transfer function is a highpass filter, hence the noise is shaped up in frequency and is then limited in the signal band. To design this loop properly the optimal coefficients calculated in chapter 4 are applied. This will give an optimal loop filter characteristic.

First the structure of the loop filter and its ideal transfer function will be described. This is then followed by a description on the non-ideal behavior of the integrators to get a proper knowledge about the design considerations. The integrators are then designed at transistor-level, where non-idealities as noise and distortion is analyzed. This is followed by the design of the feedforward coefficients, which then completes the loop filter. In the last section a complete simulation of the loop filter is done.

6.2 Structure

As decided in chapter 4 the second-order loop filter is designed by two transconductance-C integrators in series, with a feedforward coefficient connected to their outputs. In section 6.6 the feedforward coefficients will be designed. Figure 6.1 is showing the complete structure of the loop filter. In equation 3.25 the transfer function was given for the loop filter including the feedforward coefficients. This can now be rewritten as,

\[ H_f(s) = \frac{G_{m1}}{C_1} \left( \frac{G_{m3} G_{m2}}{s^2} + G_{m4}s \right) = \frac{w_{u1}(G_{m3}w_{u2} + G_{m4}s)}{s^2} \] (6.1)
when the transfer function of a $G_m$-$C$ integrator is:

$$H_I(s) = \frac{G_m}{sC} \quad (6.2)$$

From equation 6.1 the feedforward zero can be derived:

$$w_z = -\frac{a_2}{a_1} w_{u2} = -\frac{G_{m3}}{G_{m4}} w_{u2} \quad (6.3)$$

### 6.3 Non-ideal behavior

In figure 6.2 an example of a transfer function of an integrator is shown. In the ideal case the dc-gain, $A_0$, of both integrators is infinite, but in

![Diagram of integrator](image)

Figure 6.2: Transfer function of the $G_m$-$C$ integrator. The black line shows the gain and the grey line shows the phase.

the non-ideal case it is limited because of limited output resistance, $R_0$. 

![Diagram of integrator](image)
6.4 First integrator

The capacitive load at the output node is causing a first-order roll-off and the unity-gain frequency can be found at $G_m/C$ derived in equation A.20. Due to the coupling capacitance between the input and output a zero is introduced and the roll-off is leveled out at $G_m/C_{dg}$. The roll-off is a dashed line in the figure, which means it is a bit uncertain what the actual behavior is, due to influence from higher poles.

In the complete loop filter, in figure 6.3, we see the effect of the feedforward coefficients, a first-order roll-off at high frequencies. For stability it is important that this roll-off is starting before crossing unity-gain, since this would give optimal a phase-margin of 90 degrees.

![Figure 6.3: Transfer function of the loop filter. The black line shows the gain and the grey line shows the phase.](image)

6.4 First integrator

The first integrator is outside the loop, hence noise and distortion will be transferred directly to the output without any noise shaping. This makes the design of the first integrator critical. Although by proper design this contribution to the total noise can be limited, making the quantization noise remain as the dominant noise source.

In figure 6.4 the structure of the first integrator is shown. Here transistor M3 and M4 are current sources that are supplying both the integrator and the DAC. The DAC was designed in chapter 5. Because of the limiting supply voltage it was not possible to use cascades between the current sources and the output nodes to improve output resistance and the dc-gain derived in A.19. This dc-gain is setting the level of the noise-floor in the noise transfer function, therefore by integrating over
the noise floor it can be shown if the contribution to the total noise could be neglected or not. Since the noise requirement is low, simulations showed that cascaded transistors between the current sources and the output nodes were not needed. Transistor M1 and M2 are input transistors. They are converting a voltage to a current through the transconductance, $g_m$. Noise and distortion analysis will set their minimum width and $g_m$ respectively. To control the common-mode feedback, which is required in a fully differential structure, transistor M5, M6 and M7 are used. Transistor M6 and M7 are biased in the linear region, and through a copy-branch controlling the common-mode voltage together with transistor M5.

6.4.1 Flicker and thermal noise

In this section the circuit noise is calculated, to give the minimum width and length of the transistors. Every transistor is generating noise, mainly thermal and flicker noise in a CMOS transistor. To limit the analysis we only take into account the most contributing transistors. Here the input transistors, M1 and M2, and the current sources, M3 and M4, are dominating the noise contribution. In chapter 3 it has been seen that the noise spectral density for a CMOS transistor can be expressed by the following equation:

$$V_{n_i}^2(f) = 4k_BT\gamma \frac{1}{g_{m_i}} + \frac{K_{f,P/N}}{W_iL_iC_{ox}f}$$  \hspace{1cm} (6.4)

In order to make an estimation of the noise contribution all noise sources are referred back to the input of transistor M1 and M2. First
we find the gains from the noise sources to the output nodes. From input transistors M1 and M2 the gain is expressed as,

$$\left|\frac{V_{no}}{V_{n1}}\right| = \left|\frac{V_{no}}{V_{n2}}\right| = g_{m1}R_o$$  \hspace{1cm} (6.5)

where $R_o$ is the output resistance at the output node. Continuing with the current source M3 and M4, the gain is expressed as

$$\left|\frac{V_{no}}{V_{n3}}\right| = \left|\frac{V_{no}}{V_{n4}}\right| = g_{m3}R_o$$  \hspace{1cm} (6.6)

Using the gain expressions a total output noise spectral density can be expressed at the output node.

$$V_{no}^2(f) = 2(g_{m1}R_o)^2V_{n1}^2(f) + 2(g_{m3}R_o)^2V_{n3}^2(f)$$  \hspace{1cm} (6.7)

Now referring this noise back to the input, by dividing the output noise spectral density with the gain of the input transistor, $(g_{m1}R_o)^2$, yields the following equation:

$$V_{ni}^2(f) = 2V_{n1}^2(f) + 2\left(\frac{g_{m3}}{g_{m1}}\right)^2V_{n3}^2(f)$$  \hspace{1cm} (6.8)

If the values from equation 6.4 is inserted the equivalent rms input noise density can be expressed, allowing a calculation of the SNR.

The thermal noise can now be calculated,

$$V_{th}(f) = \sqrt{\frac{2 \cdot 4kBT\gamma}{g_{m1}}(1 + \frac{g_{m3}}{g_{m1}})df} = \frac{51.8 \text{ nV/}\sqrt{\text{Hz}}}{(6.9)}$$

where $\gamma = 1.3$, $g_{m1} = 110 \mu\text{A/V}$, $g_{m3} = 643 \mu\text{A/V}$, $k = 1.38 \cdot 10^{-23}$ J/K and $T = 300$ K.

The flicker noise can be calculated to,

$$V_f(f) = \sqrt{\frac{2K_{f,N}}{W_1L_1C_{ox}f} + \frac{2K_{f,P}}{W_3L_3C_{ox}f}\left(\frac{g_{m3}}{g_{m1}}\right)^2df} = \frac{5.83 \mu\text{V/}\sqrt{\text{Hz}}}{(6.10)}$$

where $W = 0.32 \mu\text{m}$, $L = 0.2 \mu\text{m}$, $C_{ox} = 16.2 \text{ mF/m}^2$, $K_{f,N} = 14.6 \cdot 10^{-24} \text{ V}^2\text{F}$ and $K_{f,P} = 9.72 \cdot 10^{-24} \text{ V}^2\text{F}$.

During the design it can be helpful to calculate the flicker-knee. It shows where the turn-over point from thermal- to flicker noise domination is. The flicker-knee, $f_C$ is calculated by equalizing the thermal and flicker noise spectral densities, yielding a flicker frequency of $f_C = 12.7$ MHz for the first integrator. If not the current sources are included in
the calculations the flicker-knee is equal to 72 MHz, which is quite high due to the small transistor area of the input transistors.

The total input referral noise is calculated by integrating the flicker noise in equation 6.10 and the thermal noise in equation 6.9 over the signal band.

\[
V_{eq} = \sqrt{\int_0^{264M} V_n^2(f) df} = \sqrt{(843 \mu V)^2 + (811 \mu V)^2} = 1170 \mu V
\]

Here it is shown that the contributions from the flicker noise and the thermal noise are similar. An improvement of SNR could be done by increasing the gain, or by increasing the area of the input transistors. A SNR can now be derived by comparing \(V_{eq,rms}\) with the maximum rms input voltage equal to 212 mV.

\[
SNR_{noise} = 20 \log \left( \frac{V_{rms}^{in}}{V_{rms}^{eq}} \right) = 45.2 \text{ dB} \quad (6.12)
\]

This noise contribution is high above the requirement, hence the chosen sizing is good enough.

### 6.4.2 Third harmonic distortion

Also distortion give raise to noise, but since the proposed structure is fully differential even order harmonic distortion is reduced. Although the second harmonic is reduced the third harmonic distortion can be significant. In appendix A the following expression for the third harmonic distortion is derived,

\[
HD3 \approx \frac{1}{32} \left( \frac{\hat{v}_{in}}{V_{GT}} \right)^2
\]

where \(\hat{v}_{in}\) is the differential input amplitude and \(V_{GT} = V_{GS1} - V_T\). By choosing

\[
\hat{v}_{in} < V_{GT}
\]

the distortion is less than -30 dB and hence the SNR requirement of 30 dB is fulfilled. In order to allow a high input amplitude the previous expression motivates a high \(V_{GT}\). The \(V_{GT}\) of the integrator can be expressed as,

\[
V_{GT} = V_{GS1} - V_T = V_{in,CM} - V_{DS5} - V_{DS6} - V_T
\]

where \(V_{DS5}\) is equal to 200 mV biased in saturation region and \(V_{DS6}\) is equal to 50 mV biased in linear region. Since \(V_T\) is equal to 300 mV, this would give a \(V_{GT}\) of \(V_{in,CM} - 550\) mV, which equals 400 mV when the input common-mode voltage is chosen to be 950 mV. This may be true
in calculations, but DC operation results from Cadence gave a result of 300 mV. Hence, the first integrator achieve a $V_{GT}$ of 300 mV yielding a SNR of 30 dB, which is at the edge of the required SNR. An increase of SNR can be made by increasing the input common-mode voltage, but here the supply voltage is a limitation. The result from equation 6.12 indicate a input signal that is higher than required. Hence, a solution to decrease the third harmonic would be to decrease the input amplitude and increase the common-mode input level. Another solution that is possible is to use degeneration.

### 6.4.3 Common-mode output voltage and clipping level

Since the common-mode output voltage is equal to the input common-mode voltage of the second integrator the choice of the common-mode is treated in section 6.5.

The clipping levels determine the maximum voltage-swing at the output nodes of the integrators. In order to keep transistor M3 and M4 in saturation the clipping level cannot be too high. In the high-level simulation optimal coefficients were calculated to control those levels. In order to choose the clipping level of the first integrator, noise and distortion in the second integrator and in the first feedforward coefficient have to be considered.

### 6.4.4 Transfer function

In figure 6.5 the transfer function simulation of the first integrator at transistor level is shown. A dc-gain of 21 dB is reached. Although this is a quite low dc-gain it is difficult to achieve a higher value without cascodes. With the low SNR requirement of 30 dB it may still be good enough.

### 6.5 Second integrator

The structure of the second integrator is the same as the first one. This integrator is after the first integrator in the signal path and therefore its noise and distortion is first-order filtered, by the gain of the first integrator. At low frequencies this equals the dc-gain, which was determined to 21 dB. This is relaxing the requirements on the second integrator and the design here is therefore less critical.
6.5.1 Common-mode output voltage and clipping levels

By adjusting the first integrator common-mode output voltage and the clipping level, power consumption and transistor area can be optimized. But since the design of the second integrator is not crucial common-mode voltage and clipping levels are chosen more directly. The common-mode output voltage is chosen to be 800 mV and the clipping levels to be 400 mV differential. Also the second integrator is given the same common-mode output and clipping level.

6.5.2 Flicker and thermal noise

Here the calculations for the noise are the same as they were for the first integrator in section 6.4. The equivalent input noise is calculated to,

$$V_{eq}^{rms} = \sqrt{(348 \, \mu V)^2 + (1610 \, \mu V)^2} = 1650 \, \mu V \quad (6.16)$$

which is showing a much larger contribution from the flicker noise due to the lower current supplied by the current sources. Comparing $V_{eq}^{rms}$ with the maximum rms input voltage, it yields a SNR of,

$$SNR_{noise} = 20 \log\left(\frac{V_{in}^{rms}}{V_{eq}^{rms}}\right) = 44.7 \, dB \quad (6.17)$$

where $V_{in}^{rms}$ is equal to the clipping level rms value of 283 mV. When including the first-order filtering this SNR is equal to 66 dB at low
frequencies. This indicates a sufficient high clipping level and a small decrease would not degrade of the total SNR. A lower input amplitude can be required if the third harmonic is too large.

6.5.3 Third harmonic distortion

For an optimal designed Sigma-Delta modulator the maximum input to the second integrator is the clipping level. Here a clipping level of 0.4 V was chosen. This yields a third harmonic distortion of,

\[ HD_3 \approx -6 \text{ dB} \] (6.18)

where \( V_{GT} = 100 \text{ mV}, V_{DS5} = 280 \text{ mV} \) and \( V_{DS7} = 50 \text{ mV} \). Due to the first-order filtering this is equal to a SNR of 26 dB at low frequencies, which is too low. In the worst case the third harmonic is at the edge of the signal band, where the gain of the first integrator is zero, hence a HD3 of at least -30 dB would be preferred. In chapter 7 the simulation results are shown.

6.5.4 Transfer function

In figure 6.6 the transfer function of the second integrator at transistor-level is shown. A dc-gain of 19 dB is reached.

![Transfer function](image)

Figure 6.6: Transfer function of the second integrator at 4.224 GHz. The solid line represent the gain and the dashed line the phase.
6.6 Feedforward

In this section the feedforward coefficients are designed. As mentioned in chapter 3 the feedforward coefficients provide loop stability by introducing a zero in the signal transfer function, making a first-order roll-off at high frequencies. By using the optimal coefficients derived in chapter 4 the circuit can be designed. Since the feedforward coefficients are inside the loop, noise and distortion is second-order filtered. At low frequencies this filtering is limited by the dc-gain equal to 40 dB.

6.6.1 Structure

Making use of the current law, which says that addition and subtraction of current are permitted, the feedforward coefficients are designed as a simple differential pair pulling current from the comparator. The differential pair is converting a voltage to a scaled current according to the optimal coefficients. Noise and distortion conditions are not very crucial here, since the error is second-order filtered. In figure 6.7 the structure is shown.

![Figure 6.7: The schematic of the feedforward coefficients](image)

6.6.2 Design

In chapter 4 the optimal feedforward coefficients where calculated. Recalling table 4.1 and equation 6.3 the transconductance of the second feedforward coefficient should be made 1.4 times larger then the first feedforward coefficient. Since the transconductance is proportional to the width, shown in equation A.11 this relation can be transfered to the width. Hence, W4, W5 and W6 is made 1.4 times larger than W1, W2 and W3.
6.6.3 Third harmonic distortion

The third harmonic distortion for the first coefficient is given by,

\[ HD3 = -19 \text{ dB} \]  
\[ (6.19) \]

where \( V_{GT1} = 210 \text{ mV}, V_{DS3} = 240 \text{ mV} \). The second coefficient resulted in the same SNR, where \( V_{GT4} = 210 \text{ mV}, V_{DS6} = 225 \text{ mV} \). Due to the second-order filtering this is equal to a SNR of 59 dB at low frequencies, which is sufficient.

6.7 Loop filter

In figure 6.8 the transfer function of the loop filter at transistor level is shown.

6.7.1 Transfer function

Figure 6.8: Transfer function of the loop filter sampled at 4.224 GHz. The solid line represent the gain and the dashed line the phase.

A dc-gain of 40 dB is achieved and the phase-margin at half the sampling frequency is 72 degrees.
Chapter 7

System simulation

7.1 Introduction

In this chapter the complete system is simulated. To analyze the performance, simulations have been done for different sampling frequencies with different delays. The delay is possible to vary by changing the delay between the two clocks, which are controlling the comparator and the d flip-flop respectively. In the next section the results will be shown.

7.2 Results

During the simulations of the whole Sigma-Delta modulator the comparator was fine tuned to optimize the performance. Three parameters were used: Firstly, the width of the diode transistors was tuned in such a way that the voltage swing was less than 0.9 V for the maximum input current swing that the comparator experiences. This limited memory effect in the input stage is due to the relatively large current sources that are directly connected to the input nodes. Secondly, the transmission gate connected between the output nodes was sized for a proper reset, avoiding memory effect in the output nodes. Last, the delay between the clock driving the comparator and the clock driving the d flip-flop, was optimized to be sufficiently large to limit the numbers of non-taken decisions.

Although high-level simulations in chapter 4 and simulations of the feedback delay in chapter 5 showed that a sampling frequency of 8.448 GHz was too high for a stable behavior, it was simulated together with the other sampling frequencies 6.336 GHz and 4.224 GHz. The comparator was fine tuned for each sampling frequency.

In table 7.1 the achieved SNR of the Sigma-Delta modulator is shown. Different delays have been created by changing the time be-
Table 7.1: SNR simulation of the Sigma-Delta modulator, where the SNR is shown at different sampling frequencies, $f_s$, including the excess feedback delays, $t_d$.

<table>
<thead>
<tr>
<th>Sample frequency, Delay</th>
<th>73 ps</th>
<th>83 ps</th>
<th>93 ps</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.224 GHz</td>
<td>19 dB</td>
<td>19 dB</td>
<td>17 dB</td>
</tr>
<tr>
<td>6.336 GHz</td>
<td>27 dB</td>
<td>27 dB</td>
<td>27 dB</td>
</tr>
<tr>
<td>8.448 GHz</td>
<td>27 dB</td>
<td>29 dB</td>
<td>28 dB</td>
</tr>
</tbody>
</table>

Between the two clocks, driving the comparator and the d flip-flop respectively. A delay of 83 ps is the best choice if stability is not concerned. At longer delays the SNR drops due to the delay and at shorter delays the comparator has too many non-taken decisions. A delay of 83 ps is equal to 35%, 53% and 70%, at the sampling frequencies 4.224 GHz, 6.336 GHz and 8.448 GHz respectively. In [9] it was reported that a delay of 38% is the maximum delay in a second-order Sigma-Delta modulator to achieve a stable system.

In figure 7.2 (last page in the chapter) the output spectrum for the three different sampling frequencies with a feedback delay of 83 ps are shown. It can been seen that the overshoot of the spectrum is more significant at high sampling frequencies and is move closer to the signal band. It can also be seen that the curve is more fluctuating. All this indicates an instable behavior at higher sampling frequencies than 4.224 GHz.

During the simulations it was found that the optimal clipping level of 0.4 V was not reached, but instead had a maximum level of 0.2 V. The reason for this is that the DAC current was not compensated for the feedback delay. Therefore the amount of charge was not sufficient to charge the voltage up to the clipping level. As a result, the third harmonic distortion from the second integrator was lower than expected. When recalculating the third harmonic distortion for a clipping level of 0.2 V it results in,

$$HD3 \approx -18 \text{ dB}$$  \hspace{1cm} (7.1)

which gives a SNR of 39 dB at low frequencies. This calculated value is not completely accurate due to the third harmonic calculation. The calculation is assuming a transistor that is working in strong inversion and has a sinusoidal input. The input transistors in the second integrator has a $V_{GT}$ of 100 mV, which is close or inside the weak inversion region. This means that the the third harmonic distortion is limited. The input signal is not sinusoidal but triangular and this increases the SNR by a few dB, since it has a lower rms value. In figure 7.1 simulation results of the third harmonic distortion can be seen. It equals -34 dB, which gives a difference between the signal level of -2 dB, equal
to a signal-to-distortion-ratio, SDR, of 32 dB. This can be compared with the expected SDR of 21 dB at the signal frequency, when having optimal designed coefficients. Hence, in this design the SDR is sufficient, but when changing the design so that a clipping level of 0.4 V is reached the third harmonic has to decrease. This can be made either by decreasing the clipping level, which is possible due to the sufficient SNR caused by the circuit noise, or by increasing $V_{GT}$ and hence the power consumption.

Figure 7.1: Output spectrum of a 50 MHz input signal, sampled at 4.224 GHz, with a feedback delay of 83 ps. The third harmonic distortion can be seen at 150 MHz.

7.3 Layout considerations

7.3.1 Introduction

Although this project did not aim at creating the layout, some considerations have come up during the design phase. At high-speeds capacitive loads can be crucial for the performance. In previous simulations capacitive load from wires has been neglected, which may not be true in reality. In this section wire capacitance and delays is discussed, followed by recommendations on the block placement.

7.3.2 Wire delays

In CMOS12 the capacitance in wires can be calculated to 360 aF/µm², given a minimum length of 0.12 µm the capacitance can be expressed as 43.2 aF/µm. Hence, 1 fF, is equal to a wire length of 23 µm. In CMOS090 this can be assumed to be in the same range.
7.3.3 Block placement

In the report it has been shown that the feedback delay is critical, hence special attention must be taken on the feedback path during layout. In this path the capacitance should be limited, and therefore short wires are preferred. By placing the quantizer and the first integrator close to each other the wire length can be limited. Distances between the first integrator, the second integrator, the feedforward coefficients and the quantizer are not critical, hence wire capacitances can be neglected compared to the integration capacitances.
Figure 7.2: Output spectrum of a 100 MHz input signal, sampled at (a) 4.224 GHz, (b) 6.336 GHz, (c) 8.448 GHz, with a feedback delay of 83 ps
Chapter 8

Conclusion

The specified SNR of 30 dB could not be reached. Instead a stable Sigma-Delta modulator at a sampling frequency of 4.224 GHz was designed. It achieved a SNR of 19 dB and had a power consumption of 0.5 mW. The feedback delay was 83 ps, 35% of the sampling period.

In order to increase the sampling frequencies an analysis of the maximum feedback delay allowed have to be done. In [9] the maximum delay to ensure stability was reported to be 38% of a sampling period for a second-order Sigma-Delta modulator. This indicates that the result mentioned above is close to what maximly can be achieved at a feedback delay of 83 ps.

Since the DAC current was not compensated for the delay the modulator was not optimally designed. An increase of the current and a decrease of the third harmonic distortion in the second integrator could give a small change in SNR. The solutions that were given, will only give a small increase of power consumption.

8.1 Further improvements

Since the designed structure was not sufficient to achieve the required SNR, improvements have to be made. Four solutions exist;

Firstly, the speed of the feedback loop can probably be improved. This can be achieved by changing from full swing to a limited swing in the feedback loop, hence limiting the amount of charge to move. If the delay could be reduced to 55 ps a stable system at 6.336 GHz would be possible and a SNR close to 30 dB could be achieved.

Secondly, the DAC pulse can be modified. Instead of using a NRZ pulse, a RZ pulse can be applied. Now the pulse can be modified to feed back the optimal amount of charge to the first integrating capacitance, although the feedback loop has a delay. This would increase the
power consumption, but not considerably since the DAC current is not dominant.

The third solution is to change the structure to a one-delay structure. This would change the structure of the modulator completely and is not considered here. In [3] it can be studied in detail.

Lastly, a multi-feedback structure can be designed. This would solve the delay problem, but would increase the complexity of the matching. In [9] it can be studied in detail.

The first and the second solution is the most promising ones. The second solution could easily be simulated, by changing the design of the DAC. A third clock needs to be included and would introduce a more complex DAC structure. If a sampling frequency of 6.336 GHz with a delay of 83 ps is chosen, the third clock has to be asymmetric. This means that the time when the clock is high must be shorter than the time when the clock is low. Such a clock is possible to design.

Also the d flip-flop designed in this report has to be changed. A fully differential structure is preferred, since this would give a more robust design and the structure would be less sensitive for mismatch.
References


## Notation

Symbols used in the report.

### Variables and parameters

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{gs}$</td>
<td>Gate-source voltage</td>
<td>[V]</td>
</tr>
<tr>
<td>$V_{sb}$</td>
<td>Source-bulk voltage</td>
<td>[V]</td>
</tr>
<tr>
<td>$V_{T0}$</td>
<td>Threshold voltage</td>
<td>[V]</td>
</tr>
<tr>
<td>$I_{ds}$</td>
<td>Drain-source current</td>
<td>[A]</td>
</tr>
<tr>
<td>$r_{ds}$</td>
<td>Drain-source resistance</td>
<td>[Ω]</td>
</tr>
<tr>
<td>$g_{m}$</td>
<td>Transconductance</td>
<td>[A/V]</td>
</tr>
<tr>
<td>$g_{ds}$</td>
<td>Conductance</td>
<td>[1/Ω]</td>
</tr>
<tr>
<td>$k_B$</td>
<td>Boltzmann's constant</td>
<td>[J/K]</td>
</tr>
<tr>
<td>$T$</td>
<td>Temperature</td>
<td>[K]</td>
</tr>
<tr>
<td>$K_f$</td>
<td>Flicker noise constant</td>
<td></td>
</tr>
<tr>
<td>$\sigma_j$</td>
<td>Jitter constant</td>
<td></td>
</tr>
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<td>$W$</td>
<td>Transistor width</td>
<td>[m]</td>
</tr>
<tr>
<td>$L$</td>
<td>Transistor length</td>
<td>[m]</td>
</tr>
<tr>
<td>$f$</td>
<td>Frequency</td>
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</tr>
<tr>
<td>$\tau$</td>
<td>Time-constant</td>
<td>[s/rad]</td>
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<td>[Ω]</td>
</tr>
<tr>
<td>$C$</td>
<td>Capacitance</td>
<td>[F]</td>
</tr>
<tr>
<td>$t_{ox}$</td>
<td>Oxide thickness</td>
<td>[m]</td>
</tr>
<tr>
<td>$\mu$</td>
<td>Charge mobility</td>
<td>[cm²/V·s]</td>
</tr>
<tr>
<td>$\epsilon$</td>
<td>Permittibility</td>
<td>[F/m]</td>
</tr>
</tbody>
</table>
Appendix A

Basic analog circuit design

In this chapter the element knowledge about CMOS technology and analog design will be summarized.

A.1 MOSFET equations

A.1.1 Large signals

\[ V_{GT} = V_{GS} - V_T \] \hspace{1cm} (A.1)

Subthreshold

\[ I_{DS} \approx 0 \quad V_{GT} < 0 \] \hspace{1cm} (A.2)

Linear region

\[ I_{DS} = k_{W} \frac{W}{L} \cdot (V_{GT} \cdot V_{DS} + \frac{V_{DS}^2}{2})(1 + \lambda V_{DS}) \quad V_{GT} > V_{DS} \geq 0 \] \hspace{1cm} (A.3)

Saturation region

\[ I_{DS} = k_{W} \frac{W}{2L} \cdot V_{GT}^2 \cdot (1 + \lambda V_{DS}) \quad V_{DS} > V_{GT} \geq 0 \] \hspace{1cm} (A.4)

Body effect

\[ V_{T'} = V_T|_{V_{SB} > 0} = V_{T_0} + \gamma \cdot (\sqrt{2|\phi_F| + V_{SB}} - \sqrt{2|\phi_F|}) \] \hspace{1cm} (A.5)

\[ k = \frac{\mu \epsilon}{t_{ox}} = \mu C_{ox} \] \hspace{1cm} (A.6)

The parameter \( \mu \) is called charge mobility, \( t_{ox} \) is the gate-oxide thickness and \( C_{OX} \) is the gate-capacitance.
Output impedance constant

\[ \lambda = \frac{k_{ds}}{2L \cdot \sqrt{V_{DS} - V_{GS} + V_T + \phi_0}} \quad (A.7) \]

\[ k_{ds} = \sqrt{\frac{2K_s \cdot \epsilon_0}{q \cdot N_A}} \quad (A.8) \]

Body effect constant

\[ \gamma = \sqrt{\frac{2q \cdot N_A \cdot K_s \cdot \epsilon_0}{C_{OX}}} \quad (A.9) \]

A.1.2 Small signals

The transconductance can be written in several ways which can be useful during design:

\[ g_m = \frac{dI_D}{dV_{GS}} = \mu \cdot C_{OX} \cdot \frac{W}{L} \cdot V_{GT} \quad (A.10) \]

\[ g_m = \sqrt{2\mu \cdot C_{OX} \cdot \frac{W}{L} \cdot I_D} \quad (A.11) \]

\[ g_m = \frac{2I_D}{V_{GT}} \quad (A.12) \]

Source-bulk transconductance

\[ g_s = \frac{dI_D}{dV_{SB}} = \frac{\gamma \cdot g_m}{2\sqrt{V_{SB} + 2|\phi_F|}} \quad (A.13) \]

Conductance

\[ g_{ds} = \frac{1}{r_{ds}} = \frac{dI_D}{dV_{DS}} = \lambda \cdot I_{Dsat} \approx \lambda \cdot I_D \quad (A.14) \]

If ignoring channel-length modulation \( \lambda \approx 0 \).

A.1.3 Noise

Thermal and flicker noise spectral density respectively, see [4]:

\[ V_i^2(f) = 4k_BT\left(\frac{2}{3}\right) \frac{1}{g_m} + \frac{K_f}{WLC_{ox}f} \quad (A.15) \]
A.2 Derivation of unity-gain frequency at the comparator output

Using a small signal model shown in figure A.1 for each transistor in the comparator some parameters can be derived. Since the structure is fully differential the structure is symmetric and hence only one node has to be considered. Here all the capacitances at the output node are collected in $C_{TOT}$.

![Small signal model of a CMOS transistor.](image)

Figure A.1: Small signal model of a CMOS transistor.

Deriving the transfer function from the input, which in this case is the gate voltage at the latch transistor and hence the output voltage of the other output node $p$, to the output node $m$ yields

$$
\frac{V_{outm}(s)}{V_{outp}(s)} = g_m v_{GSl} \cdot \frac{1}{g_{ds3} + g_{ds5} + g_m + sC_{TOT}} \quad (A.16)
$$

By resolving the expression for the following structure the first pole, $p_1$ and the DC-gain, $A_0$, can be derived.

$$
A(s) = \frac{A_0}{1 + \frac{1}{p_1}} \quad (A.17)
$$

Identifying $p_1$ from equation A.16 yields

$$
p_1 = \frac{g_{ds3} + g_{ds5} + g_m}{C_{TOT}} \quad (A.18)
$$

Identifying $A_0$ from equation A.16 yields

$$
A_0 = g_m R_0 = \frac{g_m}{g_{ds3} + g_{ds5} + g_m} \quad (A.19)
$$

When $A_0$ is large the following expression is true.

$$
w_u = |A_0| p_1 = \frac{g_m}{C_{TOT}} \quad (A.20)
A.3 Differential pair calculation

In order to limit distortion a differential pair is designed in such a way that a maximum voltage swing at the integrators outputs could be converted to a current.

A maximum differential input voltage swing around a common-mode level can be calculated as in the following way, according to [7], assuming saturation:

$$\Delta v = \sqrt{\frac{I_{ss}}{\mu_n C_{ox}} \frac{W}{L}}$$ (A.21)

If we express the width over length of the input transistor,

$$\frac{W}{L} = \frac{I_{Dsat}}{V_{GT}^2} = \frac{I_{ss}}{2V_{GT}^2}$$ (A.22)

then \( \Delta v \) is expressed as:

$$\Delta v = \sqrt{\frac{I_{ss}}{\mu_n C_{ox}} \frac{I_{ss}}{2V_{GT}^2}} = \frac{2V_{GT}^2}{\mu_n C_{ox}}$$ (A.23)

\( V_{GT} = V_{GS} - V_{Tn} \) and \( V_{GS} \) is determined by the difference between the common-mode voltage level and the source-bulk voltage. This means that it is only possible to increase \( \Delta v \) by either increasing the common-mode voltage or decreasing the source-bulk voltage.

A.4 Third harmonic distortion

Following calculations can be verified in [1] and in [10].

$$I_{out} = I_{D1} - I_{D2}$$ (A.24)

$$I_b = I_{D1} + I_{D2}$$ (A.25)

Saturation:

$$I_D = \alpha V_{GT}^2$$ (A.26)

$$V_{in} = V_{GS1} - V_{GS2} = \sqrt{\frac{I_{D1}}{\alpha}} - \sqrt{\frac{I_{D2}}{\alpha}}$$ (A.27)

$$V_{in}^2 = \frac{1}{\alpha} (I_{D1} + I_{D2} - 2\sqrt{I_{D1}I_{D2}})$$

$$= \frac{1}{\alpha} (I_b - 2\sqrt{I_{D1}I_{D2}})$$

$$= \sqrt{4I_{D1}I_{D2} = (I_{D1} + I_{D2})^2 - (I_{D1} - I_{D2})^2 = I_b^2 - I_{out}^2} /$$

$$= \frac{1}{\alpha} (I_b - \sqrt{I_b^2 - I_{out}^2})$$
\[ i_{out} = \alpha v_{in} \sqrt{\frac{2I_b}{\alpha} - v_{in}^2} \]  
(A.28)

Taylor expansion around \( v_{in} = 0 \):

\[ i_{out} = I_{out} + \frac{\delta i_D}{\delta v_{in}}|_{v_{in}=0} v_{in} + \cdots + \frac{1}{N!} \frac{\delta^N i_D}{\delta v_{in}^N} |_{v_{in}=0} v_{in}^N \]  
(A.29)

\[ \frac{\delta i_D}{\delta v_{in}} |_{v_{in}=0} = \sqrt{2\alpha I_b} = g_1 \]  
(A.30)

\[ \frac{\delta^2 i_D}{2 \delta v_{in}^2} |_{v_{in}=0} = 0 \]  
(A.31)

\[ \frac{1}{6} \frac{\delta^3 i_D}{\delta v_{in}^3} |_{v_{in}=0} = -\alpha \sqrt{\frac{\alpha}{8I_b}} = g_3 \]  
(A.32)

\[ v_{in} = \hat{v}_{in} \cos(\omega t) \]  
(A.33)

\[ \cos^3(x) = \frac{3}{4} \cos(x) + \frac{1}{4} \cos(3x) \]  
(A.34)

\[ H_1 = \hat{v}_{in} g_1 + \frac{3}{4} H_3 \]  
(A.35)

Here the second term in \( H_1 \) is neglected. A third harmonic distortion can now be derived:

\[ HD3 \approx \frac{H_3}{H_1} = \frac{1}{16} \frac{\alpha}{I_b} \hat{v}_{in}^2 \]

\[ = \frac{1}{32} \left( \frac{\hat{v}_{in}}{V_{GT}} \right)^2 \]
Appendix B

Transistor sizing

In this appendix the transistor sizes for the Sigma-Delta modulator sampled with a frequency of 4.224 GHz are given.

In table B.1 the current consumption of the Sigma-Delta modulator is summarized. A total current of \( \approx 416 \ \mu A \) were consumed. This is equal to a power consumption of 0.5 mW.

<table>
<thead>
<tr>
<th>Block</th>
<th>Current [( \mu A )]</th>
</tr>
</thead>
<tbody>
<tr>
<td>First integrator</td>
<td>40</td>
</tr>
<tr>
<td>Second integrator</td>
<td>30</td>
</tr>
<tr>
<td>Feed forward coefficients</td>
<td>53</td>
</tr>
<tr>
<td>Comparator</td>
<td>197</td>
</tr>
<tr>
<td>D flip-flop</td>
<td>50</td>
</tr>
<tr>
<td>DAC</td>
<td>46</td>
</tr>
<tr>
<td>Total</td>
<td>416</td>
</tr>
</tbody>
</table>

Table B.1: Current consumption of the Sigma-Delta modulator

In table B.2 the sizing of the Sigma-Delta modulator is summarized.
Table B.2: Transistor sizing of the Sigma-Delta modulator [$\mu m$] (a) First integrator, (b) Second integrator, (c) Feed forward coefficients, (d) Comparator, (e) D flip-flop, (f) DAC

<table>
<thead>
<tr>
<th>Transistor</th>
<th>Sizing [W/L]</th>
<th>Transistor</th>
<th>Sizing [W/L]</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1</td>
<td>0.32/0.2</td>
<td>M1</td>
<td>0.7/0.1</td>
</tr>
<tr>
<td>M3</td>
<td>23.6/0.3</td>
<td>M3</td>
<td>7.5/0.3</td>
</tr>
<tr>
<td>M5</td>
<td>60/2</td>
<td>M5</td>
<td>30/2</td>
</tr>
<tr>
<td>M6</td>
<td>0.44/0.1</td>
<td>M6</td>
<td>0.34/0.1</td>
</tr>
<tr>
<td>C1</td>
<td>30 fF</td>
<td>C1</td>
<td>62 fF</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Transistor</th>
<th>Sizing [W/L]</th>
<th>Transistor</th>
<th>Sizing [W/L]</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1</td>
<td>0.7/0.1</td>
<td>M1</td>
<td>48/0.3</td>
</tr>
<tr>
<td>M3</td>
<td>7.5/0.3</td>
<td>M3</td>
<td>4.8/0.1</td>
</tr>
<tr>
<td>M5</td>
<td>30/2</td>
<td>M5</td>
<td>1.4/0.1</td>
</tr>
<tr>
<td>M6</td>
<td>0.34/0.1</td>
<td>M7</td>
<td>0.24/0.1</td>
</tr>
<tr>
<td>C1</td>
<td>62 fF</td>
<td>Mpp</td>
<td>1.9/0.1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Mpn</td>
<td>1.5/0.1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Transistor</th>
<th>Sizing [W/L]</th>
<th>Transistor</th>
<th>Sizing [W/L]</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1</td>
<td>0.4/0.3</td>
<td>M1</td>
<td>0.12/0.1</td>
</tr>
<tr>
<td>M2</td>
<td>0.6/0.1</td>
<td>M3</td>
<td>30/3</td>
</tr>
<tr>
<td>M3</td>
<td>15/2</td>
<td>M4</td>
<td>0.56/0.3</td>
</tr>
<tr>
<td>M4</td>
<td>0.56/0.3</td>
<td>M5</td>
<td>0.4/0.1</td>
</tr>
<tr>
<td>M5</td>
<td>0.6/0.1</td>
<td>M6</td>
<td>3.6/0.1</td>
</tr>
<tr>
<td>M6</td>
<td>21/2</td>
<td>M7</td>
<td>1.2/0.1</td>
</tr>
<tr>
<td>M7</td>
<td>21/2</td>
<td>M8</td>
<td>0.32/0.1</td>
</tr>
<tr>
<td>M8</td>
<td>21/2</td>
<td>M9</td>
<td>0.12/0.1</td>
</tr>
<tr>
<td>M9</td>
<td>0.36/0.1</td>
<td>M10</td>
<td>0.12/0.1</td>
</tr>
<tr>
<td>M10</td>
<td>0.36/0.1</td>
<td>M11</td>
<td>0.36/0.1</td>
</tr>
</tbody>
</table>
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