THE UNIVERSITY OF CALGARY

Spiral Inductor

Q-Enhancement Techniques

by

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A THESIS

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Abstract

On-chip inductors are important, performance-limiting components in monolithic radio frequency (RF) circuits, such as voltage-controlled oscillators, low-noise amplifiers and passive-element filters. The quality factor of the inductors is limited by the resistive losses in the spiral coil and by the substrate losses. In this work we propose a method for generating an inductor of high quality, theoretically infinite, by looking at the input of the primary winding of a transformer, with the secondary driven by a current appropriately related to the input signal. This technique generates a compensated passive rather than an active inductor. The electrical, noise and distortion properties of this circuit are presented. A way to employ this circuit in a buffered voltage controlled oscillator (VCO) with reduced power consumption is also shown.
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Dedication

This work is dedicated to my parents Mihai and Mihaela Georgescu and to all my teachers.
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List Of Symbols and Abbreviations

Chapter 1

\( RF \) - radio frequency
\( VCO \) - voltage controlled oscillator

Chapter 2

\( E \) - electric field
\( H \) - magnetic field
\( P_t \) - average power dissipated by the network
\( W_m \) - magnetic energy
\( W_e \) - electric energy
\( E_{\text{store}} \) - energy stored per cycle
\( E_{\text{diss}} \) - energy dissipated per cycle
\( Q \) - quality factor
\( T \) - cycle time
\( \omega \) - angular frequency
\( \delta \) - skin depth
\( \sigma \) - electrical conductivity
\( \mu \) - magnetic permittivity
\( \epsilon \) - electric permittivity
\( \epsilon_r \) - relative electric permittivity

Chapter 3

\( N \) - number of turns
\( L_i \) - inductance of the \( i^{th} \) inductor
\( M_{ij} \) - mutual inductance between the \( i^{th} \) and \( j^{th} \) inductors
\( K_{ij} \) - inverse mutual inductance between the \( i^{th} \) and \( j^{th} \) inductors
\( L_{se} \) - series inductance
\( L_{sh} \) - shunt inductance
\( n \) - turns ratio
\( k \) - coupling coefficient \( k = \sqrt{(M_{12}M_{21})/(L_{12}L_{21})} \)
\( \alpha_2, \alpha_1 \) - interpolation constants
\( d \) - effective skin depth
\( d_{\text{avg}} \) - averaged diameter of the inductor
\( \delta \) - skin depth
\( \epsilon_{\text{ox}} \) - oxide permittivity
\( \epsilon_{\text{sub}} \) - substrate permittivity
\( K1, K2 \) - interpolation constants
l - length of the inductor
μ₀ - permeability of free space
n - number of turns
ρ_{sub} - resistivity of the substrate
s - inductor track spacing
σ - metal conductivity
t_{ox:M1M2} - oxide thickness between top metal and underpass
t_{ox:M1} - oxide thickness between top metal and substrate
t_{sub} - substrate thickness
t_{M1} - inductor metal thickness
w - inductor track width

Chapter 4

\( g_m \) - transistor transconductance
\( g_{ds} \) - transistor output resistance
\( \gamma \) - error factor in secondary current
\( k \) - coupling coefficient \( k = \sqrt{(M_{12}M_{21})/(L_{12}L_{21})} \)
\( r_{\pi} \) - bipolar base resistance

Chapter 5

\( \beta(j\omega) \) - feedback factor
\( A_v \) - forward gain
\( \Gamma_{IN} \) - input reflection coefficient
\( \Gamma_L \) - load reflection coefficient
\( Z_0 \) - standard impedance 50Ω
\( Z_{IN} \) - input impedance
\( Z_L \) - load impedance

Chapter 6

\( k \) - Boltzmann constant \( 1.38 \times 10^{-23} \text{J/K} \)
\( T \) - temperature
\( r_{\pi} \) - bipolar base resistance
\( \gamma \) - empirical noise factor depending on process
\( \delta \) - empirical noise factor depending on process
\( q \) - electron charge \( 1.6 \times 10^{-19} \text{C} \)
\( I_B \) - bipolar base bias current
\( I_C \) - bipolar collector current
\( K_1 \) - empirical noise factor depending on process
\( NF \) - noise figure
\( THD \) - total harmonic distortion
$k$ - coupling coefficient between primary and secondary

$IP3$ - third order intercept point
Chapter 1

Introduction

1.1 Overview

The annual worldwide sales of cellular phones have exceeded $2.5B. The global positioning system is already a $5B market. In Europe, the sales of equipment and services for mobile communications have reached $30B. Despite the economic situation of 2002, the radio frequency (RF) and wireless markets will continue to expand as their size and complexity are driven by population growth. As a natural consequence, the research interest in the design and optimization of integrated building blocks and radio-transceivers has observed continuous growth. Passive elements such as inductors, capacitors, and transformers play a critical part in today’s transceivers. In this work we will focus on methods for improving the effective quality of on-chip spiral inductors, and we will present a novel active method which, with some trade-offs, brings the quality of spiral inductors to arbitrarily high-values.

In the development of integrated circuits, passive devices have traditionally played a minor role in comparison with active devices. The most obvious reason is the area requirement. Active devices are continuously down-scaling while passive devices remain large. At low frequency designers emulated passive functionality with active components to make their products more area and cost-effective.

When low loss, high-quality devices were needed, they were usually connected externally on-board rather than on-chip. This is possible as long as few external
components are needed and the package parasitics are negligible in comparison with characteristics of the external device at the operating frequency.

Inductors and transformers play a decisive role in the performance of circuits operating at high frequencies. Emulated active inductors employing several transistors are difficult to realize at higher frequency as the gain of active devices drops and the stability and linearity problems become severe. In addition, actively emulated inductors have a finite dynamic range, require voltage supply range to operate and inject additional noise into the circuits.

1.2 Applications of Passive Devices

There are several important applications of passive devices in wireless building blocks. One such example is narrow-band matching. Impedance matching allows circuit designers to obtain minimal noise, maximum gain, minimal reflection and optimal efficiency when designing circuit building blocks such as low-noise amplifiers (LNAs) and mixers.

Passive devices may be required to generate an LC tuned load. A tuned load can replace a resistive load to obtain gain at high frequency. The advantages are clear as an LC circuit is less noisy than a resistor, consumes less voltage supply range, and obtains a larger impedance at high frequency since a resistive load is always limited by the RC time constant which limits the frequency response. Tuned loads are also a critical component of oscillators. The LC parallel circuit sets the center frequency of the oscillator. A high quality low loss LC circuit yields oscillators with low power consumption and superior noise performance.
Another example is inductor degeneration or series-feedback. Series feedback can be used to increase or match the input impedance, stabilize the gain, and lower the non-linearity of an amplifier.

Inductors and capacitors can be used to realize a low-pass filter. Filters of this type are superior to active filter realizations such as gm-C or MOSFET-C filters as they operate at higher frequencies, have higher dynamic range due to the intrinsic linearity of the passive devices and inject less noise while requiring no DC power to operate.

A center-tapped transformer serving as a balun may be used to convert a differential signal into a single-ended signal to drive external components. Differential operation is advantageous in the on-chip environment due to the intrinsic noise rejection and isolation. Off-chip components, such as surface acoustic waves filters, are single-ended and a balun is needed to convert external single-ended signals to on-chip differential signals.

Finally, inductors and capacitors can be employed to form an artificial transmission line in a distributed (travelling wave) amplifier. Since the LC network acts like a transmission line, it has a broadband response. A wave propagating on the gate-line is amplified and transferred onto the drain line. If the wave speed on the drain line matches the gate line, the signals on the drain line add in phase and the drain line delivers power into a matched load.
1.3 Contributions of This Work

In the beginning chapters of this work we review the passive methods for producing high quality inductors and we propose a new layout optimization algorithm.

In the subsequent chapters we propose a method of producing a high quality inductor by looking at the input of the primary winding of a transformer with the secondary driven by a current appropriately related to the input signal. This technique generates a compensated passive rather than an active inductor. The electrical, noise and distortion properties of this circuit are presented. A method to employ this circuit in a buffered voltage controlled oscillator (VCO) with reduced power consumption is also presented.
Chapter 2

On-chip Passive Devices Background

2.1 The Quality of Passive Devices

To perform a study of integrated on-chip passive devices one has to define the performance indices for the quality of a passive device. In general, the complex power delivered to a one-port network at some frequency is given by [1]:

$$P = \frac{1}{2} \int_S E \times H \cdot ds = P_l + 2j\omega(W_m - W_e)$$  \hspace{1cm} (2.1)

where $P_l$ represents the average power dissipated by the network and $W_m$ and $W_e$ represent the time average of the stored magnetic and electric energy. One can define the input impedance as follows [1]:

$$Z_{in} = Z = R + jX = \frac{V}{I} = \frac{VI^*}{|I|^2} = \frac{P_l + 2j\omega(W_m - W_e)}{\frac{1}{2}|I|^2}$$  \hspace{1cm} (2.2)

If $W_m > W_e$ the device exhibits an inductive characteristic. If $W_m < W_e$ the device exhibits a capacitive characteristic. If $W_m = W_e$ the device exhibits a resistive characteristic.

The quality factor is the traditional measure of how the behaviour of a real passive device resembles the ideal case. It has the following general definition:
2.2 Loss Mechanisms

\[ Q = 2\pi \frac{E_{\text{store}}}{E_{\text{diss}}} \]  \hspace{1cm} (2.3)

where \( E_{\text{store}} \) is the maximum energy stored per cycle whereas \( E_{\text{diss}} \) is the energy dissipated per cycle. Implicit in the above definition is that device is excited sinusoidally. From (2.2) with \( T \) equal to the cycle time

\[ Q = 2\pi \frac{(W_m + W_e)}{P_l \cdot T} = \frac{\omega(W_m + W_e)}{P_l} \]  \hspace{1cm} (2.4)

The higher the Q factor, the lower the loss of a passive device. This definition is useful for characterizing inductors, transformers or capacitors as such devices are meant to store energy while dissipating little to no energy in the process. Thus ideal inductors and capacitors have infinite \( Q \) whereas practical devices have finite \( Q \). Applying the above definition to an ideal inductor \( L \) where \( W_e = 0 \), in series with a resistor \( R \), one obtains \( Q = \omega L/R \) and similarly for an ideal capacitor \( C \) where \( W_m = 0 \) in series with a resistor, \( Q = (\omega CR)^{-1} \).

2.2 Loss Mechanisms

To understand how the quality of an integrated passive device may be degraded the loss mechanisms should be analyzed. The Q factor of integrated passive devices is largely a function of the material properties used to construct the integrated circuits (ICs). The loss mechanisms are typically:
2.3 Metal Losses

- finite conductivity of the metal
- proximity effects due to presence of a nearby metal segment
- current crowding at the edge due to skin effect
- metal segments coupled magnetically and electrically through oxide or air
- substrate injection
- substrate current by ohmic eddy and displacement currents
- lateral currents in the substrate to substrate taps

2.3 Metal Losses

Passive devices such as inductors and capacitors are constructed from layers of metal, typically aluminum, and polysilicon layers. Hence, the conductivity of metal and polysilicon layers plays an integral part in determining the Q factor of such devices especially at lower frequencies. For instance a capacitor is constructed by placing two metal plates in close proximity. Reactive energy is stored in the electric field formed by the charges on such conductors. Since the metal layers are not infinitely conductive, energy is lost to heat in the volume of the conductors. This loss can be represented by a resistor placed in series with the capacitor. Similarly, an inductor is wound using metal conductors of finite conductivity. Most of the reactive energy is stored in the magnetic field of the device, but energy is lost to heat in the volume of the conductors.

Fig. 2.1 shows a cross-section of the metal layers of a typical CMOS process. Most processes come with three or more interconnection metal layers. This may include one or two layers of polysilicon as well. A typical CMOS process may include
six metal layers, with the thicker top metal layer separated from the substrate by approximately 10\(\mu m\) of oxide.

The metal layers are constructed from aluminum which has a room temperature conductivity of \(\sigma = 3.65 \cdot 10^7 S/m\). Typical metal layers have a thickness ranging from .5\(\mu m\) to 4\(\mu m\), resulting in sheet resistance values from 55\(m\Omega/\square\) to 7\(m\Omega/\square\). Even though silver, copper, and gold are more conductive, with \(\sigma_{Ag} = 6.21 \cdot 10^7 S/m\), \(\sigma_{Cu} = 5.88 \cdot 10^7 S/m\) and \(\sigma_{Au} = 4.55 \cdot 10^7 S/m\), aluminum is the more compatible metal in the IC process. Electromigration in Al is another problem, setting an upper bound on the maximum safe current density. Although electromigration with AC currents is less problematic, it remains one of the important limitations preventing integration of ”high power” passives on Si, such as matching networks at the output of a power amplifier. The necessary metal width would require excessively large areas resulting in low self-resonant frequencies.

Many IC processes targeting wireless communications integrated circuits are now
providing a thick top-metal layer option for constructing inductors. Such a metal layer is also useful for high speed digital building blocks and clock lines and thus this option is widely available in digital processes as well. This top metal layer may also reside on top of a thick insulator to ensure minimum parasitic capacitance. The modern multimetal IC processes opened up the possibility of designing structures with many different layers and sophisticated geometries.

At increasingly higher frequencies the current distribution in the metal layers changes, even in the absence of the substrate, due to eddy currents in the metalization, skin and proximity effects, current constriction, and current crowding. At any given frequency alternating currents take the path of least impedance. Currents tend to accumulate at the outer layer or skin of conductors since magnetic fields of the device penetrate the conductors and produce opposing electric fields within the volume of the conductors. When the effective cross-sectional area of the conductors decreases at increasing frequencies, the current density increases, converting more energy into heat. For an isolated conductor, the magnetic fields originate from the conductor itself (the self-inductance). This increase in AC resistance is known as skin effect and typically follows a $\sqrt{f}$ dependence. This rate of increase can be traced to the effective depth of penetration $\delta$ of the current since the effective area is a function of the skin depth

$$\delta = \sqrt{\frac{2}{\omega \mu \sigma}}. \quad (2.5)$$

In a multi-conductor system, the magnetic field in the vicinity of a particular
conductor can be written as the sum of two terms, the self-magnetic field and the neighbor-magnetic field. Thus the increase in resistance of any particular conductor can be attributed not only to skin effect but also to proximity effects, the effect of nearby conductors. If nearby conductors enhance the magnetic field near a given conductor, the AC resistance will increase even further and this is the case for a spiral inductor. On the other hand if the nearby fields oppose the field of a given conductor as is the case of the transformer the AC resistance will decrease as a result.

2.4 Substrate Losses

Integrated passive devices must reside near a lossy Si substrate. The substrate is a major source of loss and frequency limitation which is a direct consequence of the conductive nature of Si as opposed to the insulating nature of GaAs. The Si substrate resistivity varies from $10^{23} \text{atoms/cm}^3$ to $0.001 \text{cm}$ for heavily doped Si ($10^{20} \text{cm}^3$). In fact, to combat these substrate induced losses, some researchers propose removing the substrate from under the device by selective etching.

The conducting nature of the Si substrate leads to various forms of loss, namely conversion of electromagnetic energy into heat in the volume of the substrate. To gain physical insight into the problem, we can delineate between three separate loss mechanisms. First, electric energy is coupled to the substrate through the displacement current. This displacement current flows through the substrate to nearby grounds, either at the surface of the substrate or at the backplane of the substrate. Second, induced currents flow in the substrate due to the time-varying solenoidal
electric fields which induce substrate currents. The electrically induced currents flow vertically or laterally, but perpendicular to the spiral segments. Eddy currents flow parallel to the device segments.

Finally, all other loss mechanisms can be lumped into radiation. Electromagnetically induced losses occur at much higher frequencies where the physical dimensions of the device approach the wavelength at the frequency of propagation in the medium of interest. This frequency is actually difficult to quantify due to various propagation mechanisms of the substrate. If propagation into the air is considered, the free-space wavelength is the appropriate factor. However, even at 100 Ghz the wavelength of propagation is ten times longer than any RF inductor or capacitor and therefore propagation in air may be ignored.

Efficient electromagnetic propagation into the substrate occurs at lower frequencies due to the lower propagation speed, roughly at a factor $\sqrt{\varepsilon_r}$ lower due to the diamagnetic nature of Si. Since $\varepsilon_r \approx 11.9$ in Si, this is slightly slower than propagation in air. Furthermore, due to the lossy nature of the substrate, waves travelling vertically into the surface of the substrate can propagate partially in the lossless oxide and partially in the substrate. As the substrate is made heavily conductive, the wave is constrained to the oxide and the substrate acts like a lossy ground plane.

### 2.5 Si IC Process Substrate Structure

The substrate of both CMOS and bipolar processes consists of one or more layers of Si or a compatible material and conductive layers. Layers of varying conductivity are added to the bulk substrate by various fabrication processes, such as diffusion,
chemical vapor deposition and growth, epitaxy, and ion implantation. Various layers of oxide ($SiO_2$ for instance) and polymide are also grown to provide insulation from the substrate and between the metal layers.

In general, the more conductive the substrate layers the more detrimental the resulting losses. It is therefore no surprise that intrinsic Si substrates result in the lowest losses. Due to the close proximity of the Si substrate to the inductors and transformers residing in the metal layers, the case of an infinitely conductive substrate is also problematic. For a heavily conductive substrate, the magnetic and electric fields do not penetrate the substrate appreciably and even though no substrate induced losses occur, the surface currents flowing in the substrate acting like "ground-plane" currents producing opposing magnetic fields which tend to drive the inductance value of coils to low, non-usable values. The capacitors would also have considerable parasitic losses to ground and therefore the substrate is usually covered by an epitaxial layer to prevent such effects.

Therefore, given the choice, designers of ICs and process engineers should ensure that as few as possible conductive substrate layers appear under or near an inductor. This is unfortunately not always possible due to planarization constraints. Furthermore the thickest possible oxide should be realized under the device to minimize the substrate capacitance. This not only minimizes the losses, but also maximizes the self-resonant frequency of the device. In the limit, self-resonance will occur due to interwinding capacitance as opposed to substrate capacitance. Since interwinding capacitance can be controlled by increasing the metal spacing, this gives the IC designer more control over the passive device behavior.

Most bipolar and BiCMOS substrates come with a standard resistivity value of
10 – 20$\Omega cm$. With this value of resistivity, electrically induced losses dominate the substrate losses in the 1-10 GHz frequency range. This is also the case for bulk CMOS substrates with the same range of resistivity. In such a case one must ensure that no conductive n or p wells appear below the device. This may require a special mask to block the dopants in the well creation, especially for a twin well CMOS process. To minimize the chance of latch-up, many modern CMOS logic processes begin with a heavily conductive thick substrate about 700$\mu m$ thick and grow a thin epitaxial layer of resistive Si on the surface to house the wells. This is unfortunate for RF/microwave circuits as the bulk substrate can be as conductive as $10^4 S/m$ and this can be a major source of substrate induced loss due to eddy currents and electric losses to the substrate. As a result most CMOS process come with a substrate option. Fig. 2.2 shows the differences between the two substrates.

![Figure 2.2: Non-epitaxial and epitaxial CMOS substrates](image)

The backplane of the substrate may or may not be grounded. Even if it is physically grounded for DC signals, AC signals are constrained to flow within several skin depths $\delta$ and this factor is a strong function of the conductivity. For heavily conductive substrates, currents are constrained to flow at the surface of the substrate.
at high frequencies whereas for moderately conductive substrates currents flow deep into the substrate and into the backplane ground.

In the test fixtures to be presented the ground plane was physically realized by using a conductive silver epoxy to cement the chip to the ground metal plane on the surface of the board.

Unless the substrate thickness is reduced substantially, the conductive backplane ground is sufficiently distant not to appreciably influence the electromagnetic behavior of the inductor.
Chapter 3

Passive Methods for Improving The Quality of On-chip Inductors

3.1 Process Methods for Improving On-Chip Passives

In order to reduce the metal and substrate induced losses many research efforts have been aimed at modifying the IC process to minimize losses. Using thick and more conductive metallization minimizes the low frequency losses whereas using a high resistivity substrate along with a thick oxide layer minimizes the substrate losses. Naturally, using an oxide with a lower dielectric constant or eliminating the substrate as a coupling media to ground reduces the losses as well. Another approach is to attempt to realize a lateral coil on-chip by using the top and bottom metal layers and vias as the side. This approach has been successfully demonstrated in [2] using special post-processing steps to realize sufficient cross-sectional area in the coil. This approach has the added advantage of positioning the magnetic fields laterally to the substrate where eddy currents are reduced. In a vertical coil or spiral, the magnetic field is strongest at the center of the coil. Due to the finite conductivity of the substrate the changing magnetic fields leak into the substrate and produce eddy currents. Eddy current can be a significant source of loss and the lateral coil technique might be an effective method to combat this loss mechanism. Standard monolithic integration, however, has failed to produce a lateral coil with sufficient
cross-sectional area to produce significant Q. Some innovative strategies related to the lateral coil idea employ a combination of metal and bond wires to realize the coil. The work presented in [3] claims tight tolerance on the inductance value which is a primary concern when using bond wires. An interesting alternative is presented in [4]. To reduce the coupling to the substrate an insulating core is grown on top of the passivation layers of the IC chip. This insulating core is wrapped with traces of metal to create a 3D solenoid on top of the chip with its axis parallel to the backplane of the chip. Q factors as high as 13 at 900 MHz for a 2.6 nH inductor may be obtained.

3.2 Layout Methods of On-Chip Passives

In this section we will discuss various ways to lay out inductors using the planar metallization layers of a typical IC process. Off-chip inductors are usually realized as a solenoidal coil or toroid. Each additional turn adds to magnetic field in phase with the previous turn. The magnetic energy is generated mostly in the inner core of each winding. The inductance is largely a function of the area of the loop and the number of turns in the winding typically resulting in an $N^2$ dependence.

![Figure 3.1: Square and Spiral Inductors](image)
Since on-chip inductors are constrained to be planar, the typical solution is to form a spiral, as shown in Fig. 3.1. A square spiral is a popular alternative especially since some processes restrict designers to use 90° layout angles. A polygon spiral is a compromise between a purely circular spiral and a square spiral.

In designing integrated circuits an enhanced quality inductor can be generated by centertapping an inductor to better exploit the mutual inductance properties. To perform centertapping one has to find a symmetry center. In a simple spiral such as shown in Fig. 3.1 it is difficult to find such a point since the resulting half spirals have inherently slightly different geometries and thus slightly different electrical properties.

To solve this problem some researchers have proposed symmetric structures, such as that shown in Fig. 3.2. Note that each turn involves a metal-level interchange, a process that requires vias. A different center-tapped structure proposed in [5] requires only one metal interchange. These structures have a natural geometric center which coincides with the electrical point. This center is needed in differential circuits as such points can be grounded or connected to supply without disturbing the differential signal. Circular or polygon versions are also possible.
In the modern multi-metal processes it is natural to investigate whether or not the quality of inductors can be improved by using several layers. Two simple approaches in utilizing the metal layers are to connect multiple spiral inductors in series or in shunt. While $N$ spirals in series increase the series resistance approximately $N$ times (neglecting via resistance), the inductance value increases faster due to the mutual magnetic coupling. At low frequencies where the current flowing through each series connected spiral $I_j$ is equal, the effective inductance of $N$ series connected coupled inductors is:

$$L_{se} = \sum_{i=1}^{N} L_i + 2 \sum_{i=1}^{N} \sum_{j \neq i} M_{ij}$$  \hspace{1cm} (3.1)

where $M_{ij}$ is the mutual magnetic coupling between each series connect spiral $i$ and $j$. Thus the series connection approaches an $N^2$ increase in inductance and the $Q$ factor can potentially increase by a factor of $N$ for the case of perfectly coupled spirals ($k=1$).

Alternatively, in the shunt connection the series resistance drops by a factor of $N$ (assuming equal resistivity in each metal layer and uniform current distribution among the coils) whereas the inductance of mutually coupled inductors drops to

$$L_{sh} = \frac{1}{\sum_{i=1}^{N} \sum_{j=1}^{N} 1/K_{ij}}$$  \hspace{1cm} (3.2)

where the matrix $K$ is the inverse of the mutual inductance matrix $M$. This result certainly agrees with the case of a diagonal matrix $M$ corresponding to zero coupling.
3.2 Layout Methods of On-Chip Passives

since in such a case we have the familiar result for parallel inductors

\[ L_{sh} = \frac{1}{\sum_{i=1}^{N} \frac{1}{M_{ii}}} . \] (3.3)

For the case of two coupled inductors we have a simpler relation:

\[ L_{sh} = \frac{1}{2} \frac{L_1L_2 - M^2}{L_1 + L_2 - 2M} . \] (3.4)

For the case of perfectly coupled equal inductors, with \( k = +1 \), the above results yield \( L_{sh} = L \). For the general case the matrix \( M \) is singular but by symmetry the current flowing through all inductors is equal so the voltage across the \( j \)th inductor is:

\[ V_j = \sum_{k=1}^{N} sM_{jk}I_k = \frac{I}{N} \sum_{k=1}^{N} sM_{jk} = \frac{I}{N} sL \sum_{k=1}^{N} 1 = sLI \] (3.5)

and so we have

\[ L_{sh} = L_1 = L_2 = \ldots = L_N . \] (3.6)

In the case of perfectly coupled equal inductors the Q factor also improves by a factor of \( N \) due to drop in series resistance. In practice, both the series and shunt connection offer a Q improvement close to the theoretical limit due to the tight coupling achievable in the on-chip environment. These benefits, however, only occur
at low frequencies where the above assumptions hold.

At high frequencies, both approaches may in fact reduce the quality over the case of a single layer coil due to the capacitive and substrate effects. The series connection suffers from high interwinding capacitance which lowers the self-resonance frequency. The shunt connection moves the devices closer to the substrate where capacitive current injection into the substrate may dominate the loss of the device. Only sophisticated and time consuming simulations may clarify what is the optimum number of layers that should be shunted to produce a higher quality inductor and when the substrate losses will start to dominate. Unfortunately this raises a predictability issue. The tolerances on the inter-metal dielectric layer thicknesses are up to 20% and therefore the inductor performance should be, by design, independent of the distance to the substrate.

Another way to minimize substrate losses while maintaining metallic losses constant is to use a tapered inductor. A tapered spiral is shown in Fig. 3.3. The metal pitch and spacing are varied to minimize the current constriction at high frequency. Current constriction, or skin effect, is non-uniform as a function of the location in the spiral due to the non-uniformity of the magnetic field. At low frequencies the current is nearly uniform whereas at high frequency non-uniform current flows due to proximity effects.

The magnetic field is strongest in the center of the spiral, and thus the time varying magnetic field produces eddy currents of greatest strength in the volume of conductors near the center of the device. Since at high frequency current constriction limits the current to the outer edges of the conductors, conductor width does not have as strong an influence on minimizing metal losses as at low frequency. Therefore
the radius of the inner spiral turns should not be too small. Another approach is to decrease the width of the inner turns and to effectively move these turns closer to the outer edge.

Tapering can be an effective method for increasing the self resonant frequency of a device since it maintains the inductance while reducing the cross-sectional area.

3.3 Transformers

On-chip transformers are generated with planar spiral structures just as inductors. To maximize the coupling factor $k$, two inductors can be interwound to form transformers. These transformers have equal turns ratio at the primary and secondary. Since the turns ration $n$ is given by:

$$n = k \sqrt{\frac{L_2}{L_1}}$$

one way to make $n$ different from 1 is to alter the number of turns and metal pitch in the secondary. Coupling factors close to 0.9 can be achieved with planar spirals.

If center tapped-transformers are desired, such as in a balun, a structure such
3.4 Patterned Ground Shields

In an attempt to shield a device from substrate losses, researchers have proposed building a shield with metal layers or polysilicon layers to block electromagnetic energy from coupling to the substrate. While electrostatic shielding works well for capacitors and RF pads, especially at "low-frequencies", the shield must be patterned in the case of inductors so as to avoid or reduce the effects of eddy currents in the shield. Due to the close proximity of the device and the shield, using solid metal-
Figure 3.6: Frlan Transformer

lization would allow image eddy currents to flow which would produce an opposing magnetic field. This would reduce the device magnetic energy storage and hence the Q factor. A patterned shield similar to Fig. 3.7 only allows shield currents to flow perpendicular to the conductive paths of a spiral inductor, thereby preventing the majority of eddy currents which flow parallel to the device.

The effects of a shield, or any other grounding structure can be analyzed with the EM simulators presented in this work. At first glance a patterned shield seems like a very effective means of improving the device.

However, consider a simplified on-chip inductor model with a lossy inductor and a parasitic lossy capacitor, $C_s$ in series with a loss resistor $R_s$ as shown in Fig. 3.8. Then the action of the shield is to effectively increase the $Q_C$ factor of the capacitor portion of the equivalent circuit. Consider a series to parallel transformation of this lossy capacitor into $C_p$ in shunt with $R_p$.

\[
R_p = (1 + Q_C^2)R_s 
\]

\[
C_p = \frac{Q_C^2}{1 + Q_C^2}C_s
\]
3.4 Patterned Ground Shields

Figure 3.7: Inductor with a grounded patterned shield

Figure 3.8: Patterned Grounded Shield (PGS) effect
Suppose that without a shield the $Q_C$ factor of this capacitor is very low i.e. $R_s$ is very high, $Q_C << 1$, such that

$$R_{\text{low}Q} = (1 + Q_C^2)R_s$$  \hspace{1cm} (3.10)

$$C_{\text{low}Q} = Q_C^2C_s$$  \hspace{1cm} (3.11)

If $R_{\text{low}}$ is then already larger than the parallel equivalent inductor loss resistor then this capacitor plays a minor role in determining the overall $Q$ and shielding will actually deteriorate the performance of the device. Note that since $C_{\text{low}} << C_s$, the effective shunt capacitance is small and does not lower the self-resonant frequency of the device. Clearly, in this case shielding does not help. Now consider the other extreme where the resistor $R_{\text{low}}$ loads the tank significantly. Then clearly increasing the capacitor $Q_C$ factor helps, since for $Q_C >> 1$

$$R_{\text{high}Q} = Q_C^2R_s$$  \hspace{1cm} (3.12)

$$C_{\text{high}Q} = C_s$$  \hspace{1cm} (3.13)

This occurs, on the other hand, at the expense of lowered self-resonance since now the parasitic capacitor loads the tank. So we see the shield may potentially improve the overall tank $Q$ but at the cost of reducing the usable frequency range of the device. Another approach, discussed in [6] surrounds the device with an open halo of substrate contacts. This has the added benefit of increasing the capacitor
Another potential problem with the shield arises due to finite non-zero ground inductance. Since most packaged IC’s suffer both package and bond wire inductance, the actual zero potential resides off-chip and there is considerable “ground bounce” on-chip. A typical IC has several inductors and transformers and if they are shielded, they are all effectively tied to a common non-zero impedance point. Thus a parasitic coupling path exists from device to device.

For instance, in an amplifier, this intra-block leakage can either lower the gain (as negative feedback) or cause instability (as positive feedback). Inter-block coupling, on the other hand, can produce spectral leakage, spurs and reduced SNR.

The parasitic substrate coupling is an issue to be considered in all packaged ICs. However patterned ground shields tend to worsen this problem as the substrate capacitance value is increased and the resistive isolation lowered.

### 3.5 Optimization of Inductor Circuits

It was shown that the complicated loss mechanisms associated with spiral on-chip inductors limit the circuit performance and make design optimization difficult. Currently, designers are limited to using a library of previously fabricated inductors or using a 3D field solver such as ASITIC [7], HP ADS Momentum, Cadence Passive Modeller or ANSOFT HFSS. The former method is a severe constraint on the design optimization and the latter requires a considerable computational effort and raises a flexibility issue. In many cases, inductor circuit performance is dependent on both passive and active components surrounding the inductor. Therefore, using a passive
modeler based on a 3D field solver, to optimize the circuit leads the designer to an optimization based on brute force or trial and error. Field solvers are better suited for fine tuning and analysis of circuits rather than for use in the first stages of the design.

Hershenson et al. [8] have proposed an optimization with constraints method based on geometric programming. This method requires modelling of the inductor circuit using equations of a specific posynomial shape, which means every constraint and optimization objective has to be written as a positive sum of monomials with real powers. Although a large class of functions can be approximated using posynomials the designer is forced to put valuable time into shaping the equations while preserving the precision of the model.

### 3.6 Gradient descent vs geometric programming

This thesis proposes constrained gradient descent optimization as an alternative to geometric programming, using ASITIC as the validation tool. Unlike geometric programming which yields a stable global optimum if it exists, the gradient descent may yield a local optimum and the solution is dependent on the initial condition. However the constraints and the optimization objective functions may take any smooth differentiable shape. It may be easier for the designer to vary the initial condition and allow small variations in the constraints in order to improve convergence rather than lose precision and fight with the equation shape using geometric programming. A gradient descent constrained optimization can be easily implemented in the MATLAB optimization toolbox using the `constr` function or more recently
The losses in an on-chip inductor are due to a variety of mechanisms such as metal resistance, skin effect, proximity effect, substrate losses and eddy currents. These losses are a complicated function of the inductor geometry, which is defined by the outside diameter, the track width, the spacing between tracks, the number of turns, and a multitude of process parameters.

The widely accepted spiral inductor model is the broadband $\pi$ - model shown in Fig. 3.9. ASITIC uses a narrowband $\pi$ - model shown in Fig. 3.10. The two models can be compared at a particular frequency using parallel to series and series to parallel transformations.

A variety of formulas may be employed to estimate $L_s$. $R_s$ is usually modelled to
include skin effect and $C_s$ is approximated as a parallel plate estimation between the spiral metal and underpass metal and an interwinding component [10], [11], [12]. A commonly used set of equations for the $L_s$, $R_s$, $C_s$ portion of the circuit is given in equations 3.14, 3.15, 3.16. The list of symbols of this thesis describes each of the variables used in this section.

\[
L_s = \frac{K_1\mu_0n^2d_{\text{avg}}}{1 + K_2\delta} \quad (3.14)
\]
\[
R_s = \frac{1}{\sigma w\delta(1 - e^{t_{M1}/\delta})} \quad (3.15)
\]
\[
C_s = \frac{\varepsilon_{ox}nw^2}{t_{oxM1M2}} + \frac{\varepsilon_{ox}t_{M1}(n - 1)t}{t_{oxM1M2}} \quad (3.16)
\]

The substrate losses represented by the $C_{s1,2}$, $C_{s1,2}$, $R_{s1,2}$ in Fig. 3.9 branches are very important as they reduce the Q of the inductor at high frequencies, especially above 3GHz.

So far these losses have been approximated using a parallel plate estimation.
However comparing the parallel plate estimation with ASITIC evaluations shows that a correction is needed.

### 3.8 Substrate losses correction

In order to estimate the substrate losses more accurately, these losses shown in Fig. 3.11(a) were decomposed into parallel plate losses (Fig. 3.11(b)) and two-wire losses (Fig. 3.11(c)). This accounts for the losses underneath the inductor tracks as well as the fringing losses.

![Figure 3.11: (a), (b), (c) Decomposition of losses](image)

<table>
<thead>
<tr>
<th>Loss</th>
<th>Simple</th>
<th>Improved</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{ox}$</td>
<td>$\frac{\varepsilon_{ox} l_w}{2t_{oxM1}}$</td>
<td>$\frac{\varepsilon_{ox} l_w}{2t_{oxM1}} + \frac{4\alpha_1 \varepsilon_{ox} d_{avg} \pi}{\cosh^{-1}(2t_{sub}/d)}$</td>
</tr>
<tr>
<td>$C_{si}$</td>
<td>$\frac{\varepsilon_{sub} l_w}{2t_{sub}}$</td>
<td>$\frac{\varepsilon_{sub} l_w}{2t_{sub}} + \frac{4\alpha_2 \varepsilon_{sub} d_{avg} \pi}{\cosh^{-1}(2t_{sub}/d)}$</td>
</tr>
<tr>
<td>$R_{si}$</td>
<td>$\frac{2\rho_{sub} l_w}{l_w}$</td>
<td>$2\left(\frac{\varepsilon_{sub} l_w}{2\rho_{sub} l_w} + \frac{4\alpha_2 d_{avg} \pi}{\rho_{sub} \cosh^{-1}(2t_{sub}/d)}\right)^{-1}$</td>
</tr>
</tbody>
</table>

**Table 3.1: Modelling Equations**

The diameter of the approximating wire is proportional to the skin depth and the two-wire losses are approximated using the method described in [13] and the
3.9 Optimization Problems

Once an accurate analytical model for the spiral inductor has been established some
synthesis problems can be addressed. A gradient descent optimization with con-
straints was coded in Matlab making use of the constr function. The mathematical
objective and constraints of the problem are similar to those presented in [8] but the

method of images. Table 3.1 shows the simple and improved equations for the
substrate losses. Table 3.2 shows the difference made by these corrections in a
standard CMOS process. To see why the two wire losses configuration was chosen
consider the following configuration: an inductor track 10μm wide on top of an
8μm thick oxide on top of a 700μm thick Si substrate. Assuming the back-plane
assumption holds (i.e. the back plane of the substrate is grounded) the inductor
track is essentially a microstrip line above a ground plane. Using the method of
images the microstrip line field will fringe as a fraction of the two wire transmission
line field with Si dielectric in between. This fraction, represented by coefficients
α₁ and α₂ is technology dependent and can be easily determined using ASITIC. A
standard CMOS process requires α₁ =0.3 and α₂=0.6. Note, however that in many
design situations the substrate losses are shorted by using a ground shield which
mildly improves the Q of the inductor but lowers the self resonant frequency [14].
The presence of substrate contact halos [6] would also make these substrate loss
equations invalid. Also note that these substrate losses do not significantly affect
the Q of the inductor at frequencies of up to 3GHz and therefore the validity of the
results obtained in [10], [14] is not affected.
3.9 Optimization Problems

<table>
<thead>
<tr>
<th>f (GHz)</th>
<th>Geometry</th>
<th>ASITIC</th>
<th>Simple Model</th>
<th>Improved Model</th>
</tr>
</thead>
<tbody>
<tr>
<td>l, w, s, n (µ m)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C_{sub}(fF)</td>
<td>R_{sub}(Ohm)</td>
<td>C_{sub}(fF)</td>
<td>R_{sub}(Ohm)</td>
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<td>10</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
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<td>250</td>
<td>20</td>
<td>1</td>
<td>2</td>
</tr>
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<td>1</td>
<td>2</td>
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<td>10</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Table 3.2: Substrate losses estimated using various models

equations characterizing the inductor have been corrected as presented in Table 3.1.

An example optimization flow is described in Fig. 3.12.

3.9.1 Design of an inductor with maximized Q

This problem requires the geometry of an inductor of given L with maximum Q.

There are two paths to solve this problem. One path is to use ASITIC and do a brute force sweep using the \textit{optL} command. The second path is to perform a constrained optimization in Matlab. For a one port grounded inductor, the broadband model
described in Fig. 3.9 has to be substituted at the frequency of interest with the equivalent circuit described in Fig. 3.13.

![Circuit Diagram](image)

**Figure 3.13: One port grounded model**

Using parallel to series and series to parallel transformations it can be shown that:

\[
R_p = \frac{1 + \left[\frac{\omega R_{si1}(C_{si1} + C_{ox1})}{\omega^2 R_{si1} C_{ox1}^2}\right]^2}{\omega^2 R_{si1} C_{ox1}^2} \quad (3.17)
\]

\[
C_{tot} = C_{ox1} + \frac{\omega^2 R_{si1}(C_{si1} + C_{ox1}) C_{si1} C_{ox1}}{1 + \left[\frac{\omega R_{si1}(C_{si1} + C_{ox1})}{\omega^2 R_{si1} C_{ox1}^2}\right]^2} \quad (3.18)
\]

It can also be inferred that:

\[
Q = \frac{\omega L_s}{R_s} \cdot \frac{R_p(1 - \frac{R_s^2 C_{tot}}{L_s} - \omega^2 L_s C_{tot})}{R_p + \left[\frac{(\frac{\omega L_s}{R_s})^2}{1}ight] R_s} \quad (3.19)
\]

\[
f_{self} = \frac{1}{2\pi} \sqrt{\frac{1}{L_s C_{tot} - \frac{R_s^2}{L_s^2}}} \quad (3.20)
\]

where \(f_{self}\) is the self-resonant frequency.
The optimization problem is stated as:

*Maximize objective function:*

- \( Q \) - quality factor

*with constraints on:*  
- \( l, w, s, n \) - geometry  
  - \( L_s \) - inductance range  
  - \( f_{self} \) - self resonant frequency.

Both ASITIC optimization and Matlab constrained optimization yield optimized inductors with results compared in Table 3.3.

### 3.9.2 Design of an optimized LC tank

This problem requires to maximize the LC tank parallel loss resistance while maintaining a specified resonant frequency. In this case ASITIC cannot be used efficiently because the result is dependent on the tank capacitance and losses. Essentially the parasitics of the inductor may influence the resonant frequency as well as the \( Q \) of the tank in combination with the tank capacitance. Both the tank capacitance and the inductor geometry may vary. This is easy to specify within an optimization with constraints process but it is not controllable within ASITIC.

### 3.9.3 Other optimization problems

When designing inductors for LC tunable oscillators, the tuning range constitutes an additional constraint on the geometry of the inductor. The size of the inductor is limited by the variable capacitor and the quality of the resonating tank improves with an increased inductor size.

When designing shunt peaked amplifiers the inductor loss capacitance has to be minimized with a constraint on the time constant ratio of the loaded tank.
3.10 Predictability of Passive Pads

With minor modifications gradient descent optimization may be used to design circuits which involve inductors with patterned ground shields.

<table>
<thead>
<tr>
<th>Objective</th>
<th>f (GHz)</th>
<th>Model Synthesis</th>
<th>ASITIC L (nH)</th>
<th>ASITIC Q (nH)</th>
<th>ASITIC Synthesis l,w,s,n (µm)</th>
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<td>1.7</td>
<td>0.94</td>
<td>4.2</td>
</tr>
</tbody>
</table>

Table 3.3: The synthesis of optimized inductors

### 3.10 Predictability of Passive Pads

This section quantifies the ability to obtain precise simulations and thus predictions of the behaviour of passive elements in the CMOS process that was available for the fabrication of circuits.

The simplest configuration that one can imagine to be used to calibrate the simulators for the substrate of the given process is the measurement and simulation of open pads.

The 1-port S-parameter characterizes the input impedance of an open pad. It can be easily measured using a network analyzer and a wafer prober. The measurement procedure is simple and the measurement error is expected to be minimal.

In this work pads were chosen to be squares with a 100µm side length and with 150µm spacing to respect the wafer prober probe pitch. A gold bondwire connected the ground backplane with the ground pads. The pads were constructed with all the metal layers available in the process. The 3D structure that was measured is shown in Fig. 3.14.
There were two types of substrates available in the process, a mixed signal and a logic substrate as shown in Fig. 2.2(a) and (b). The pads were fabricated on an epitaxial CMOS logic substrate. In an epitaxial logic process the resistive losses are very high due solely to the small resistance of the epitaxial layer since the highly doped bulk is basically a short circuit. On a non-epitaxial mixed signal substrate the resistive losses are much smaller due to the thick high resistivity bulk silicon underneath the pad.

![Figure 3.14: Pads structure simulated (ANSOFT)](image)

If the process parameters are known a quick mathematical estimate for the pad model shown in Fig. 3.15 can be obtained using a parallel plate approximation,
using $R_{\text{sub}} = \frac{\rho_{\text{sub}} t_{\text{sub}}}{A}$, $C_{\text{ox}} = \frac{\varepsilon_{\text{ox}} A}{t_{\text{ox}}}$, $C_{\text{sub}} = \frac{\varepsilon_{\text{sub}} A}{t_{\text{sub}}}$. Unfortunately exact values cannot be presented because they are covered by a confidentiality agreement. Suffice it to say that the parallel plate estimation indicates slightly lower losses than the actual measured values due to second order phenomena such as fringing. Nevertheless the simple equations can be used as a starting point.

We shall investigate now to what extent powerful EM simulators can predict the measured behaviour of the pads. Three simulators were used to address the problem: HP ADS Momentum, ANSOFT HFSS, and Cadence passive modeler. The results from the Cadence passive modeler were significantly different from the other simulations and the measurements. These results are presented in a separate graph shown in Fig. 3.16. It is not certain the Cadence passive modeler would be suitable for simulating pads on a lossy epitaxial substrate but this experiment tends to suggest a negative answer.

Fig. 3.17 show the HP ADS Momentum and ANSOFT HFSS predicted response as well as the actual measured response of the pads. The plots describe the real and imaginary impedance as well as the input reflection coefficient. Several measurements were taken from different die and there were no noticeable differences. By analyzing the graphs presented there are several facts to be noted: the measured resistance of the pads is half of that predicted; the measured reactance of the pads is predicted within process tolerances. Because the reactance dominates, the impedance of the pads is predicted with reasonable accuracy.

A huge effort was put into reconciling the discrepancy with respect to the measured resistance. Most likely the cause of this discrepancy is an inaccurate description of the process given to the simulator i.e. the epitaxial layer is thinner or has higher
resistivity than actually assumed in the simulator. These suppositions led to trouble calls to our silicon broker but they eventually remained unanswered. It was accepted that an error will exist in prediction of passive elements behaviour. There is no scientific reason to modify the process information given by the foundry in order to obtain agreement between simulations and measurements.

The investigation of the pads was also revealing in terms of a simulator choice. ANSOFT HFSS, a 3D simulator based on the finite element method, required a high number of iterations in order to obtain convergence. The fact that the result was known, i.e. measured, was critical in appreciating whether a change in the convergence settings is needed or not. HP ADS Momentum is a 2.5D simulator based on the method of moments. This simulator was fast and robust without requiring

Figure 3.16: Simulated pad behavior (Cadence)
3.10 Predictability of Passive Pads

Figure 3.17: Real, Imaginary Impedance and Smith plot of the pads input reflection coefficient

too many additional specifications besides the process and the layout of the circuit. While the freedom given by a full 3D simulator such as ANSOFT HFSS needs to be appreciated, the author recommends the use of HP ADS Momentum for simulation of on-chip passives due to its robustness, speed and ease of use.
Chapter 4

Active Compensation Schemes for Spiral Inductors

4.1 Overview

Previous chapters have illustrated the efforts of improving the Quality of the spiral inductors using passive methods. Researchers have naturally asked the question whether active methods are a better solution to the Q-enhancement problem. Once active devices are used some of the more desirable properties of a passive device disappear. Transistors will consume power, add noise, limit the dynamic range and create potential instability. Different active schemes emulating improved inductors will exhibit different features and will be suitable for different applications. Two main active circuit strategies for eliminating losses in inductors have been published. The first strategy is to replace the inductor with active elements building an active inductor. The second strategy is to compensate the losses in an on-chip spiral inductor by wrapping active circuitry around it. Several successful attempts following this strategy employ an on-chip transformer and compensate the losses in the primary on-chip winding by exciting the secondary with the appropriate stimulus.

Although most of this work revolves around the second strategy a brief overview of strengths and weaknesses of active inductors is given.
4.2 Active Inductors

One implementation described in [15] of such an active inductor is shown in Fig. 4.1 a) using a gyrator and capacitor. The equivalent inductance can easily be calculated to be:

\[
L_{eq} = \frac{C_L}{g_{mi}g_{mv}}. \tag{4.1}
\]

Figure 4.1: A gyrator-based active inductor. (a) Circuit diagram. (b) Equivalent noise sources

Very high speeds can be achieved using modern processes. Active inductors have been demonstrated to work at 1 or 2 GHz [16]. Active inductors have the tunability advantage which may seem to make them suitable for an application such as a voltage controlled oscillator.

One major drawback of active inductors relates to achieving small \(L_{eq}\) without high currents required to obtain large \(g_m\). For example assuming \(C_L\) is 1pF in order to obtain a 10 nH \(L_{eq}\) the \(g_{mi}g_{mv}\) has to be \(0.1 \, m(A/V)^2\) and the \(g_m\)'s have to average 10 mA/V, a value difficult to obtain in most CMOS processes without significant
power consumption. Another major problem associated with active inductors is their noise contribution to the circuit. Noise is generated by both transconductors in the gyrator. The equivalent noise sources of an active inductor are shown in Fig. 4.1 b).

The equivalent input noise of each transconductor is represented by a voltage source \( dv_{gm}^2 \) of value \( 4kT F_{gm}/g_m df \), with \( g_m \) the transconductance value and \( F_{gm} \) a noise factor depending on the practical implementation. The inductor’s equivalent noise sources can be calculated to be [17]:

\[
\begin{align*}
\text{di}_L^2 &= 4kT \cdot F_{gmi} \cdot g_{mi} \cdot df \quad (4.2) \\
\text{dv}_L^2 &= 4kT \cdot \frac{F_{gmv}}{g_{mi}} \cdot df \quad (4.3)
\end{align*}
\]

It is shown in [15] that these noise sources have a destructive effect on phase noise if used in an oscillator making the gyrator based active inductor unsuitable for the application. Another good critique of active inductors may be found in [12] pp. 268-269.

### 4.3 Actively Compensated Spiral Inductors

The second strategy for creating high-Q inductors is to actively compensate the losses in a spiral inductor. Ideally we would like to keep the inductor isolated from the compensating circuitry to simplify the bias requirements and to ease connections with the rest of the circuit. The configuration that comes to mind is that of a transformer since there is high-frequency interaction between the windings of a transformer but no physical connection. As we shall see in the next section it is indeed possible
to compensate the losses in a spiral inductor as a primary winding of an on-chip transformer by appropriately stimulating the secondary.

4.4 Principle of operation

In Fig. 4.2 where the spirals are lossy it can be proven that for properly chosen $I_s = f(v_{in})$, $Z_{in}$ is purely imaginary i.e. a lossless inductor. This property is however frequency dependent.

Figure 4.2: Compensation principle

The on-chip transformer is modelled as shown in Fig. 4.3, [18].

Figure 4.3: Transformer model

Kirchhoff laws require:

$$v_{in} = I_p s L_p + I_p R_s + s I_s M_{sp}$$ (4.4)
To have \( Re\left(\frac{v_{in}}{I_p}\right) = 0 \), the following condition must be met:

\[
Re(R_{sp} + \frac{sI_sM_{sp}(R_s + sL_p)}{v_{in} - sI_sM_{sp}}) = 0.
\]  

(4.5)

Assuming \( I_s = (x + jy)v_{in} \) the condition that characterizes \( (x + jy) \) is:

\[
Re(R_{sp} + \frac{s(x + jy)M_{sp}(R_s + j\omega L_p)}{1 - s(x + jy)j\omega M_{sp}}) = 0
\]

(4.6)

In a simplified case we may obtain \( Re\left(\frac{v_{in}}{I_p}\right) = 0 \) requiring only:

\[
v_{in} = I_p sL_p
\]

(4.7)

\[
I_s = -\frac{I_p R_s}{sM_{sp}}
\]

(4.8)

In this case it can be inferred that

\[
I_s = \frac{v_{in} R_s}{\omega^2 L_p M_{sp}}.
\]

(4.9)

In general, \( M = k\sqrt{L_p L_s} \) where \( k \) is the coupling factor between the primary and secondary windings, typically 0.7 to 0.9 for monolithic transformers in Silicon. Thus the required secondary current becomes, in the general case

\[
I_s = \frac{v_{in} R_s}{\omega^2 k L_p \sqrt{L_p L_s}}.
\]

(4.10)

If we make a unity turns ratio transformer with \( L_p = L_s \) the required current
reduces to:

\[
I_s = \frac{v_{in} R_s}{k \omega^2 L_p} = \frac{v_{in}}{k Q^2 R_s^2}
\]

(4.11)

where \( Q \) is the quality factor of a coil with winding resistance \( R_s \) and inductance \( L_p \). When this current is forced through the secondary winding, the primary circuit behaves like a lossless inductor of value \( L_p \), with infinite Q factor at the frequency \( \omega \). This compensation technique is useful in narrowband applications with a fixed value of \( I_s \), or it can be used in wideband applications if the compensation current is made to vary as \( \frac{1}{\omega^2} \).

To illustrate the principle discussed, consider three different resonant circuits as shown in Fig. 4.4 below: A lossy resonant circuit, a perfect lossless circuit and a transformer compensated circuit.

The values shown are typical values for a monolithic inductor resonating at approximately 1 GHz. The input currents drawn from the signal source in each case...
are shown in Fig. 4.5.

\[ I_s = \gamma \frac{v_{in} R_s}{k \omega^2 L_p^2} \]  

(4.12)

where \( \gamma \) can be less than or greater than unity, and is ideally unity. In that case, the
impedance of the transformer compensated inductor can be shown to be:

\[ Z_{\text{comp}} = \frac{R_s(1 - \gamma) + j\omega L_p(1 + \frac{R_s^2 \gamma}{\omega^2 L_p^2})}{1 + \frac{R_s^2 \gamma}{\omega^2 L_p^2}} \quad (4.13) \]

When \( \gamma = 1 \), the compensated inductor is purely inductive, i.e., lossless.

In general the compensated circuit with incorrect compensating current can be likened to a new series connection of a resistor \( R_{S\text{comp}} \) and an inductor \( L_{P\text{compSeries}} \), where by inspection of the equation for \( Z_{\text{comp}} \), recognizing that \( \frac{\omega^2 L_p^2}{R_s^2} = Q^2 \), we see that:

\[ R_{S\text{comp}} = \frac{R_s(1 - \gamma)}{1 + \frac{\gamma^2}{Q^2}} \quad (4.14) \]
\[ L_{S\text{compSeries}} = \frac{L_p(1 + \frac{\gamma^2}{Q^2})}{1 + \frac{\gamma^2}{Q^2}} \quad (4.15) \]

Then for convenience, this series circuit can be represented by an equivalent parallel \( L_{P\text{compParallel}}/R_{P\text{comp}} \) circuit, where:

\[ R_{P\text{comp}} = R_{S\text{comp}}(1 + Q_{\text{comp}}^2) \quad (4.16) \]
\[ L_{P\text{compParallel}} = L_{P\text{compSeries}}(1 + \frac{1}{Q_{\text{comp}}^2}) \quad (4.17) \]
\[ Q_{\text{comp}} = \frac{\omega L_{P\text{compSeries}}}{R_{S\text{comp}}} \quad (4.18) \]

With some manipulation, it can be shown that the parallel loss resistance is:

\[ R_{P\text{comp}} = R_s \left[ \frac{(1 - \gamma)^2 + Q^2(1 + \frac{\gamma^2}{Q^2})^2}{(1 - \gamma)(1 + \frac{\gamma^2}{Q^2})} \right] \quad (4.19) \]
where \( Q = \frac{\omega L_S}{R_s} \), the uncompensated Q-factor of the original transformer primary coil.

The effects of the compensation are best seen by comparing the compensated \( R_{P_{\text{comp}}} \) with the uncompensated \( R_P = R_S(1 + Q^2) \). Taking the ratio gives:

\[
\frac{R_{P_{\text{comp}}}}{R_P} = \frac{(1 - \gamma)^2 + Q^2(1 + \frac{\gamma}{Q^2})^2}{(1 + Q^2)(1 - \gamma)(1 + \frac{\gamma^2}{Q^2})}
\] (4.20)

If \( Q^2 >> 1 \) this becomes

\[
\frac{R_{P_{\text{comp}}}}{R_P} = \frac{1}{1 - \gamma}
\] (4.21)

In this case, when \( \gamma = 1 \), \( R_{P_{\text{comp}}} = \infty \) as required. It can also be shown that the compensated parallel equivalent inductance is given by:

\[
L_{P_{\text{comp Parallel}}} = L_P \frac{(1 + \frac{\gamma}{Q^2})(1 + \frac{(1 - \gamma)^2}{Q^2(1 + \frac{\gamma}{Q^2})^2})}{1 + \frac{\gamma^2}{Q^2}}
\] (4.22)

Again, when \( \gamma = 1 \), \( L_{P_{\text{comp Parallel}}} = L_P \), i.e. the value of the inductance is not affected by the compensation. Perhaps the most important result is that the compensated Q-Factor of the primary coil is given by

\[
Q_{\text{comp}} = \frac{\omega L_{P_{\text{comp Series}}}}{R_{\text{comp}}} = \frac{Q}{(1 - \gamma)(1 + \frac{\gamma}{Q^2})}
\] (4.23)

If the original uncompensated coil \( Q^2 >> 1 \), this becomes:

\[
Q_{\text{comp}} = \frac{Q}{1 - \gamma}
\] (4.24)
This means that even with a 10% error in the compensating current, the compensated inductor has a Q factor 10 times that of the uncompensated circuit as shown in Fig. 4.6. It is also worth noting that Q can be made negative if $\gamma > 1$ which allows for other losses to be compensated if they appear in parallel with the transformer primary coil. A typical variation in compensated Q factor with $\gamma$ is shown in Fig. 4.7, for the case where the uncompensated Q factor is 8.

Figure 4.6: Lossy, lossless, and imperfectly ($\gamma = 0.9$) compensated resonant circuit currents

4.5 State of the art

An implementation of a transformer based compensation scheme consisting of coupled RF and drive coils was presented first in [19]. The circuit employs phase-shifting of the mutual components and demonstrates measured quality factors, Q, as high as a 2000. However, for obtaining such high performance the drive coil has to be driven
4.5 State of the art

Figure 4.7: Enhanced Q versus compensating current error factor, $\gamma$

off-chip with a rather complex circuit.

In [20] another transformer based compensation scheme was successfully employed in the design of a low noise amplifier with the boot-strapped inductor name. The drive circuit is shown in Fig. 4.8.

![Boot-strapped inductor circuit diagram](image)

Figure 4.8: Boot-strapped inductor

It was shown that:

$$Z_{in} = [R_1 + r_\pi - \omega M_g r_\pi \sin(\phi)] + j\omega[L_1 + M_g r_\pi \cos(\phi)] = R_{eff} + j\omega L_{eff} \quad (4.25)$$
where $R_1$ is the parasitic series resistance of $L_1$ and $\phi$ is the angle between $i_1$ and $i_2$. By changing the bias conditions of $Q_1$ and $Q_2$ the quality factor and the inductance seen in $Z_{in}$ can be changed. The circuit was implemented in a SiGe bipolar process and the attained Q was 30.

In [21] a CMOS compensation scheme was presented. This method employs a current mirror and uses both NMOS and PMOS transistors. The circuit is shown in Fig. 4.9, where $C_1$ is a large capacitor required for biasing.

![Figure 4.9: Mirror compensation scheme](image)

It can be shown that:

$$Z_{in} = [R_1 + r_x - \omega M m_0 \sin(\phi)] + j \omega [L_1 + M m_0 \cos(\phi)] = R_{eff} + j \omega L_{eff}$$

(4.26)

where $i_2 = i_1 m_0 e^{j\phi}$ and $M$ is the mutual coupling between the transformer windings. If the current ratio $i_2/i_1$ is properly selected, the real part of $Z_{in}$, $R_{eff}$, can be cancelled and the quality factor can be raised to theoretically infinite values.

In [22] a transformer based compensation scheme for $LC$ resonators was pre-
4.6 Novel Active Compensation Scheme

A new principle for a tunable transformer based compensation scheme which realizes the function of an enhanced high-Q LC tank is shown in Fig. 4.11 where the tunable resistor is a FET in triode.
Figure 4.11: Two Transistor Compensation Scheme

A detailed small signal model of the circuit implementation is shown in Fig. 4.12. The impedance $Z_{in}$ as indicated in Fig. 4.12 can be derived from the following equations:

$$I_{in} = I_p + sC_{gs}(V_{in} - V_s) + sV_{in}C_{res} \quad (4.28)$$

$$(V_{in} - V_s)(g_m + sC_{gs}) + (V_d - V_s)g_{ds} = \frac{V_s}{g_{dstune}} \quad (4.29)$$

$$I_s = g_m(V_{in} - V_s) + (V_d - V_s)g_{ds} - g_{mb}V_s \quad (4.30)$$

$$V_d + sMI_p + (R_s + sL_s)I_s = 0 \quad (4.31)$$
\[ V_{in} = sMI_s + (R_p + sL_p)I_p \] (4.32)

Due to its complexity the previous model is not suitable for synthesis and design of a Q-enhancement circuit. One should always keep in mind that to generate such a circuit the critical aspects relate to the initial sizing of the transistors and the transformer. To establish this starting point a simplified model is needed which gives the designer simple design equations. The effects of \( g_{ds} \) and \( g_{mb} \) may be considered negligible compared to \( g_m \) for a first order analysis. The simulator can perform detailed analysis afterwards.

Therefore a model with manageable complexity is shown in Fig. 4.13.

\[ i_s = v_s g_{dstune} = \frac{g_m v_{in}}{1 + g_m / g_{dstune}}. \] \( (4.33) \)

Summing currents at the \( v_{in} \) node gives

\[ i_{in} = v_{in} sC + \frac{(v_{in} - sM_i_s)}{R_s + sL_s}. \] \( (4.34) \)
From equation (4.34) the input impedance of the resonant tank is:

\[
\frac{v_{in}}{i_{in}} = Z_{in} = \frac{R_s + sL_s}{s^2L_sC_{res} + s(R_sC - G_mL_s) + 1}
\]  

(4.35)

where

\[
G_m = \frac{ki_s}{v_{in}} = \frac{kg_m}{1 + g_m/g_{d_{tune}}}
\]  

(4.36)

From equation (4.35) assuming \(R_s<<\omega L_s\) it can be shown that the compensated Q factor is approximately given by

\[
Q_{COMP} = \frac{1}{\omega_{res} R_s C_{res} \left(1 - \frac{G_m L_s}{R_s C}\right)}
\]  

(4.37)

where \(\omega_{res} = 1/\sqrt{L_s C_{res}}\). For infinite Q at \(\omega_{res}\)

\[
G_m = \frac{R_s}{(\omega_{res} L_s)^2} = \frac{R_s C_{res}}{L_s}
\]  

(4.38)

The two FETs in the circuit must be sized such that this last condition is met. Obviously dependency of \(g_{d_{tune}}\) is currently controlled by tuning the voltage on the FET in triode. The Frlan transformer must be sized such that its windings have high Q which reduces the required current swing in the secondary and, as a consequence, the total power consumption.
4.7 Electrical Simulations and Measurements

The circuit of Fig. 4.11 was implemented in a $0.18\mu m$ CMOS logic process with a low resistivity epitaxial substrate. A logic process was selected for the implementation because the passive inductors fabricated using this process would have a very low $Q$ in the range of 1 to 2, allowing the capabilities of the $Q$-enhancement method to be fully demonstrated. A die micrograph of the circuit is shown in Fig. 4.14. The transformer windings are designed to have an inductance of 4nH. The transformer primary is resonating with its loss capacitance and with the parasitics of the pad. The circuit draws $\approx 5mA$ of a $VDD = 1V$ supply for a 5mW total with $V_{tune} = 1.7V$ and $V_{bias}=1V$ when full compensation is achieved. According to the simulator results, the power consumption would be greatly reduced if the circuit was implemented on a low-loss non-epitaxial substrate.
Figure 4.15: Simulated vs measured S11 for various gate tuning voltages

The input reflection coefficient of the Q-enhanced parallel resonant tank was measured using an HP8510 Network Analyzer and a Cascade Microtech Wafer Prober. Fig. 4.15 shows the measured and simulated S11 traces for different values of the enhanced Q, corresponding to different gate voltages applied to the triode FET, M1. Fig. 4.16 shows the measured absolute values of the tank input impedance for different values of the enhanced Q, corresponding to different gate voltages applied to the triode FET, M1.

The simulated curves in Fig. 4.15 were generated using a full layout simulation of the passive components, including the pads, the transformer, and the interconnects in HP ADS Momentum, a 2.5D electromagnetic modeler. To accurately simulate the behaviour of the transformer and the pads, a full layout simulation was set up in HP ADS Momentum. The layout was basically migrated into the EM simulator. This can be seen by comparing Fig. 4.17 and Fig. 4.14. The structure to be simulated was also imported into a 3 dimensional EM simulator as shown in Fig. 4.18.
Figure 4.16: Measured $|Z_{in}|$ for various gate tuning voltages

Figure 4.17: Layout structure simulated in HP ADS Momentum

Figure 4.18: Layout structure simulated in ANSOFT HFSS
The discrepancy in the measured and the simulated results is possibly due to the lack of an accurate substrate model for the CMOS logic process that was used to fabricate the circuit and also due to the notorious prediction errors for $g_{dstune}$. However, the tunable Q-enhancement is clearly demonstrated, with Q approaching infinity for $V_{tune} \approx 1.7V$. 
Chapter 5

Stability Issues for Q-Enhancement Techniques

5.1 Background

Since the Q-enhancement techniques employ feedback mechanisms and gain stages built with active components they will be prone to unwanted oscillations. To avoid these unwanted oscillations it is important to understand in depth what are the conditions that generate oscillations and how can they be eliminated.

A basic feedback system which may become an oscillator is shown in Fig. 5.1. It is comprised of a gain stage described by the function \( A_v(j\omega) \) and a feedback network described by the function \( \beta(j\omega) \). The gain function is sometimes referred to as the open-loop gain since it is the gain between \( v_i \) and \( v_o \) when the path through \( \beta(j\omega) \) is open.

Negative feedback occurs when the feedback signal \( v_f \) subtracts from the input signal \( v_i \). If \( v_f \) adds to \( v_i \) the feedback is positive. In other words for positive feedback the total phase shift associated with the closed loop must be \( 0^\circ \) or a multiple of \( 360^\circ \).

![Figure 5.1: Basic feedback system](image)

60
By analyzing the system in Fig. 5.1 we can infer:

\[ A_v(j\omega) = \frac{v_o}{v_i} = \frac{A_v(j\omega)}{1 - \beta(j\omega)A_v(j\omega)} \]  \hspace{1cm} (5.1)

For stability all roots of the characteristic equation:

\[ 1 - \beta(j\omega)A_v(j\omega) = 0 \]  \hspace{1cm} (5.2)

must lie in the left half s-plane, where \( s = j\omega \).

The Nyquist stability criterion relates the function \( \beta(j\omega)A_v(j\omega) \) to the number of zeros and poles of \( 1 - \beta(j\omega)A_v(j\omega) \) that lie in the right-half s-plane. The analysis is based on root locus properties and the details of the criterion can be found in any control systems textbook [23].

To determine the root locus characterizing the transfer function is a fairly complex process and it is this complexity that led practicing engineers to look for shortcuts [12] in describing the stability of the system.

Such shortcuts are the gain and phase margin. Gain margin is a measure of how close to 1 is the magnitude of \( 1/\beta(j\omega)A_v(j\omega) \) when the angle of \( \beta(j\omega)A_v(j\omega) \) is 0°. Phase margin is a measure of how close to 0° is the angle of \( \beta(j\omega)A_v(j\omega) \) when the magnitude of \( \beta(j\omega)A_v(j\omega) \) is 1. Gain and phase margins thus describe the relative degree of stability of a system since, the larger the margins the further away the system will be from unstable behaviour. There are cases when these criteria may fail [12] and therefore they should be only regarded as a subset of the general
Nyquist test. To make things more difficult there are no universally recommended values for selecting a gain and phase margin that guarantees stability and meets the other system requirements such as overshoot. They depend on the system problem to be solved.

From control systems theory we know that oscillation occurs when a network has a pair of complex conjugate poles on the imaginary axis. If the closed loop gain has a pair of complex conjugate poles in the right-half plane, close to the imaginary axis, then, due to the ever-present noise voltage generated by thermal vibrations in the network (which can be represented by a superposition of input noise signals $v_i$), a growing sinusoidal output voltage appears. The characteristics of the sinusoidal signal are determined by the complex conjugate poles in the right half plane (as given by the inverse Laplace transform). As the amplitude of the noise-induced oscillation increases, the system adjusts its parameters (for example $g_m$ of the CMOS transistors) such that the complex poles change until they reach the imaginary axis. At this point the Barkhausen equation 5.2 is satisfied and the circuit oscillates.

For a microwave circuit [24] a feedback system can be constructed as shown in Fig. 5.2. The incident $a_n$ is some noise signal generated by the circuit and $\Gamma_{IN}(j\omega)$ and $\Gamma_L(j\omega)$ are the input and load reflection coefficients.

From the signal flow graph it can be inferred that:

$$a_L = \frac{a_n\Gamma_{IN}(j\omega)}{1 - \Gamma_{IN}(j\omega)\Gamma_L(j\omega)}$$ (5.3)

Equation 5.3 is similar to 5.1. From the previous discussion we may infer that the system is unstable when the function $1 - \Gamma_{IN}(j\omega)\Gamma_L(j\omega)$ has right-half plane
zeros. The Nyquist criterion can now be applied to analyze the poles in the right-half s-plane of the function \(1 - \Gamma_{IN}(j\omega)\Gamma_{L}(j\omega)\) to see whether the system is unstable or not. There are three possibilities based on the number of encirclements of the \(1 + j0\) point by the function \(\Gamma_{IN}(j\omega)\Gamma_{L}(j\omega)\):

1. There is no encirclement of the \(1 + j0\) point. This implies the system is stable if there are no poles of \(\Gamma_{IN}(j\omega)\Gamma_{L}(j\omega)\) in the right-half s-plane; otherwise the system is unstable.

2. There is a counterclockwise encirclement or encirclements of the \(1 + j0\) point. In this case the system is stable if the number of counter clockwise encirclements is the same as the number of poles \(\Gamma_{IN}(j\omega)\Gamma_{L}(j\omega)\) in the right-half s-plane; otherwise the system is unstable.

3. There is a clockwise encirclement or encirclements of \(1 + j0\). In this case the system is unstable.

This criteria is not applicable in the form stated if \(\Gamma_{IN}(j\omega)\Gamma_{L}(j\omega)\) has zeroes or poles on the \(j\omega\)-axis. In particular \(\Gamma_{L}(j\omega)\) or \(\Gamma_{IN}(j\omega)\) should not be zero at any frequency.

It follows that if \(|\Gamma_{IN}| < 1\) for all \(j\omega\) then \(\Gamma_{IN}(j\omega)\Gamma_{L}(j\omega)\) will not encircle the
1 + j0 point of the Γ-plane which is also the open point on the Smith chart for all passive loads |Γ_L| < 1 since |Γ_{IN}(jω)Γ_L(jω)| < 1. When |Γ_{IN}| < 1 the system is unconditionally stable independent of Γ_L.

If Γ_{IN} > 1 for a range of values of ω then an encirclement might or might not exist depending on Γ_L. Therefore the stability of the system is conditioned by Γ_L.

If Z_L(ω) = R_L(ω) + jX_L(ω) is an open circuit then Γ_L = 1 and the system is stable if Γ_{IN}(jω) encircles the open circuit point on the Smith chart, i.e. the 1 + j0 point of the Γ-plane.

If Z_L(ω) = R_L(ω) + jX_L(ω) is a short circuit then Γ_L = -1 and the system is stable if -Γ_{IN}(jω) encircles the open circuit point on the Smith chart i.e. the 1 + j0 point of the Γ-plane.

The input impedance of the active circuit Z_{IN} is, in general, a function of the voltage (or current) amplitude and frequency.

\[ Z_{IN}(A, ω) = R_{IN}(A, ω) + jX_{IN}(A, ω) \]  \hspace{1cm} (5.4)

where A is the amplitude of the oscillation.

Recall:

\[ Γ_{IN}(A, ω) = \frac{Z_{IN}(A, ω) - Z_0}{Z_{IN}(A, ω) + Z_0} \]  \hspace{1cm} (5.5)

\[ Γ_L(ω) = \frac{Z_L(ω) - Z_0}{Z_L(ω) + Z_0} \]  \hspace{1cm} (5.6)

\[ 1 - Γ_L(ω)Γ_{IN}(A, ω) = \frac{2Z_0(Z_L(ω) + Z_{IN}(A, ω))}{(Z_{IN}(A, ω) + Z_0)(Z_L(ω) - Z_0)} \]  \hspace{1cm} (5.7)

Equation 5.7 reveals that a necessary condition for oscillation is that Z_L(ω) +
$Z_{IN}(\omega) = 0$.

The oscillations will continue to build up as long as this condition is satisfied. The amplitude must eventually reach a steady state value which occurs when the loop resistance is 0. This amplitude dependency shows the need to employ large signal s-parameters for the characterization of the active devices. To ensure that the frequency of oscillation determined by the previous equations is stable and a steady state frequency of oscillation is actually reached other conditions need to be added [24].

### 5.2 Q-enhancement stability

This section will refer the previous discussion to the particular case shown in Fig. 5.3. The additional question to be answered is what is the maximum Q attainable while still ensuring stability.
The impedance $Z_{in}$ shown in Fig. 5.3 can be derived from the following equations.

\[ I_{in} = I_p + sC_{gs}(V_{in} - V_s) + sV_{in}C_{res} \]  
\[ (V_{in} - V_s)(g_m + sC_{gs}) + (V_d - V_s)g_{ds} = \frac{V_s}{Z_C} \]  
\[ I_s - \frac{V_d}{Z_s} = g_m(V_{in} - V_s) + (V_d - V_s)g_{ds} - g_{mb}V_s \]  
\[ V_d + sMI_p + (R_s + sL_s)I_s = 0 \]  
\[ V_{in} = sMI_s + (R_p + sL_p)I_p \]

If $C_{gs} = 0, g_{ds} = 0$, $Z_{in}$ is:

\[ Z_{IN} = \frac{(s^2(L_x * L_p - M^2) + s(L_xR_p + L_pZ_s) + R_p(R_s + Z_s))(g_mZ_c + 1)}{A + Bs^2 + Cs + D} \]  
\[ A = (-M^2 + L_xL_p)C_{res}(g_mZ_c + 1) \]  
\[ B = (L_xL_pC_{res} + L_pC_{res}Z_s + L_pC_{res}R_s)(g_mZ_c + 1) \]  
\[ C = (g_mZ_c + 1)(L_x + Z_sR_pC_{res} + R_sR_pC_{res}) - g_mZ_sM \]  
\[ D = Z_s(g_mZ_c + 1) + R_s(g_mZ_c + 1) \]

A sufficient condition for stability is that $\Gamma_{IN}(j\omega)\Gamma_L(j\omega)$ does not encircle the $1 + j0$ point.

A strong condition for stability is $|\Gamma_{IN}(j\omega)| < 1$.

These cumbersome mathematical formulas have limited practical value since the simplified mathematical model of the transistors as well as the transformer model employed to generate the previous equations are merely first order estimates of the behaviour at GHz frequencies. The simulator can verify whether or not the stability
conditions are met but even advanced simulations are ultimately limited by the accuracy of the models.

If the simplified circuit model in Fig. 4.13 is used the poles of the transfer function for $Z_{in}$ (equation (4.35)) are given by:

$$s = \frac{G_m}{C_{res}} - \frac{R_s}{L_s} \pm \sqrt{\left(\frac{G_m}{C_{res}} - \frac{R_s}{L_s}\right)^2 - \frac{4}{L_s C_{res}}}.$$  \hspace{1cm} (5.18)

The proposed Q-enhanced LC tank will be unstable if these poles lie in the right half plane. The circuit will be unstable if $Re(Z_{in}) < 0$ at $\omega_{res}$ where

$$Re(Z_{in}) = \frac{R_s - \omega^2 L_s^2 G_m}{(1 - \omega^2 L_s C_{res})^2 + \omega^2 (R_s C_{res} - G_m L_s)^2}.$$  \hspace{1cm} (5.19)

The stability condition can be written as:

$$G_m \leq \frac{R_s C_{res}}{L_s}.$$  \hspace{1cm} (5.20)

The above condition assumes linear behavior of the feedback circuit. Several nonlinear effects may occur in practice. If the enhanced Q is sufficiently high, $|S11|$ can be less than 1 at $\omega_{res}$ but greater than 1 for some frequency greater than $\omega_{res}$ because the compensating voltage in the primary is proportional to $\omega^2$. In this case the circuit may oscillate due to nonlinear effects even though the linear stability condition is satisfied.

Nonlinear effects occur because of the variation of $g_{ds}$ and $g_m$ at large signal swings. These variations cause $G_m$ to vary with the voltage across the tank, and can cause oscillation if a large signal is applied. We have found that this nonlinear effect
Figure 5.4: Measured input reflection coefficient $\Gamma_{IN}$ for various tuning voltages may be mitigated by modestly increasing the loss resistance of the secondary coil, without sacrificing Q tunability and enhancement.

To obtain a maximized quality factor from the unloaded Q-enhanced LC tank shown in Fig. 5.3 one has to require $Z_{IN}$ to follow the characteristic of an ideal LC tank with $R_{IN} = \infty$ when $X_{IN} = 0$. In other words $\Gamma_{IN}(j\omega)$ has to be brought close to $1 + j0$ while still keeping the circuit stable. As shown in figure 5.4 variations in the tuning voltage can render the circuit unstable.

Thus to obtain a maximized quality factor one must bring the Q-enhancement circuit right on the verge of instability. This trade-off is a drawback of all known Q-enhancement circuits. To create a high Q-impedance on the edge of the Smith chart is the objective of this work. To ensure that this circuit is stable under all circumstances is a challenge that requires future work. Even if measured data is available for $Z_{IN}$, as it is in our case, process variations may cause differences from
chip to chip. A feedback mechanism needs to be developed to prevent the circuit from becoming an unwanted oscillator.

Note that the circuit described in [21] which emulates a compensated inductor rather than a compensated LC tank does not seem to respect the stability criteria and the equations presented indicate that unless a stabilizing circuit or load is added the circuit is essentially an oscillator. To prove this one should observe that the current in the secondary necessary to cancel the losses in the primary at a given frequency is inversely proportional to the square of the frequency. Therefore, the current selected to cancel the losses at the frequency where the circuit is supposed to operate as a perfect inductor will be higher than the current needed to compensate the losses at the self resonant frequency and therefore the circuit will be oscillating unless the circuit is somehow stabilized.

The circuit described in [22] does not seem to suffer any stability problem since there is no dependence on the frequency for cancelling the losses. It is likely the circuit presented in [20] may suffer some stability problems as well.

Since the details of the RF behaviour of the passives in the references mentioned are not available any definite statements about the stability are best avoided.

### 5.3 Unconditional Stability

By referring to Fig. 5.4 or Fig. 5.5 it can be seen that there are passive loads $Z_L$ for which the circuit becomes unstable even if the unloaded Q-enhanced circuit $Z_L = \infty$ is stable. Thus to make the circuit stable for all passive loads we must ensure that $Z_{IN}$ is a passive impedance and $\Gamma_{IN}$ stays inside the Smith chart for all frequencies.
There are at least two methods to achieve this goal: The first method is to add a capacitor in the secondary as shown in Fig. 5.6. The input reflection coefficient of such a circuit is shown in Fig. 5.7 and the enhanced quality factor is shown in Fig. 5.8. Simulated unconditionally stable Q’s as high as 750 were obtained using this scheme.

To understand the principle behind this mechanism of stabilizing the circuit one should remember that the current in the secondary necessary to cancel the losses in the primary at a given frequency is inversely proportional to the square of the frequency. Therefore, the current in the secondary selected to cancel the losses at the resonant frequency may be more than the required current to cancel the losses at a higher frequency and thus $Z_{IN}$ may exhibit a negative resistance, which in turn may create an unstable circuit for certain loads. The role of the capacitor is to leak some of the compensating current so that the current through the secondary is

---

**Figure 5.5:** Input reflection coefficient $\Gamma_{IN}$ without any stabilization circuitry
5.3 Unconditional Stability

Figure 5.6: Unconditional stability with capacitor loading the secondary diminished at higher frequencies and the instability conditions are avoided.

For the capacitor stabilized circuit it can be shown that:

\[
\begin{align*}
Z_{in} &= \frac{A + jB}{M + jN} \\
A &= R_s(1 - \frac{2\omega^2}{\omega_{res}^2}) \\
B &= \omega(1 + \omega_{res}^2 C_{stab}^2 R_s^2 - \frac{\omega^2}{\omega_{res}(1 - k^2)}) \\
M &= (1 - \frac{\omega^2}{\omega_{res}^2}(1 + \frac{C_{res}}{C_{stab}}) - \omega^2 C_{res} C_{stab} R_s^2 + \frac{\omega^4}{\omega_{res}^4} C_{res} C_{stab} (1 - k^2)) \\
N &= \omega((C_{stab} + C_{res})R_s - \frac{2C_{res} R_s \omega^2}{\omega_{res}^2} - \frac{g_m L_s k^2}{1 + g_m R_C}).
\end{align*}
\]

If the enhanced Q is high then a good approximation of the resulting resonant frequency of the primary is

\[
f_{res} \approx \frac{1}{2\pi \sqrt{L_s (C_{res} + C_{stab}) + C_{res} C_{stab} R_s^2}}.
\]

A second method to create an unconditionally stable circuit is to add a low-Q
5.3 Unconditional Stability

Figure 5.7: Input reflection coefficient $\Gamma_{IN}$ for a capacitor stabilized circuit

Figure 5.8: Input impedance and Q factor for a capacitor stabilized circuit
Figure 5.9: Unconditional stability with an LC tank in the source of the tuned FET resonant tank in the source of the tuned FET as shown in Fig. 5.9. The input reflection coefficient of such a circuit is shown in Fig. 5.10 and the enhanced quality factor is shown in Fig. 5.11. Simulated unconditionally stable Q’s above 200 were also obtained using this scheme.

Once again the principle behind this mechanism of stabilizing the circuit is to reduce the current in the secondary at a given high frequency. The resistance offered by the tuned FET increases dramatically at the resonant frequency of the stabilizing LC tank, the secondary current is reduced and thus $Z_{IN}$ will no longer exhibit a negative resistance which creates a potentially unstable system.

The advantage of this last scheme is that it does not affect the self resonant frequency of the Q-enhanced LC tank. However it is more complex and requires precisely designed values for $L_{stab}$ and $C_{stab}$. 
Figure 5.10: Input reflection coefficient $\Gamma_{IN}$ for an LC stabilized circuit

Figure 5.11: Input impedance and Q factor for an LC stabilized circuit
Chapter 6

Noise and Linearity

6.1 Noise Analysis Background

It was mentioned in the introductory chapters that addition of active parts to compensate losses in the passive components adds noise and limits the linearity of the circuits. The purpose of the analysis that follows, is to quantify these drawbacks for the proposed Q-enhancement scheme.

There is a wealth of publications that have studied in detail various noise mechanisms. However, to the circuit designer the relevant aspects are usually described using simple circuit models that characterize the noise sources quantitatively. It is important to define the noise models that characterize the elements used in the Q-enhancement circuit.

For a resistor the noise model is shown in Fig. 6.1:

\[
\begin{align*}
\overline{e_n^2} &= 4kT R \Delta f 
\end{align*}
\]  

Figure 6.1: Resistor thermal noise model

where

\[
\overline{e_n^2} = 4kT R \Delta f
\]  

(6.1)
6.1 Noise Analysis Background

\[
\overline{i_n^2} = \frac{v_n^2}{R} = \frac{4kT \Delta f}{R} = 4kTG \Delta f. \tag{6.2}
\]

The noise model for a bipolar transistor is shown in Fig. 6.2:

![Bipolar transistor noise model](image)

Figure 6.2: Bipolar transistor noise model

where

\[
\overline{e_b^2} = 4kTr_b \Delta f \tag{6.3}
\]

\[
\overline{i_{nb}^2} = 2qI_B \Delta f + \frac{K_1}{f} \Delta f \tag{6.4}
\]

\[
\overline{i_{nc}^2} = 2qI_C \Delta f. \tag{6.5}
\]

For a MOS transistor the noise model is shown in Fig. 6.3:

![MOS noise model](image)

Figure 6.3: MOS noise model

where

\[
\overline{i_{nd}^2} = \gamma 4kTg_{d0} \Delta f + \frac{K_1}{f} \Delta f \tag{6.6}
\]
\[ \bar{v}^2_{ng} = 4kT\delta r_g \Delta f \]  
(6.7)

\[ r_g = \frac{1}{5g_{d0}}. \]  
(6.8)

where \( \gamma \) and \( \delta \) are chosen empirically to match the observed noise behavior of a given fabrication process. In our analysis the 1/f noise was ignored, \( K_1=0 \), since at the high frequency of operation this noise source is not significant. To simplify the analysis the gate noise \( \bar{v}^2_{ng} \) was also ignored. The agreement between simulations and measurements tends to suggest that this noise source is not dominant. An exact expression for \( \gamma \) for long channels is [25]

\[ \gamma = \frac{1 - v + (v^2/3)}{1 - v/2} \]  
(6.9)

where \( v = V_d/V_{dsat} \) and \( \gamma = 2/3 \) for \( V_{ds} > V_{dsat} \). Quite often circuit simulators replace \( g_{d0} \) with \( g_m \), which is strictly valid only for long channel devices. Nicollini [26] has shown that the following expression agrees closely with measurements on long channel devices, and is in common use for level 1 FET models in circuit simulators:

\[ \frac{1}{\sqrt{\Delta f}} = \sqrt{\gamma 4kT(g_m + g_{mb} + g_{ds})} \]  
(6.10)

where \( \gamma = 1 - V_{ds}/(3V_{dsat}) \) for \( V_{ds} < V_{dsat} \) and \( \gamma = 2/3 \) for \( V_{ds} > V_{dsat} \). In order to facilitate comparison of theory with simulation, and to gain a physical understanding of the dominant noise sources and their functional dependence on circuit parameters, the Nicollini model is used.
6.2 Noise Analysis of the Q-enhancement Scheme

To perform predictions on the noise behaviour of the Q-enhancement circuit the sophisticated EM model can no longer be used. The available tools can not perform a noise analysis (periodic steady state) with an S-parameter block. Therefore it is necessary to fit the EM model of the passive elements in the layout with a lumped element model as shown in Fig. 6.4. The simulator may be able to cope with a sophisticated lumped element model fit but to obtain an analytical description of the circuit a simple model is required.

![Equivalent lumped element model for the EM model](image)

Figure 6.4: Equivalent lumped element model for the EM model

To show how crude this approximation is the s-parameters obtained from the models are compared in Fig. 6.5. An improved model is obtained if the 1pF capacitor is considered lossy with a 45Ω resistor connected in series to account for some of the substrate losses in the epitaxial substrate of both the pads and the transformer as shown in Fig. 6.6. An even better model is obtained if the distributed loss capacitance in the secondary is taken into account as a lumped element. However, considering these effects complicates the analysis significantly. Therefore the simplified model of Fig. 6.4 is used.
There are several other important inaccuracies that should be considered. In reality the effective series loss resistance in the windings of the transformers is only \( \approx 10\Omega \), the extra resistance being needed to account for the losses in the epitaxial substrate and for the fact that these losses are distributed across the length of the transformer windings and not only in series with the windings, a fact which deteriorates the precision of the analysis. The simplified model which does not consider the secondary loss capacitance creates a number of illusions. For example at very high frequencies the compensating current required to compensate the losses in the primary winding of an on-chip transformer described in Eq. 4.10 is approaching zero. A second consequence is that the secondary loss resistance does not contribute to the noise performance of the circuit. However, this not exactly true due to the presence of the secondary loss capacitance. For a first order approximation we choose to ignore these effects.

![Figure 6.5: S-Parameters comparison with a lossless 1pF capacitor](image)

To clarify the use of various indices the schematic shown in Fig. 6.7 was used for
Figure 6.6: S-Parameters comparison with the 45Ω resistor in series with the capacitor

Figure 6.7: Q-Enhancement schematic for noise analysis

noise analysis. All the small signal elements pertaining to transistor M1 are indexed 1 and all the small signal elements pertaining to the transistor M2 are indexed 2.

The noise voltage that appears at the input terminals of the tank across an arbitrary source resistance $R_{src}$ is of interest. Using superposition we analyze the contribution to this equivalent input referred noise voltage from each noise source in the circuit. The three main noise sources are the thermal noise of $R_s$ in the primary, and the thermal drain current noises of M1 and M2, taking the internal feedback
6.2 Noise Analysis of the Q-enhancement Scheme

Figure 6.8: Equivalent circuit for calculating input referred noise contribution of (a) $R_s$, (b) M1, and (c) M2

into account. For the case where there is no additional stabilization circuitry, we can neglect the thermal noise contributions from $R_s$ in the secondary. Once again, we neglect $g_{ds2}$ and $g_{mb2}$ for simplicity.

The contribution of the thermal noise of $R_s$ may be analyzed using the circuit of Fig. 6.8 (a). The contributions of the thermal drain noise currents of M1 and M2 may be analyzed by examining Fig. 6.8 (b) and (c) respectively, where the induced voltage in the secondary has been omitted because in the simplified lumped model used it is in series with a current source in each case, and has no effect on the output noise. In reality because of the distributed losses to the substrate it does have an
6.2 Noise Analysis of the Q-enhancement Scheme

effect.

The noise contributions of $R_s$, M1, and M2 are shown in Table 6.1,

<table>
<thead>
<tr>
<th>Component</th>
<th>Thermal noise generated</th>
<th>Contribution to $\bar{v}_{in}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_s$</td>
<td>$\frac{\bar{e}_n}{\sqrt{\Delta f}} = \sqrt{4kTR_s}$</td>
<td>$\frac{\bar{e}_n}{\sqrt{\Delta f}}$</td>
</tr>
<tr>
<td>M1</td>
<td>$\frac{i_{d1}}{\sqrt{\Delta f}} = \sqrt{\gamma 4kT(g_{m1} + g_{ds1})}$</td>
<td>$\frac{i_{d1}}{\sqrt{\Delta f}}$</td>
</tr>
<tr>
<td>M2</td>
<td>$\frac{i_{d2}}{\sqrt{\Delta f}} = \sqrt{\gamma 4kT g_{m2}}$</td>
<td>$\frac{i_{d2}}{\sqrt{\Delta f}}$</td>
</tr>
</tbody>
</table>

Table 6.1: Noise Contributions of $R_s$, M1, and M2, to the input referred noise, $v_{in}$

where

$$D = s^2 + s \left( \frac{1}{CR_{src}} + \frac{R_s}{L_s} - \frac{G_m}{C} \right) + \frac{R_s + R_{src}}{L_s CR_{src}}. \quad (6.11)$$

$$G_m = \frac{k_i2}{v_{in}} = \frac{k g_{m2}}{1 + g_{m2}/g_{ds1}}. \quad (6.12)$$

The calculated noise contributions are plotted in Fig. 6.9 for the case where $R_{src} = \infty$ and a given biased condition was chosen. These results agree exactly with simulated results using a simple lumped element transformer model and Level 1 FET models. It can be seen that the main contributor to the total input referred noise is the triode FET, M1.

The maximum noise is of interest when considering the use of the actively compensated inductance in a circuit application. The worst-case noise voltage across the tank will occur when $R_{src} = \infty$. Using the equations in Table 6.1, the peak noise due to M1, M2, and $R_s$ can be written in terms of the compensated Q factor, $Q_{COMP}$ as

$$\frac{\bar{v}_{in}}{\sqrt{\Delta f}} = K \sqrt{\frac{i_{d1}^2}{\Delta f} \cdot \frac{1}{g_{ds1}} + \frac{i_{d2}^2}{\Delta f} \cdot \frac{1}{g_{m2}} + \frac{e_n^2}{\Delta f} \cdot \frac{C}{L_s G_m^2}} \quad (6.13)$$
where $K$ is a dimensionless constant given by:

$$K = G_m Q_{COMP} \sqrt{\frac{L_s}{C}}$$  \hspace{1cm} (6.14)

and $Q_{COMP}$

$$Q_{COMP} = \frac{1}{\omega_{res} R_s C \left(1 - \frac{G_m L_s}{R_s C}\right)}.$$  \hspace{1cm} (6.15)

The terms inside the square root of equation (6.13) represent the peak noise contributions of $M_1$, $M_2$, and $R_s$ as shown in Fig. 6.9.

It was previously shown that the Q-enhancement circuit may become unstable due to the frequency dependence of the positive feedback and two possible methods of stabilizing it were proposed: resonating the transformer secondary with a capacitor and degenerating the source of $M_1$ with a resonant tank. Resonating the secondary with a capacitor results in a total input referred noise similar to the case with no stabilization. When the secondary capacitance is present, the secondary loss resistance clearly contributes to the input referred noise even without considering the losses to the substrate. However, to maintain the same resonant frequency, the primary capacitance should be reduced. The net result is that the overall input referred noise does not change appreciably from the case when the secondary capacitor is not present.

The simulated noise contributions of $R_{s1}$, $R_{s2}$, $M_1$, and $M_2$ to the input referred noise voltage for the circuit with a resonated secondary with $R_{src} = \infty$ and a given bias condition are shown in Fig. 6.10.

For a passive LC tank where the inductor has a series loss $R$ the peak output
6.2 Noise Analysis of the Q-enhancement Scheme

Figure 6.9: Simulated input referred noise contributions for $R_s$, M1, and M2

Figure 6.10: Simulated input referred noise contributions for $R_{s1}$, $R_{s2}$, M1, and M2 with resonated transformer secondary
noise is obtained at resonance and it is:

\[ e_{nRLCpeak} = Q \cdot \sqrt{4kT} \]  \hspace{1cm} (6.16)

where \( Q = 1/R \cdot \sqrt{L/C} \). The noise bandwidth for the passive LC tank in Hz is \( B = f_{\text{res}}/Q \) where \( f_{\text{res}} \) is the resonant frequency of the tank.

Recall that:

\[
\frac{\tilde{v}_{in}}{\sqrt{\Delta f}} = K \sqrt{\frac{i_{d1}^2}{\Delta f} \cdot \frac{1}{g_{ds1}} + \frac{i_{d2}^2}{\Delta f} \cdot \frac{1}{g_{m2}} + \frac{e_{n}^2}{\Delta f} \cdot \frac{C}{L_s G_m^2}} \approx Q_{COMP} G_m \sqrt{\frac{L}{C}} \sqrt{\frac{i_{d1}^2}{g_{ds1}}} \]  \hspace{1cm} (6.17)

If we assume

\[
\frac{i_{d1}}{\sqrt{\Delta f}} = \sqrt{\gamma/4kT g_{ds1}} \]  \hspace{1cm} (6.18)

where \( g_{ds1} = \mu C_{ox} \frac{W}{L} (V_{GS} - V_T - V_{DS}) \) then the noise of the active circuit is:

\[
\frac{\tilde{v}_{in}}{\sqrt{\Delta f}} = Q_{COMP} G_m \sqrt{\frac{L}{C}} \sqrt{\frac{4kT \gamma}{\mu C_{ox} \frac{W}{L} (V_{GS} - V_T)}} \]  \hspace{1cm} (6.19)

where \( V_{DS} \) was assumed small.

It follows that the compensated circuit noise is higher than that of the passive circuit for a given quality factor. The conclusion is that, if the passive circuit could attain the Q’s of the compensated circuit, it would be superior in noise performance. Unfortunately this is not the case.

The second proposed stabilization technique based on placing a resonant tank in the source of M1 does not change the input referred noise significantly near resonance because the impedance of the stabilizing tank is low near the resonant frequency of
Figure 6.11: Q-Enhancement Circuit with tuning transistor M1 eliminated the primary tank.

The analytical formulas presented above have primarily a qualitative value. Due to the complicated model of the transistor models at RF and the intricacies of the model required for the passive elements it is unwise to expect good agreement between measurements and the analytical formulas presented. The formulas are meant to give the designer an insight into locating the noise sources and finding ways to minimize their effect.

Due to the fact that M1 is the most significant noise source a designer might choose to eliminate it at the cost of losing flexibility on biasing of M2. An alternative implementation of the circuit which excludes M1 is shown in Fig. 6.11.

6.3 Noise Measurement

The measurement of the input referred voltage noise of the parallel resonant tank with a Q-enhanced inductor posed a problem because of the 50Ω measurement environment. Loading the high impedance Q-enhanced tank with 50Ω degrades the Q and attenuates the input referred noise to a level where it is difficult to make a meaningful measurement. An effort was made to address this problem by placing
an external common emitter buffer amplifier with high input impedance and 50Ω between the tank and the spectrum analyzer used to measure the noise as shown in Fig. 6.14.

![Noise Measurement Test Setup Diagram](image)

Figure 6.12: Noise measurement test setup

To extract the noise in $V/\sqrt{\text{Hz}}$ the following steps were taken.

1. The excess noise ratio (ENR) over -174dBm/Hz was measured on the Agilent E4440 spectrum analyzer.

2. The pre-amp had 40dB gain and 2 dB NF, thus $\text{ENR'} = \text{ENR} - 42\text{dB}$, where $\text{ENR'}$ is the ENR at the pre-amp input

3. The noise at the input of the pre-amp is $(\text{ENR'} - 174\text{dBm/Hz})$

4. Noise power at the pre-amp input in dBm/Hz is $10\log((V^2/\text{Hz})/(50\Omega \times 0.001\text{W}))$

5. The noise in $V/\sqrt{\text{Hz}}$ was then determined from step 4.

The buffer amplifier was implemented with a discrete bipolar transistor with an intrinsic input impedance in the $k\Omega$ range. A significant degradation in the tank Q
was still incurred using the bipolar buffer mainly due to the package parasitics. It was predicted in the simulator that the loaded enhanced Q will be less than 5 for tuning voltages less than 2.7V as shown in Fig. 6.13.

![Simulated impedance of the loaded Q-enhancement circuit](image)

Figure 6.13: Simulated impedance of the loaded Q-enhancement circuit

The loaded enhanced Q was still greater than the unloaded un-enhanced Q and the input noise was measurable.

Fig. 6.14 shows the measured input referred noise of the Q-enhancement circuit for five different values of Q. The simulated input referred noise was within 50% of the measured value. From equation 6.13 it may be estimated that the noise scales with loaded enhanced Q. Thus it may be inferred that for a Q of 150 the noise would be 50 times greater than when the Q is 3. The noise contribution of the bipolar transistor is small and may be evaluated using the model in Fig. 6.2. Unfortunately the package parasitics change the simplified model significantly. The gain and noise contribution of the bipolar transistor can be determined in the simulator or with a special 50 Ω test fixture.
Figure 6.14: Measured input referred noise vs frequency at output of npn buffer for various loaded Q’s (results shown for loaded $Q = 3.2, 2.8, 2.1$)

6.4 Linearity Analysis

To analyze the linearity of the Q enhancement circuit a performance index is needed. Note that the Q enhancement circuit is a 1-port device. It was attempted to develop a linearity performance index similar to the IP3 of a two port device.

The Q-enhancement circuit may be considered as a voltage input, current output device. Thus to estimate the linearity we will analyze the spectral content of the current waveform when the amplitude of the input voltage is increased. This is analogous to an amplifier where the spectral content of the output is analyzed as the input power is increased.

Again the lumped model had to be used and simplified LEVEL 1 models were used for the transistors to facilitate simulations. Transient time-domain simulations were performed and a discrete Fourier transform (DFT) was performed on the current waveform. The powers in the fundamental and in the second and third harmonics
6.4 Linearity Analysis

were recorded and plotted against the sweeping voltage as shown in Fig. 6.15.

Note that the limited dynamic range that the Q-enhancement circuit supports can be derived from a theoretical argument. The secondary winding of the transformer has to be driven with high currents. For a realistic case where \( L = 2 \text{nH} \), \( k = 0.75 \) and \( R_s = 7.5 \ \Omega \) and the compensating circuit is operating at 1.8GHz, the amplitude of the compensating current for a 100mV input is 2mA, according to Eq. 4.10. This compensating current requires high bias currents and clearly imposes a severe limit on the linearity. The linearity may be improved if the quality of the transformer windings is good along with a good coupling factor.

Figure 6.15: Linearity behaviour of the Q-enhancement circuit
Chapter 7

Conclusion and Future Developments

This work presented several techniques for enhancing the quality of on-chip spiral inductors. First some passive methods were presented together with predictability and optimization issues. Then active methods were introduced. After a short critique of active inductors and a presentation of the state of the art in transformer based Q-enhancement techniques, a new transformer based Q-enhancement technique was introduced and proven to be functional.

As a natural consequence of using active components the Q-enhancement stability, noise and linearity were limitations that needed to be addressed. Equations or methods to analyze, quantify and qualify these aspects have been provided.

Further work is needed to define and improve the stability, noise and linearity properties of the circuit. A potential voltage controlled oscillator (VCO) that employs this scheme is shown in Fig. 7.1. This VCO recycles the power required in the buffers to compensate the Q of the resonant tank for the core transistors and therefore the core power may be reduced, yielding a low power consumption. The circuit has been built and proven to be a tunable oscillator. However, properties such as phase noise and load pull are still under scrutiny.

Soorapanth and Wong [22] have demonstrated the application of a Q-enhanced series resonant circuit to the realization of a bandpass filter structure, requiring an array of RF chokes to provide DC bias to the circuit. The circuit described in this work can be employed in the design of a monolithic coupled resonator bandpass
Figure 7.1: VCO employing the compensation scheme

Figure 7.2: Proposed application of the Q-enhancement technique to a coupled resonator bandpass filter

filter of the type shown in Fig. 7.2. No RF chokes are required to bias the Q-enhancement circuits in this implementation. The realization of filters of this type is being investigated as well as the use of this scheme in LNAs, and other RF building blocks.
Bibliography


1995.


