CHAPTER 1 Introduction

1.1 Motivation

The coming of Information Technology age is characterized by a series of high data rate transaction services such as World Wide Web browsing, multimedia transmission and personal communication services. The advance of IC technology not only makes these kinds of services more available than before, but also more portable due to the decreasing size of the wireless terminals. Since the power source occupies a large part of the portable system. Continuous shrinkage of the system will become impossible without reducing battery size. However, by looking back at the battery development in the past twenty years, the decreasing of battery size with the same power delivery capacity is apparently slow. Therefore, the viable way to break the size bottleneck is to increase the wireless system power efficiency.

On the other hand, high demand for wideband services within a limited frequency band puts further constraint in the frequency spectrum. Therefore wideband linear modulation techniques such as multicarrier modulation (MCM) become more attractive than ever before. OFDM (Orthogonal Frequency Division Multiplexing) is one of the MCM signals. Due to its high bandwidth efficiency and high data rate transmission capacity, OFDM
becomes the most probable modulation technique beyond third generation wireless system.

While OFDM scheme has very good spectral efficiency, its envelope fluctuates strongly. Applying power-efficiency non-linear power amplifier on such kind of signal leads to out-band radiation and server adjacent channel interference. To reduce distortion, linear power amplifiers such as Class A or Class AB power amplifiers are needed. However the linear power amplifiers are intuitively power inefficient and inhibit the reduction of the wireless system size. To tackle this problem, some linearization techniques applied on high efficient PAs are considered here.

1.2 Research Goal

This research project focuses on the design of a linearized power amplifier which can also maintain a high power efficiency for wideband modulation signal -- OFDM. Different linearization techniques are compared and the Envelope Elimination and Restoration (EER) technique is finally chosen for OFDM signal amplification. System simulation is done to find out the design guidelines of EER power amplifier. Finally, a wideband DC-DC power converter is designed using BiCMOS process to linearize a commercial RF power amplifier.

1.3 Thesis Outline

This thesis consists of seven chapters. Chapter 2 gives introduction of OFDM signal and system. Also, the power loss in an ideal power amplifier is reviewed. Different power
amplifier linearization techniques are analysed and compared in chapter 3. Chapter 4 describes the system simulation of an OFDM radio system with EER power amplifier and the required parameters of the EER power amplifier are found through the simulation. Chapter 5 considers the design of a wideband DC-DC power converter for the linearized power amplifier. Chapter 6 shows the measurement results and the implementation of EER PA. The final chapter is about the future works to improve the linearity and power efficiency of EER PA.
2.1 Introduction

Previously, the relative bandwidth inefficiency modulation techniques, such as MSK, GMSK and TFM, were used in mobile communications. The reason of their popularity is due to their constant envelope property which is appropriate for using non-linear power-efficiency amplifier. However, to accommodate more and more users in limited channel space, linear modulation techniques, such as QAM (Quadratic Amplitude Modulation), is more attractive. But, since these modulation signals present nonlinear envelope, it is necessary to use linear power amplifiers which are less efficient than conventional Class-C power amplifiers or switch mode power amplifiers.

Although QAM is spectrum efficient, single carrier QAM signal is not suitable for very high speed transmission due to the multipath delay effects. To transceive high data rate information, a growing interest is shown by researchers and product developers in using MCM (Multi-carrier Modulation) signals which have higher resistance to multipath delay effects than conventional single carrier modulation signals. However, the envelope of MCM signal is non-constant even when its subchannels are modulated with constant envelope modulation techniques. Also, when the bandwidth of multicarrier signal increases by
adding more subcarriers, the envelope spreads wider and the power efficiency of a linear power amplifier decreases. Therefore, in order to achieve both high bandwidth and power efficiency, some clever linearization techniques should be used and a brief introduction to these techniques is given in later section.

2.2 Linear Power Amplifier

To linearly amplify a signal, power amplifiers such as Class-A and Class-AB power amplifiers should be properly biased to avoid distortion. For an ideal power amplifier ("Ideal" here means no parasitic power loss.), there are two reasons which cause power loss. They are: 1) biasing current power loss; 2) power loss due to envelope variation. The following subsections discuss the two types of power loss.

2.2.1. Biasing Power Loss:

Consider a Class A power amplifier shown in Fig. 2.1, the gate voltage should be biased such that the biasing current is equal to half of the maximum output current to avoid clipping. Assume a maximum signal is applied in the input, Fig. 2.2a and Fig. 2.2b show the power transistor current and corresponding drain voltage respectively. By multiplying the drain voltage and the current, we get the power dissipation in the transistor. It shows that about 50% of the DC power is wasted due to the biasing current.

The solution to the biasing power loss is to reduce the biasing current like Class C power amplifier which can partially remove this kind of power loss. As switch mode power amplifier such as Class-D and Class-E power amplifier do not need any biasing. They do not have biasing power loss. However, Class-C, D, E are nonlinear power amplifiers.
A linear modulation signal has the property of nonconstant envelope which causes matching network $V_{\text{bias}}$, $V_{\text{DD}}$, $R_{\text{FC}}$, $I_T$, $V_{\text{in}}$, $R_{\text{L}}$

Fig. 2.2a

Biasing current

Fig. 2.2b

$V_{\text{dd}}$

$V(t)$

$\therefore$ Max. efficiency is 50 %

2.2.2. Power loss due to envelope variation

A linear modulation signal has the property of nonconstant envelope which causes...
power loss in the power amplifier. Consider the signal in Fig. 2.3. To linearly amplify the signal, the power amplifier should be able to provide a maximum power that is equal to maximum output power. However, when the envelope is very small and only a small output power is needed. Then the remaining DC power is lost. Constant envelope modulation can solve this problem. But bandwidth efficiency need to be sacrificed. Other solutions include signal processing and coding techniques which can reduce the envelope variation. But, some other disadvantages exist in these techniques and will be discussed in later sections.

2.3 MCM (Multicarrier Modulation)

When data rate increases, the symbol period of single carrier modulation signal may be much shorter than the multipath delay. If this case occurs, ISI (inter symbol interference) will greatly affect the transceiver performance. Equalization can mitigate this to some extent, but typically at the cost of increased noise, so it leads to a transmitter power penalty or an increased vulnerability to interference. Multicarrier modulation (MCM) can be used to tackle this problem. The principle of MCM, shown in Fig. 2.4, is to transmit data by dividing the stream into several parallel bit streams, each of which has a much lower bit rate, and by using these substreams to modulate a number of subcarriers.

In earlier days, MCM concept is borrowed from the conventional FDM technology. Space is needed between each subcarrier for easy filtering in the receiver as illustrated in Fig. 2.5[1]. The space reduce the bandwidth efficiency. As the advance of both software and hardware technology, more fascinating multicarrier modulation techniques, which do not need the space between the subcarriers, evolve. In the next section, we show a special
scheme called OFDM which allows the subcarriers to be overlaid and thus high spectrum efficiency can be achieved.

**FIGURE 2.4. Multicarrier transmitter**

\[ \text{serial data bits} \rightarrow \text{Serial to parallel converter} \rightarrow \text{modulator} \rightarrow \text{output signal} \]

\[ f_{c1}, f_{c2} \text{ and } f_{cn} \text{ are subcarriers} \]

**FIGURE 2.5. Early MCM transmit power spectra**

\[ \text{amp} \rightarrow \text{freq.} \]

\[ f_{c_{n-1}}, f_{cn}, f_{c_{n+1}} \]

### 2.4 OFDM

The early application of OFDM (Orthogonal Frequency Division Multiplexing) is in military and it was gradually evolved from MCM technique. Each subcarrier in OFDM is orthogonal to other subcarriers and this condition is not always maintained in other MCM signals. Due to the orthogonality property, the subcarriers can be overlaid together and form a high bandwidth efficiency signal as shown in Fig. 2.6.

Originally, the subcarriers are generated by using an array of sinusoidal generators as
illustrated in Fig. 2.7. As the number of the subchannels becomes larger, sinusoidal generator array and coherent demodulators required in a parallel system become expensive and complex. The receiver needs precise phasing of the demodulating carriers and sampling times in order to keep crosstalk between subchannels acceptable[2].

FIGURE 2.6. OFDM signal spectrum

It appears clearly that OFDM signal can be generated easily using Fast Fourier Transform (FFT) at the transmitter and receiver. For a relatively long time, the complexity of a real time Fourier Transform appeared prohibitive. Until recently, the well developed VLSI technology makes FFT implementation more viable. Fig. 2.8 shows an FFT based OFDM system.

FIGURE 2.7. Early OFDM transmitter
Refer to the above figure, a high bit rate serial binary number is first mapped to a sequence of complex numbers \( (d_0, d_1, ..., d_{N-1}) \), where \( d_n = a_n + jb_n \). Then after performing FFT of the complex numbers, a vector \( D = (D_0, D_1, ..., D_{N-1}) \) of \( N \) complex numbers is obtained, where

\[
D_m = \sum_{n=0}^{N-1} d_n e^{-j(2\pi nm)/N} = \sum_{n=0}^{N-1} d_n e^{-j2\pi f_n t_m} \quad m = 0, 1, 2, ... N - 1
\]

where \( f_n = n/(N\Delta t) \), \( t_m = m\Delta t \) and \( \Delta t \) is the symbol duration of the serial data sequence \( d_n \). The parallel \( D_m \) data stream is then converted to serial output and then upsampled and applied to a low-pass filter, a continuous time that approximates the frequency division multiplexed signal is finally obtained. The I and Q of the final modulation signals are:

\[
I(t) = \sum_{n=0}^{N-1} (a_n \cos 2\pi f_n t + b_n \sin 2\pi f_n t) \quad 0 \leq t \leq N\Delta t \quad \text{(EQ 2.2)}
\]

\[
Q(t) = \sum_{n=0}^{N-1} (b_n \cos 2\pi f_n t - a_n \sin 2\pi f_n t) \quad 0 \leq t \leq N\Delta t \quad \text{(EQ 2.3)}
\]

After passing through the IQ modulator and being upconverted, the signal is power amplified and transmitted out.
Chapter 2: Power Amplifier and OFDM

The advantage of orthogonality of the subcarriers in OFDM signal is that the subchannels can be completely separated. However, when there are intersymbol interference (ISI) and interchannel interference (ICI) introduced by transmission channel distortion, energy from other subchannels will spread to adjacent channels. One way to prevent ISI is to precede each OFDM symbol with an extended guard interval $T_g$. So the total symbol duration is equal to $T + T_g$, where $T$ is the useful symbol duration. When the guard interval is larger than the maximum multipath delay, ISI can be avoided. However, other distortions such as frequency selective fading still exist. Coding techniques can be used to reduce this kind of distortion.

2.5 Peak to Average Power Ratio (PAPR)

The peak-to-average-power-ratio is a measurement of envelope signal fluctuation and is defined as:

$$PAPR = \frac{\text{MAX}_{0 \leq t < T} |s(t)|^2}{\int_0^T |s(t)|^2 dt}$$

As the output signal of OFDM transmitter is the result of all the subcarriers adding together with random amplitude and phase and each subcarrier is independently modulated, according to the Central Limit Theory, the resulting signal amplitude approaches a gaussian distribution as more and more subcarriers are added together. Therefore the envelope signal is Raleigh distributed with high peak to average power ratio. Because of this, all circuits between the modulator and the demodulator must be linear and with high dynamic range. But the most harmful effect is in the RF power amplifier. To reduce the distortion and spectral spreading, the OFDM signal should have enough back off from

$PAPR_{\text{MAX}} = \frac{1}{T} \int_0^T |s(t)|^2 dt$
power amplifier saturation region. But large back-off reduce the power efficiency to an unacceptable value. Fig. 2.9 shows the envelope distribution of a 64-QAM OFDM signal. If a Class-A power amplifier is applied and the signal is back-offed to avoid the clipping distortion, the average power efficiency is only about 5%.

FIGURE 2.9. Envelope distribution of 64-QAM OFDM

To reduce the the envelope fluctuation, many PAPR reduction techniques were proposed. These techniques are depicted in next section.

2.6 PAPR reduction techniques

The PAPR reduction techniques mainly belong to one of the following three groups: coding, clipping and signal processing. In the following subsections, these techniques are studied individually and disadvantages are pointed out.

2.6.1. Coding

Many different coding techniques have been proposed. If the number of the subcarriers is small, some of the coding techniques are quite attractive. But these techniques become very complex and the coding rate is low when the number of the subcarriers is large. Some
of the coding methods are shown below.

1) Selected mapping

Firstly, N distinct vectors \( P_n = [p_1^n, p_2^n, ..., p_D^n] \) with \( p_u^n = e^{j\varphi_u^n} \) are defined, where \( \varphi_u^n \in [0, 2\pi] \), \( u = 1:D, n = 1:N \) [3]. After mapping the input data to the subcarriers by FFT, we have the modulated vector \( V[u] \). \( V[u] \) is then multiplied with N vectors \( p_n \), resulting in a set of N different vectors as:

\[
V_n[u] \cdot e^{j\varphi_u^n} \quad \text{where} \quad n = 1...N
\]

Then, all the vectors are transformed to the time domain and the one with the lowest PAPR is selected.

Selected mapping technique is suitable for small number of subcarriers. But it is very complex for very large number of subcarriers. And choosing \( e^{j\varphi_u^n} \) properly is also a problem.

2.) Block coding

Block coding reduces the PAPR by avoiding transmitting the codewords which have large peak to mean envelope power ratio [4]. To find the codeword with the lowest PAPR, the PAPRs of all the codewords must be calculated. Also, there exists a tradeoff between the PAPR reduction and the coding rate. To lower PAPR, the coding rate should also be reduced.

3.) Golay sequences and Reed-Muller codes

The technique encodes \( \log_2(m!/2)+m+1 \) data bits to \( 2^m \) code bits so that the PAPR is at
most 2 and has a minimum distance of at least $2^m$ [5]. However, when $m$ is large, the coding rate is small. For example, the coding rate is less than 0.5 for $m=4$.

Actually, there is a limit that the PAPR can be reduced by coding according to [6]. It is also computation intensive to find a suitable codeword. So far, no coding solution is known which can maintain a reasonable coding rate for arbitrary numbers of subcarriers.

2.6.2. Clipping technique

The OFDM signal is intentionally clipped to reduce the PAPR. Clipping not only causes inband distortion, it also causes outband radiation. Adaptive clipping scheme can be employed to obtain the optimal clipping ratio by using appropriate real-time channel evaluation techniques[7]. However, the clipping distortion is still a limiting factor for large clipping ratio.

2.6.3. Signal processing

The signal processing method is to use some error correction functions to limit the PAPR and reduce the outband radiation[8]. However, it generated in band interference.

Although there is no proof that a low limit exists in PAPR reduction for the above-mentioned techniques, difficulty is expected to realize large PAPR improvement for complex OFDM signal such as 64-QAM OFDM with 1024 subcarriers. Therefore, a power amplifier with some linearity is required even when PAPR reduction techniques are used and, thus, the power amplifier efficiency remains low.
CHAPTER 3  

EER and Other Linearization Techniques

3.1 Introduction

Beside the PAPR reduction techniques mentioned in previous chapter, power amplifier linearization techniques are also considered to duel with the strong fluctuation of OFDM envelope signal. As these linearization techniques are complicated and require various adjustments, they only appear in some complex, expensive RF and microwave systems before. However, as wireless systems become more sophisticated and IC technologies can achieve higher level of reproduction, these linearization techniques will definitely find their ways into the low cost portable wireless systems.

Five linearization techniques are considered and compared on the aspects such as easy implementation, linearity and power efficiency.

3.2 Feedforward

A nonlinear power amplifier not only outputs the linear replication of its input signal, it also generates an error signal. The error signal creates inband distortion as well as outband
radiation which affects nearby receivers. To cancel the error signal, we may subtract it from the nonlinear power amplifier output signal before transmitting out. And this is exactly what the feedforward linearization technique does[9][10]. Fig.3.1 depicts the principle of the feedforward technique. The output signal of the main power amplifier is scaled by $1/A_v$, where $A_v$ is the signal gain of PA. The result then subtracts the input signal to produce the error signal. The error signal, after amplified by $A_v$, is then subtracted by the PA output signal. There are also two delay elements, $\phi_1$ and $\phi_2$, to match the time delay of the main PA and the error amplifier respectively.

**FIGURE 3.1. Feedforward linearization technique**

The advantage of the feedforward topology over a feedback method is its inherent stability even with finite bandwidth and substantial phase shift in each building block. Stability is an important factor to be considered for high frequency signal feedback loop. Because phase control is very difficult in high frequency. Also, the parasitic reactances become more significant and should be taken into consideration in the feedback compensation.

However, feedforward linearization nonetheless suffers from several shortcomings. First, the implementation of the analog delay elements requires passive devices, such as microstrip, which cause power loss. Second, the inputs of the second subtractor in the
feedforward PA are power signals. Therefore, a low loss device such as a high frequency transformer, which has large size, should be used. Third, the gain and phase in the two paths should be well-matched to reduce distortion. It can be shown [11] that if the two paths from $V_{in}$ to the inputs of the first subtractor exhibit a phase mismatch of $\Delta \phi$ and a relative gain mismatch of $\Delta A/A$, then the magnitude of IM products in $V_{out}$ is suppressed by

$$E = \sqrt{1 - 2(1 + \Delta A/A) \cos \Delta \phi + (1 + \Delta A/A)^2} \quad (EQ \ 3.1)$$

However, the phase shift in the main power amplifier and the error amplifier varies with the input signal frequency. If a wideband signal is applied, different frequency components will have different amount of phase shifts. Since a simple delay line can only produce linear phase shift, it is difficult to cancel the complex phase shift. Some researchers proposed a method to deal with this problem by adding a phase equalizer in the reference path to cancel the phase mismatch as shown in Fig. 3.2. But difficulty is expected to implement the equalizer to compensate the complex phase shift of a practical power amplifier.

**FIGURE 3.2. Feedforward technique with phase equalizer**

Therefore, the feedforward technique is suitable only for narrow band signal. Also, the main amplifier should be a linear power amplifier which has a low power efficiency.
3.3 Feedback

In the feedforward system, the nonlinearity reduction corresponds to how well the phase and amplitude match in the two paths. However, due to temperature and aging effects, the phase and amplitude characteristics of the two paths should be adaptively controlled, otherwise the performance will gradually degrade. The negative feedback method has the advantage that constant compensation is maintained as long as the system is stable. There are three ways to implement the feedback amplifier: RF feedback, IF feedback and cartesian feedback methods[12].

**FIGURE 3.3. Principle of feedback technique**

![Feedback Principle Diagram](image)

3.3.1. RF feedback:

Fig.3.3 shows the model of an RF feedback amplifier[13]. Assume that the input (x) and output (y) characteristics of a nonlinear power amplifier are given as

\[
y = Ax + B\Delta x \quad \text{(EQ 3.2)}
\]

where \(Ax\) and \(B\Delta x\) denote the linear and nonlinear component respectively. Since the feedback amplifier decreases the total gain by the feedback factor \(A\beta\). Therefore a pre-amplifier is needed to compensate the gain loss. The voltage input \(x\) and output \(y\) characteristics of feedback amplifier are given as

\[
x' = A\beta x + \beta y \quad \text{(EQ 3.3)}
\]
From the above two equations, the output voltage $y$ becomes

$$y = A x' + B \Delta(x')$$ \hspace{1cm} (EQ 3.4)

The equation shows that the nonlinear components are reduced by $1/A\beta$ times.

A negative feedback amplifier may be unstable. For supressing the oscillation, a band-pass loop filter should be inserted. Fig. 3.4 shows two methods to place the loop filter. The transfer function $H(\omega)$ of the two feedback amplifiers are given as

a) $BPF(\omega)$ is in the feedback loop

$$H(\omega) = \frac{Amp(\omega)}{1 + Amp(\omega) \cdot BPF(\omega) \cdot \beta}$$ \hspace{1cm} (EQ 3.6)

b) $BPF(\omega)$ is in the main loop

$$H(\omega) = \frac{Amp(\omega) \cdot BPF(\omega)}{1 + Amp(\omega) \cdot BPF(\omega) \cdot \beta}$$ \hspace{1cm} (EQ 3.7)

From the above two equations, the out band harmonic distortion can be suppressed only when the loop filter is the in the main loop.

3.3.2.) IF feedback:
High frequency amplifier is difficult to achieve high gain and also can easily cause excessive phase shift which is the major consideration for a feedback system. To alleviate these problems, the output signal can be down-converted to a low frequency before comparing with the original signal such as the one illustrated in Fig. 3.5[14].

**FIGURE 3.5. IF feedback**

![IF feedback diagram](image)

**FIGURE 3.6. Cartesian feedback**

![Cartesian feedback diagram](image)

### 3.3.3. Cartesian feedback:

Fig. 3.6 shows the cartesian feedback structure. The PA output is first decomposed to I and Q signals before it is compared with the original baseband signal[15]. The complexity of the cartesian feedback makes it unpopular for portable terminal design. Also the added components increase the cost and power dissipation.

Like the feedforward technique, the feedback method requires a linear low efficiency
power amplifier. Moreover, the stability problem and the complexity make it not favorite to be applied in portable communication systems.

3.4 Predistortion

Predistortion is to estimate the nonlinearity of power amplifier so as to cancel it like the one in Fig. 3.7 [16]. The predistortion device (PD) can be implemented either at IF by means of analog circuitry, or at basband with digital components. The later solution is usually preferred, since it is better suited to the realization of adaptive PD, capable of tracking any possible change in the HPA parameters such as drifts due to temperature and aging, variation of the operation point etc. The complexity of the PD, either analog or digital, strictly depends upon the number of mathematical operations involved in the predistortion algorithm. When the PD is to be implemented digitally, complexity depends on the number of the samples to be processed per unit time.

A linear power amplifier is required for predistortion technique. To have better cancellation of the nonlinear components of the PA, the predistortion algorithm needs to be more complex and thus adds the cost and the power consumption. Therefore, predistortion technique also does not suit for portable systems.
3.5 LINC (Linear Power Amplifier using Nonlinear Components)

Fig. 3.8 illustrates the LINC technique [17]. The idea is that a bandpass signal with complex envelope \( s(t) \) can be expressed as

\[
s(t) = s_1(t) + s_2(t)
\]

\[(\text{EQ} \ 3.8)\]

where

\[
s_1(t) = s(t)/2 - (-1)^i \theta(t) \quad i = 1, 2
\]

\[(\text{EQ} \ 3.9)\]

and

\[
\theta(t) = \frac{i}{2} \alpha s(t) \sqrt{\frac{s_M^2}{|s(t)|^2} - 1}
\]

\[(\text{EQ} \ 3.10)\]

for \( 0 < \alpha \leq 1 \) and \( |s(t)| \leq s_M \).

From the above three equations, it is clear that \( |s_1(t)| \) and \( |s_2(t)| \) fluctuate between \( \alpha s_M(t)/2 \) and \( S_M(t)/2 \). This means that if \( \alpha = 1 \), then \( s_1(t) \) and \( s_2(t) \) are constant and can be power amplified by high efficiency non-linear power amplifiers.

However, the major drawback with this technique is its sensitivity to gain and phase...
mismatch of the two power amplifiers. The output adder also introduces significant loss for the need of a high isolation between the two PAs. Normally, the adder is designed using some microwave devices like hybrid power combiner. Thus single chip integration is difficult to achieve.

3.6 EER (Envelope Elimination and Restoration)

The basic principle of the EER technique, which is shown in Fig. 3.9, relies on the fact that any bandlimited signal can be regarded as an amplitude modulation of a constant-amplitude phase signal [18]. Because of this fact, the phase signal and envelope signal can be amplified individually. Consider an OFDM baseband complex signal during a block period in continuous time domain as expressed below

$$S(t) = I(t) + Q(t)$$

$$= \sum_{k = -N/2}^{N/2 - 1} \chi[k]e^{j2\pi kt/T}, \text{ for } t \in [0, (T + \Delta)]$$

(EQ 3.11)

where $N$ is the number of carriers, $\chi[k]$ is the complex modulating data symbols, $T$ is the symbol period, and $\Delta$ is the guard interval. The envelope and phase information can be obtained from the baseband signal $S(t)$. The phase signal after being upconverted is expressed as

$$C(t) = \cos(\omega_c t + \theta(t))$$

(EQ 3.12)

where

$$\theta(t) = \text{atan} \left( \frac{Q(t)}{I(t)} \right)$$

(EQ 3.13)
At the same time, the envelope signal $R(t)$, its distribution illustrated in Fig. 3.9, is equal to

$$R(t) = \sqrt{I^2(t) + Q^2(t)}$$ \hspace{1cm} (EQ 3.14)

A switching power supply is used to amplify $R(t)$ for its high efficiency even at low signal level. To reduce switching harmonics, a low-pass filter at the switching power supply output is added. $C(t)$, for its constant amplitude, can be amplified by a non-linear R.F. power amplifier.

The condition to apply EER technique is that the power amplifier output signal amplitude should linearly change with its drain voltage. That means

$$P_{OUT} \propto V_{DD}^2$$ \hspace{1cm} (EQ 3.15)

To see whether this is true or not for switch mode power amplifier. Class-E PA is considered and simulated in Hspice. Fig. 3.10 shows an ideal Class-E power amplifier [19][20]. In practice, $S$ is a transistor which acts as switch. The phase signal $C(t)$ turns the transistor on and off and charges and discharges $C_p$. Careful design of the circuits ensures that no voltage exists across the transistor while the current passes through it. In theory, efficiency
can reach 100%. Simulation result using HSPICE with Bsim3 CMOS transistor shows that the output voltage changes linearly with supply voltage $V_{dd}$ (see Fig. 3.11). Therefore, the restoration of the envelope to the phase signal can be done by amplitude modulation of the power supply of Class-E power amplifier with $R(t)$.

The average power efficiency of EER PA neglecting other peripheral circuits is calculated as following [21]

\[
\eta = \frac{P_{oavg}}{P_{isupply, avg}} = \frac{P_{oavg}}{(P_{oavg}/\eta_{RF})/\eta_{supply}} = \eta_{RF} \eta_{supply}
\]

$P_{oavg}$ is the average output power of the RF power amplifier. $P_{isupply, avg}$ is the average input power to the switching power supply provided by the DC power supply. $\eta_{RF}$ and $\eta_{supply}$ is the power efficiency of the RF power amplifier and the switching power supply, respectively. The switching power supply has a maximum efficiency of 80% and will be shown in later section. From the HSPICE simulation results shown in Fig. 3.11, a class-E RF power amplifier gives an efficiency of above 80% for the entire supply voltage range.
that is simulated. Thus, the EER technique can achieve a power efficiency of more than 64%, far better than a Class-A PA.

![Figure 3.11. Class E PA performance](image)

![Figure 3.12. EER transmitter](image)

Originally, EER linearization scheme as first proposed by Khan used limiter and envelope detector to produce phase and envelope signal. However, the limiter, which operates in the RF frequency range does not have enough gain to generate constant envelope. Also, the limiting process is easy to generate AM/PM distortion. According to [22], The IMD (Inter Modulation Distortion) response of a non-ideal limiter (with finite gain) can be approximated by

\[ IMD = \frac{2}{3\pi} \sin^2 e \]

(EQ 3.17)
where $e$ is the limiting angle. To reduce distortion, the envelope and phase signals are generated at the baseband instead of using an envelope detector and limiter to separate them in RF. If the RF PA is switch mode, then the baseband phase signals should be upconverted in two stages, as shown in Fig. 3.13, to alleviate the disturbance of the local oscillator by the power amplifier output.

Compare to other linearization techniques such as feedforward, feedback, LINC and predistortion, EER scheme can employ non-linear PA for both envelope and phase signals. Therefore the efficiency is higher. Moreover, all the components in the scheme can be easily integrated.

### 3.7 Conclusion

In this chapter, different types of linearization techniques have been studied. Compared with other techniques, EER scheme is a better choice for portable wireless system due to its higher power efficiency and easy for integration. However, there are still some factors which can greatly affect the performance of the EER technique and the analysis of EER PA performance on OFDM system is given in the next chapter.
CHAPTER 4 Analysis of OFDM System with EER PA

4.1 Introduction

From previous chapters, it is known that the major obstacle in applying OFDM in wireless portable system is the need of a highly linear and efficient R.F. power amplifier. The strong fluctuation of an OFDM envelope signal makes it difficult to achieve both the linearity and efficiency at the same time for classical linear PAs.

As EER is a linearization technique which can achieve PA with both high linearity and high power efficiency. We may wonder what is the performance of the system if we apply EER scheme on wideband OFDM signal and how to choose the parameters of EER technique so that the performance is optimized. In this chapter, an OFDM signal with 5MHz bandwidth is applied on EER linearized power amplifier and the performance trade-offs are evaluated. The results are compared to the performance of a linear power amplifier with different power backoffs.

The linearity of an EER system depends not only on the linearity of the switching power supply and the RF power amplifier, but also on the other system parameters. The following parameters will be considered for their effects on BER (bit error ratio): 1) low
pass filter bandwidth at the output of switching power supply; 2) time mismatch between envelope and phase signals; and 3) envelope clipping by switching power supply.

4.2 Simulation setup

The simulation model of an OFDM transmission system is depicted in Fig. 4.1. To consider a more stringent case, a 5 MHz bandwidth 64 QAM OFDM with N = 1024 subcarriers is simulated. To accurately model the effect of the EER power amplifier on OFDM signal, we run the simulation of power amplifier on RF band using EEsof Communications Design Suit[23], while the baseband stages are modeled by MATLAB.

In the simulation, a serial binary data stream first passes through a channel coding scheme. The coding scheme includes a convolution encoder concatenated with a bit interleaver. The convolution code, with a code rate $R = 2/3$, has a constraint length of 3 [24]. The bit interleaver is used to spread bit errors over the whole OFDM symbol in a block interleaver with 96 rows and 64 columns. The coded bit sequence is then mapped into 64-QAM for each subcarrier. After that, an inverse fast fourier transforms (IFFT) is processed to calculate the discrete time OFDM signal. Then, a guard interval of 1 µs is added to pre-
vent adjacent OFDM blocks from interfering with each other due to the delay spread.

To increase time resolution, the signals are upsampled respectively so that each of them comprises $N \times m$ samples within an OFDM symbol in the simulation, where $m$ is the number of samples per symbol. The effect of $m$ on BER is shown in Fig. 4.2. The difference between $m=16$ and $m=32$ is small. For simplification, we only consider $m=16$ from now on.

**FIGURE 4.2. Upsampling ratio and BER**

A 256-tap raised-cosine low-pass filter is then used for interpolation. The roll-off factor of the raised cosine filter affects the resistance of the receiver to the sampling time mismatch effect (higher roll-off factor has higher resistance to time mismatch), the envelope is not significantly affected by the roll-off factor, as shown in Fig. 4.3. But Fig. 4.4 shows that the roll-off factor has great effect on signal bandwidth. For higher bandwidth efficiency, a small roll-off factor of 0.25 is chosen.

In order to apply the EER technique for power amplification, the envelope and phase signals are generated in baseband. The phase signals are then upconverted to 835 MHz.
The recombination of envelope and phases is done in the EER power amplifier. To model the effect of frequency selective fading for an indoor environment, a static two-rays multipath channel model as [25][26] employed is used [see Fig 4.5]. The model consists of a direct path signals plus a signal path delayed by $\tau = 0.1 \mu s$. The direct path has a gain of 1 while the delayed path is attenuated by $\beta = 0.7$. The frequency transfer function [see Fig.4.5b] is

$$H(\omega) = 1 + \beta e^{j(\omega \tau + \theta)}$$  \hspace{1cm} (EQ 4.1)
Furthermore, a bandpass AWGN is also added after the two rays channel model. The operation of the receiver is the reverse of the transmitter. After downsampling and taking FFT, we have N received values

\[ y_k = h_k \cdot \chi_k + n_k; \quad k = 1, 2, ..., N \]  

(EQ 4.2)

where \( \chi_k \) is the transmitted state of subcarrier \( k \), \( h_k \) is the frequency response at subcarrier \( k \) and \( n_k \) is the noise. Since a coherent 64-QAM is used in the simulation in order to estimate the transmitted state \( \chi_k \), the channel response factor \( h_k \) must be known. We assume the frequency response factor \( h_k \) can be determined from (4.1). Then, the transmitted state \( \chi_k \) of each subcarrier in the 64-QAM constellation diagram is evaluated as

\[ \chi_k = \frac{y_k}{h_k} \]  

(EQ 4.3)

For decoding, a Viterbi hard decision decoder is used for convolution decoding.
4.3 Simulation Results

4.3.1. Low Pass Filter Bandwidth

The low-pass filter at the switching power supply output limits the envelope bandwidth. To see the effect of a low-pass filter bandwidth on BER performance, a second order Butterworth filter is used in the simulation. The delay of the filter is compensated for. Therefore, only the effect of the filter bandwidth is considered. Fig. 4.6 illustrates the effect of the low-pass filter by sweeping bandwidth versus BER with the signal-to-noise ratio (SNR) fixed at 23 dB. It shows that, as the bandwidth is larger than 12 MHz, its effect on the BER becomes smaller. Comparison between amplitude clipping and envelope bandwidth clipping is also done.

FIGURE 4.6. BER with varying LPF bandwidth

Two cases are considered for amplitude clipping. Fig. 4.7 shows the case of using soft limiter for amplitude clipping. The soft limiter is defined as

\[
V_{\text{out}} = \begin{cases} 
V_{\text{max}} & \text{if } K \cdot V_{\text{in}} > V_{\text{max}} \\
K \cdot V_{\text{in}} & \text{if } V_{\text{min}} \leq K \cdot V_{\text{in}} \leq V_{\text{max}} \\
V_{\text{min}} & \text{if } K \cdot V_{\text{in}} < V_{\text{min}} 
\end{cases} \tag{EQ 4.4}
\]
where $V_{in}$ and $V_{out}$ are the input and output signal of the soft limiter, respectively. $K$ is a constant gain. In our case, no lower limit is artificially set and minimum $V_{out}$ is equal to zero. The results indicate that the loss in SNR when using a 12 MHz bandwidth is about 0.3 dB at an SNR of 23 dB compared to no clipping, and about 0.1 dB compared to 9 dB OBO. At 9 dB OBO, clipping occurs less than 0.1% of the time. Thus, the 12 MHz bandwidth degrades the BER performance just like a small percentage clipping of the envelope.

**FIGURE 4.7.** Comparison of LPF bandwidth effect and OBO of a linear PA with soft clipping

![Graph 4.7](image1)

**FIGURE 4.8.** Comparison of LPF bandwidth effect and OBO of a linear PA

![Graph 4.8](image2)

To consider a more realistic case, the input signal power is fixed at 0 dBm and a linear
power amplifier is modeled with its gain and output third-order intercept point equal to 22 dB and 40 dBm, respectively. Its 1-dB compression point is varied to analyze the effect of back-off by varying the input-output power characteristic of the power amplifier. The results in Fig. 4.8 show that the low-pass filter with an 8 MHz bandwidth has a comparable performance with 9 dB OBO. The loss in SNR is about 0.7 dB at SNR of 23 dB compared with the ideal case. Therefore, a LPF with 12 MHz bandwidth, which is 2.4 times the RF signal bandwidth, is sufficient to provide a satisfactory performance.

**FIGURE 4.9. Time mismatch effect of phase and envelope signal on BER**

![Graph showing the effect of time mismatch on BER](chart.png)

**4.3.2 Time Mismatch Between Envelope and Phase**

To increase delay time resolution, higher upsampling rate is used. As the results in Fig. 4.9 indicated, a time-delay mismatch between the envelope and the phase signals has a great impact on BER performance. A 5-ns delay mismatch degrades the performance nearly the same as an 8 dB OBO does using a soft limiter, while a 20 ns (0.1/RF bandwidth) time delay mismatch will destroy the 5 MHz OFDM system. Since time delay will be introduced to the envelope signal by the low-pass filter at the switching supply output (for a second order 20 MHz bandwidth Butterworth filter, the delay time is 10 ns), a delay
line must be added at the phase signal to compensate for it. In addition, rather than adding a delay line for time handshaking, an envelope feedback can be used as shown in Fig.4.10.

**FIGURE 4.10. Envelope feedback**

![Envelope feedback](image)

To see the effectiveness of using an envelope feedback to reduce the impact of time delay mismatch caused by the filter, we compare an EER PA with envelope feedback and one without envelope feedback. A second order 20 MHz Butterworth filter is used in the two cases and no delay lines are added for compensation. The simulation results in Fig. 4.11 show that envelope feedback can effectively reduce the delay mismatch effect.

**FIGURE 4.11. Envelope feedback to reduce the time mismatch**

![Envelope feedback to reduce the time mismatch](image)
4.3.3 Power Efficiency and Supply Voltage

Before talking about the envelope clipping, let’s consider the relationship between power efficiency and supply voltage. We know that the PA output power is equal to $V_o \cdot I_o$ and also the maximum output voltage is about the same as the supply voltage for most power amplifiers. So when we reduce the supply voltage but want to keep the output power, then the only thing we can do is to increase the output current. That means we should decrease the output loading. However, when we decrease the output loading, the parasitic resistance becomes more significant and more power is dissipated. As shown in Fig. 4.12, the maximum efficiency is equal to

$$\eta = \frac{I^2 R_P}{I^2 (R_o + R_P)} \tag{EQ 4.5}$$

$$= \frac{R_o}{R_o + R_P}$$

Therefore, to build a highly efficient power amplifier, we should use the supply voltage more efficiently.

**FIGURE 4.12. Parasitic resistance effect**

RP is parasitic resistance.

4.3.4 Power Efficiency and Envelope Clipping

However, the envelope (supply voltage of RF PA in EER scheme) of OFDM signal is Raleigh distributed. To avoid clipping, the signal should be back-offed from its maxi-
minimum value (supply voltage). From Fig. 4.13, when signal is back-offed, more supply voltage is lost and so the power efficiency decreases. To use the supply voltage more efficiently, the envelope signal should be amplified larger. But, clipping distortion increases at the PA output. So, there exists trade-off between power efficiency and clipping distortion. It is difficult to consider the trade-offs between efficiency and clipping without practical measurement. Therefore, we consider another point: BER and clipping relationship.

**FIGURE 4.13. Envelope distribution with different amplification factors.**

4.3.5 BER and Envelope Clipping

As the OFDM envelope signal is Raleigh distributed, most of the signal is at low level. For a low power supply voltage, a Raleigh distributed envelope signal will keep the average power output and efficiency of RF power amplifier low if no clipping is allowed at switching power supply. This can be seen by the fact that the output power of a Class E power amplifier is equal to

$$P_o = \frac{0.577 \cdot V_{dd}^2}{R_L}$$

; $R_L$ is the load of PA  \(\text{(EQ 4.6)}\)
which is directly related to Vdd (or the envelope signal at switching power supply output).

To increase the average output power, clipping is inevitable due to the saturation voltage of the switching power supply when a larger output envelope signal level is needed. Simulation is done to examine the trade-off between the output power (or SNR with fixed noise level) and clipping distortion (fixed clipping level using soft limiter) by varying the envelope signal, as shown in Fig. 4.13. The envelope signal is shaped by a second-order 12 MHz low pass filter, and the time delay caused by it is compensated. Fig 4.14 illustrates the optimum clipping level in BER for several noise levels (for the same curve, the noise level is the same and only the signal power is varied.). The SNR in the legend of the graph are measured when envelope is not clipped. The clipping ratio is defined as $CR = A/\sigma$, where $A$ is clipping level and $\sigma$ is the standard deviation of envelope signal. When clipping increases, the BER is dominated by clipping distortion. While, the BER is dominated by noise when clipping is reduced. For a large noise-level (low SNR), the optimum clipping ratio is large (small clipping percentage) when the noise level is low (large SNR).

**FIGURE 4.14. Clipping effect and noise effect**

![Clipping effect and noise effect graph](image)

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As clipping ratio decreases, the clipping distortion and efficiency of power amplifier increases. Fig. 4.15 compares BER performance and efficiency of an ideal class A PA at different clipping ratios by using soft limiter. The power efficiency at minimum BER is about 9%. When clipping ratio is larger than the optimum point where BER is minimum, the BER and power efficiency degrade. Therefore, clipping ratio should be equal to or smaller than the optimum point.

**FIGURE 4.15. BER and class A power efficiency at different clipping levels.**

![Graph showing BER and class A power efficiency at different clipping levels.](image)

### 4.4 Conclusion

An OFDM transmission system using EER power amplifier was simulated and the effects of its parameters on BER were evaluated. A high performance EER PA can be achieved by: 1) a large envelope cutoff bandwidth (12 MHz for 5 MHz OFDM or 2.4 times RF signal bandwidth); 2) a time delay mismatch between the phase and envelope path which is less than 0.025/(RFbandwidth) (5 ns for a 5 MHz OFDM signal) in order to keep the loss in SNR less than 0.5 dB at SNR of 23 dB (feedback can be an effective way to reduce the impact of delay mismatch); and 3) trade-off between clipping distortion and SNR to obtain optimum BER performance.
5.1 Introduction

DC-DC power converter is originally used to regulate DC supply voltage and conventionally classified to three types, namely buck, boost and flyback converter. Fig. 5.1 shows a power converter with the buck topology.

To regulate dc signal, Vref in Fig. 5.1 is fixed. In our case Vref is the input signal which includes ac and dc components. The modulation can be pulse width modulation (PWM), delta modulation or sigma delta modulation. Except for dc regulation, power converters are also used for audio amplification for their high power efficiency. Khan is the first person to apply PWM power converter on the EER linearization scheme in 1952. However, due to some disadvantages, PWM is not good for amplifying large bandwidth signal com-
pared to delta modulation. Sigma delta may cause stability problem in our EER PA, so we will not consider it. Therefore, the power converter we designed uses delta modulation technique.

This chapter begins with the analysis and comparison of PWM and delta modulation power converter. Then the design of a wideband DC-DC power converter is followed and the performance of the converter will be shown at the end of the chapter.

5.2 Pulse Width Modulation (PWM)

Fig. 5.2 shows the PWM scheme using comparator method. The input signal and a triangular wave with fixed frequency are compared. The comparator produces a “high” when the input signal is larger than the triangular wave, and a “low” when the opposite is the case. So the result is that the width of “high” pulses (or duty cycle) varies linearly with the input signal amplitude. Since the triangular wave frequency is fixed, the output square wave frequency is also fixed and only the duty cycle varies.

The linearity of PWM depends on the speed of the comparator and the linearity of triangular wave. To have higher linearity, triangular wave is normally generated using function generator. For cost and power consideration, triangular wave may be obtained by
integration of a square wave using an RC integrator. However, the linearity of the output triangular wave is definitely worse as shown in the following equation[21]

\[
V_o(t) = V_{cc}(1 - e^{-t/RC}) = V_{cc}\left(\frac{t}{RC} - \frac{t^2}{2!R^2C^2} + \frac{t^3}{3!R^3C^3} - \ldots\right)
\]  

(EQ 5.1)

All other terms cause distortion. Therefore, it requires \( t << RC \).

PWM inherently is a nonlinear process which produces harmonic distortion of the modulation signal even if the modulator produces perfectly timed pulse. The reason is due to the varied switching frequency resulting spurious sidebands which may fall in the signal band. According to [21], if the input signal is a sinusoidal wave with amplitude \( V_{om} < V_{cc}/2 \), the magnitude of the nth spurious product associated with the kth harmonic of the switching frequency is

\[
V_{k,n} = \frac{2V_{cc}}{k\pi J_n}\left(\frac{k\pi V_{om}}{V_{cc}}\right)
\]  

(EQ 5.2)

If some of the spurious products fall in the passband, the low pass filter at the output cannot remove them and the signal is distorted.

### 5.3 Delta Modulation

Delta modulation is an alternative to PWM for providing square wave to represent input sinusoidal voltage [27]. A block diagram of an original delta modulator is illustrated in Fig.5.3. The input signal to the buffer, \( X(t) \), can be expressed as

\[
X(t) = \sum_{n = -\infty}^{\infty} \Delta(nT_s)\delta(t-nT_s)
\]  

(EQ 5.3)
where $\Delta(nT_s)$ is the difference between input and output signal and $T_s$ is the clock period. $X(t)$ is a return-to-zero signal with switching frequency equal to the clock frequency. The gate driving power loss of the buffer becomes significant if the clock frequency is large. Also, the power loss, and so the power efficiency, depends on the clock frequency. Thus, a latch is used to change return-to-zero signal to non-return-to-zero signal. Another point is that the integrator is not good to remove switching harmonics. A higher order low pass filter is used to replace it. Fig. 5.4 shows a delta modulator with non-return-to-zero square wave and second order low pass filter. This delta modulator is used in our design of DC-DC power converter.

**FIGURE 5.3. Delta modulation**

**FIGURE 5.4. Revised delta modulation**

Delta modulation’s major advantage over PWM is that it guarantees that the on and off
times of the output square wave will not fall below a certain minimum value. This ensures that the output buffer (large inverter) never makes two switching operations in quick succession. For high input frequency, this becomes more important because the buffer may not follow such fast switching and so error (distortion) is generated.

The largest difference between delta modulation and PWM is that both the frequency and the duty cycle of the output square wave in delta modulation change with the input signal. This makes the analysis of the system very difficult. On the other hand, since there is only one changing variable (duty cycle) in PWM system, the analysis is easier and conventional linear feedback theory can be applied in stability consideration. This is not the case for delta modulation. Therefore, during the design of the DC-DC power converter using delta modulation, we heavily rely on simulation to find the optimum parameters for the power converter.

### 5.4 Output Spectrum Analysis

The square waveform that is produced by delta modulator may best be visualized by considering a system which try to estimate the input signal by ramping up and down within a given margin of error. The process is illustrated in Fig. 5.5. The square waveform is analysed in [28], where it was shown that the on and off time are given in equation (5.4) and (5.5). The calculation is depicted in Fig. 5.6. The duty cycle and frequency of the waveform are given in equation (5.6) and (5.7) respectively.

\[
\tau_{on} = \frac{h}{sR} \cdot \frac{1}{1 - m} \tag{EQ 5.4}
\]
where \( m = s_m / s_R \), \( h \) is the error margin and \( f_{\text{idle}} = s_R / 2h \). Under normal condition, \( s_m \) is varied such that \( m \) is given as

\[
m = M \cdot \sin(2\pi f_{\text{mod}} t)
\]

From the above equation, we know how the duty cycle and switching frequency change with input signal. By Fourier expansion, the spectrum of the square wave, \( r(t) \), is then equal to

\[
r(t) = m \cdot V / 2 + \sum_{i=1}^{\infty} \sum_{n=-\infty}^{\infty} A_i(n) J_n(\beta) \cos(2\pi t(i f_{\text{car}} + 2n f_{\text{mod}}))
\]

where \( A_i(n) \) is equal to

\[
A_i(n) = \frac{V}{i\pi} \sin\left(\frac{i\pi}{2} 1 + \sqrt{1 - \frac{i f_{\text{car}}}{2} + \frac{n f_{\text{mod}}}{2}}\right)
\]

\( \beta \) is given as \( f_{\text{car}} / (2 * f_{\text{mod}}) \) and \( J_n(\beta) \) is a Bessel function of the first kind, order \( n \) and argument \( \beta \). \( f_{\text{mod}} \) is input frequency and \( f_{\text{car}} \) is given as

\[
f_{\text{car}} = f_{\text{idle}} \left(1 - \frac{M^2}{2}\right)
\]

The above formulae are the only mathematical models that can be found so far for delta modulator analysis. However, in our case, the models give no much help on the power converter design.
5.5 DC-DC Power Converter Parameters

Fig. 5.3 shows that the DC-DC power converter is a non-linear feedback system. The analysis of the system is very difficult as just mentioned above and the conventional feedback theory cannot be applied here. Therefore, the determination of the parameters of the system heavily relies on simulation.

The parameters to be decided for circuit design are the gain of the input stage, the clock frequency in the comparator stage and the low-pass filter bandwidth. To attenuate the switching harmonics as much as possible, the low-pass filter bandwidth is set to be equal to the input signal bandwidth. And simulation shows that the adjustment of the gain of the
input stage and the clock frequency do not help the stabilization of the feedback loop. Moreover, there is no other parameter that can be controlled. So to avoid the oscillation of the loop, a compensation element, $G(s)$, is inserted as shown in Fig. 5.7. $G(s)$ is a phase lead compensator with the transfer function given as

$$G(s) = \frac{s+z}{s+p} \quad \text{where} \; z \ll p$$  \hspace{1cm} (EQ 5.12)

**FIGURE 5.7. Compensation of the power converter**

![Compensation of the power converter diagram](image)

Fig. 5.8 shows the frequency response of $G(s)$. It generally amplifies the high frequency components and keeps the low frequency components the same. Since the comparator can only detect whether its input signal is larger or smaller than zero. If $G(s)$ is not used, the small high frequency fluctuations in the error signal (the difference between the input and output signal of the power converter) cannot be detected by comparator and will be totally ignored in the feedback system. Fig. 5.9 shows the error signal and comparator output signal of the power converter in the case that $G(s)$ is not used. It reveals that the small fluctuation does not affect the comparator decision. Fig 5.10 shows the case when $G(s)$ is inserted. $G(s)$ amplifies the small high frequency disturbance and makes it visible to the comparator. Therefore the function of $G(s)$ is to make the feedback loop more robust to the high frequency distortion.
FIGURE 5.8. Frequency response of the compensator

FIGURE 5.9. Signals without compensator

FIGURE 5.10. Signals with compensator
Due to the strong nonlinear feedback loop, circuit simulation of the power converter takes a lot of time. To save time, the system is first simulated using ideal blocks. The parameters are then chosen and tuned to the best performance before circuit design. Fig 5.11 is the output frequency spectrum of ideal block simulation. Fig. 5.12 shows the total harmonic distortion (THD) with different input signal frequencies and clock frequencies. The figure shows that when input signal frequency is lower, the distortion becomes higher. This is due to the fact that the low-pass filter bandwidth at the power converter output is fixed and the first few harmonics may remain in the passband when the input is a low frequency signal. Another point is that clock frequency higher than 500 MHz does not give apparent improvement in the performance of the power converter. Therefore, the clock frequency is set to 500 MHz.

The delay in a closed loop system causes distortion. Therefore, it is better to minimize the loop delay as much as possible. However, in the power converter, the loop delay is related to the size of the buffer. And the buffer size also determines the power efficiency of the converter. So the buffer size can be determined by the trade-off between distortion and
power efficiency. The relationship between distortion and the delay is explored by sweeping the loop delay and taking measurement of output signal total harmonic distortion as illustrated in Fig. 5.13. The graph shows that THD rises rapidly when delay is larger than 3 ns. Therefore, the total loop delay should be kept in 3 ns when choosing the buffer size.

**FIGURE 5.12. THD with different input signal frequencies and clock frequencies**

![THD with different input signal frequencies and clock frequencies](image)

**FIGURE 5.13. Distortion caused by loop delay**

![Distortion caused by loop delay](image)

The required parameters of the power converter obtained from ideal block simulation are summarized in the following:
1) The speed of the comparator is equal to input signal bandwidth (5 MHz)
   - when speed decrease, the distortion will increase. When speed increase, the comparator is difficult to build.
   - From Fig. 5.12, higher speed doesn't give much improvement

2) The delay should be less than 3 ns

3) The bandwidth of the low pass filter is set to 5 MHz
   - \( R_L \) is fixed at 12 ohms; \( L = 200 \text{ nH} \); \( C = 10 \text{nF} \)

4) The phase lead compensator is set as:
   - \( Z = 1 \text{e-8} \); \( P = 1 \text{e-9} \)

**FIGURE 5.14. Implementation of the power converter**

As the parameters are known, the circuit design can start. The detailed implementation of the power converter is shown in Fig. 5.14. The converter is implemented using AMS 0.8 \( \mu \text{m} \) BiCMOS process. The process has double poly, double metal and twin well[29]. To reduce the noise effect, differential circuit design is followed. There are only two external components. The supply voltage in final stage can be 3.3 to 5 V to control different RF
power amplifiers. In next section, the circuit design of each individual block in the power converter is introduced.

5.6 Circuit Implementation

5.6.1. Input stage

The input stage is a bipolar differential pair with resistor loading as shown in Fig. 5.15. R1 and R2 provide the biasing and also the feedback attenuation. The ratio of R2 to R1 is 9, therefore the feedback signal is attenuated by 10 before comparing with the input signal. The gain of the input stage is about 15. For power consideration and the effects of the poles, the gain should not be set too large.

![Input differential pair](image)

5.6.2. Phase Lead Compensator

Fig. 5.16 shows the compensator which looks like a emitter degenarator. The two transistors in the emitter act as resistors with tuning capability. using the small signal analysis, the transfer function is equal to
\[
T(s) = \frac{-\beta R_c (1 + R_e C_e S)(1 + R \pi C \pi S)}{[R \pi + (1 + \beta) R_e][1 + (R_e R \pi C_e + (1 + \beta) R_e R \pi C \pi) S/(R \pi + (1 + \beta) R_e)]}
\]  

(EQ 5.13)

When \( R \pi C \pi \ll R_e C_e \), then \( T(s) = (S+Z)/(S+P) \) with \( Z > P \). Fig. 5.17 compares the phase transfer function of the circuit and the ideal compensator. It shows that the circuit in Fig. 5.16 gives the compensator we want.

**FIGURE 5.16. Phase lead compensator**

**FIGURE 5.17. Phase transfer function**

5.6.3. Comparator

The comparator includes pre-amplifier, regeneration and latch as illustrated in Fig. 5.18. There are two clock signals to control the amplification and reset of the comparator.
The two clock signals are about 180 degree phase difference as shown in Fig. 5.19. The small time space between amplification and reset period is to give the bipolar regeneration stage more time to amplify the signal so as to reduce the delay. After being amplified by the bipolar regeneration stage, the signal is sent to a CMOS regeneration stage to amplify the signal to CMOS logic level. The latch then changes the return-to-zero signal to non-return-to-zero signal. During reset, transistor M1 turns on and force the voltage levels in the two sides to be equal. The next amplification cycle can start after reset by turning off M1. To reduce the offset, the layout of the comparator should be drawn as symmetrically as possible. Fig. 5.20 shows the Hspice simulation results of the comparator.
5.6.4. Buffer

Fig. 5.21 shows the buffer which includes handshaking circuit and a big inverter. Since the short circuit current in the output buffer causes large power loss, a handshaking circuit is needed to ensure PMOS and NMOS will not turn on at the same time. Fig. 5.22 is the Hspice simulation results which show that PMOS will be closed before NMOS is turned on and vice versa. To compromise for the delay, signal is fed back from earlier stage.
5.6.5. NOR & NAND Gate

Nor and nand gates, shown in Fig. 5.23 and Fig. 5.24, are used in the handshaking circuit of the buffer. BiCMOS gates are used here to reduce the delay. Although their power dissipation are large, the power-delay product is better than CMOS gates. The major disadvantage of BiCMOS gates is that they cannot give full swing output signal. Consider the nor gate in Fig. 5.23. The Vbe voltage of the bipolar transistor will drop to zero and pre-
vent the output voltage from reaching Vdd when the output signal approaches Vdd. Therefore, a feedback loop is used here to turn on the transistor M1 when output signal is large enough. The same is for pull down circuit where transistor M2 is turned on to pull down the output signal to ground. The operation of nand gate is the same as nor gate.

**FIGURE 5.24. BICMOS NAND gate**

![BiCMOS NAND gate diagram](image)

### 5.6.6. The Size of Buffer

The buffer size determines the loop delay and the power efficiency of the converter. The power loss of the output buffer includes the gate driving power loss and the turn-on resistance power loss. In the beginning, it is assumed that the delay and efficiency cannot be optimized at the same time. However, it is surprising to find that the two parameters can almost be optimized at the same time after simulation.

To optimize the buffer size, two variables are set. They are Wd and K as shown in Fig. 5.25. For equal rising time and falling time, the PMOS width is equal to two times of NMOS width. Also, to reduce the delay, all transistors are set to minimum length.
In optimizing the buffer size, the delay requirement is met first. The delay in the loop
includes the buffer delay, comparator delay and other circuits delay. The total delay should be less than 3 ns as shown in previous section. Within the 3 ns delay, 2 ns delay is given to the buffer and 1 ns delay is given to comparator and other circuits. Fig. 5.26 illustrates the buffer delay with different Wds and Ks. It shows that the delay decreases when the buffer size reduces. Fig. 5.27 shows the power efficiency varying Wds and Ks. When Wd is from 10000 µm to 20000 µm and K is from 5 to 10, the power efficiency is maximized. From Fig. 5.26, the range of Wd and K which gives the buffer delay of less than 2 ns is known. The Wds and Ks in this range in Fig. 5.27 are then optimized for power efficiency by filtering out the Wds and Ks which do not meet the delay requirements (> 2 ns). The result is shown in Fig. 5.28. From this graph, Wd and K are chosen to give the maximum power efficiency. Therefore, the sizes of the buffers are got as

\[(W/L)_{M1} = 12000\mu m/0.8\mu m; (W/L)_{M2} = 6000\mu m/0.8\mu m; (W/L)_{M3} = 1600\mu m/0.8\mu m\]

\[(W/L)_{M4} = 800\mu m/0.8\mu m; (W/L)_{M5} = 800\mu m/0.8\mu m; (W/L)_{M6} = 400\mu m/0.8\mu m\]

From Fig. 5.26 and Fig. 5.27, we can see that the delay and efficiency can almost be optimized at the same time. And this is a good news to the design.

5.7 Performance

After finishing the circuit design, the performance of the converter is measured. Fig. 5.29 shows the power efficiency with different input signal frequencies and output power levels. It is definitely that the efficiency decreases when the output power level decreases. And the reason that the efficiency decreases when the input signal frequency increases will be given in Chapter 6. Fig. 5.30 and Fig. 5.31 show the whole circuit and layout of the
power converter. The post layout simulation in Fig. 5.32 indicates that the signal to distortion ratio is larger than 55 dB.

**FIGURE 5.28. Power efficiency optimization**

![Efficiency V.S. Size of Trans.](image)

Filter out delay > 2 ns

![Efficiency within 2ns delay](image)
FIGURE 5.29. Power efficiency with different output power levels and input signal frequencies

FIGURE 5.30. The whole circuit of the power converter

FIGURE 5.31. Layout
5.8 Summary

A DC-DC power converter with 5 MHz bandwidth has been designed. The maximum power efficiency can go up to more than 80%. The output voltage ranges from 0.2V to 4.7 V and the output power is larger than 1 watt. The total die area is about 1.2 mm$^2$. There are only two external components which are the capacitor and the inductor in the low-pass filter. The values are about 10 nF and 200 nH respectively. The power converter is designed and fabricated using AMS 0.8 µm BiCMOS technology.
6.1 Introduction

In this chapter, the measurement results of each individual block of the circuit are shown. The implementation of the E.E.R. power amplifier is done by using the power converter to control the Vdd of a commercial R.F. power amplifier. The explanations are provided for the deviation of the measurement results from the simulation.

6.2 Measurement Results

6.2.1 Input stage & Zero compensation

Fig. 6.1 and 6.2 are the amplitude and phase transfer curves of the input and zero compensation stages. Except for the gain, the amplitude transfer curve is well-matched to the simulation result. The gain is lower than simulation for the fact that the output loading is only 50 ohms (the input impedance of the network analyzer.). The buffer is unable to drive the signal with such a low loading output to the expected swing. Compare to the amplitude transfer curve, the phase transfer curve deviates more from simulation. The reason is that the parasitic capacitors from pads and PCB layout cause extra phase shift.
6.2.2 Comparator

Two input signals with 50 MHz (amplitude of 10 mv) and 100 MHz (amplitude is also 10 mv) sine waves are used to test the comparator. Fig. 6.3, Fig. 6.4 and Fig. 6.5 show the output signals of the two inputs and the clock signal respectively. The outputs are squarewaves with the magnitude of Vdd. Due to the attenuation of the high impedance probe, the squarewaves are 20 dB lower than the actual magnitude. As the comparator is controlled by 500 MHz sampling clock, the delay of the comparator should be about 1 ns. However, since there is only a little space in the probe station, a long cable is used to connect the output to the measurement equipment and also the input cables are different length. Therefore, the measured delay of the comparator is larger than the expectation.
FIGURE 6.3. Comparator output with 10 mv and 50 MHz sine wave.

FIGURE 6.4. Comparator output with 10 mv and 50 MHz sine wave.

FIGURE 6.5. Clock signal spectrum.
6.2.3 Handshaking circuits

Fig. 6.6 shows the gate inputs of PMOS and NMOS of the output buffer. The graph is zoom in as in Fig. 6.7 to show the handshaking function more clearly. However, the rising time and falling time are quite large. So the handshaking function is not clearly shown. The low falling and rising slope is due to the limited bandwidth of the scope and the fact that the buffer is constructed using a long train of transistor fingers. The output signals are attenuated 20 dB by the high impedance probe also. The actual amplitude of the signal should be Vdd (3.3 volts).
6.2.4 Power converter

The power converter is tested using three sine wave input signals with 0.5 MHz, 3.5 MHz and 5 MHz respectively. Fig. 6.8 is the power converter test setup. Since input signal to the spectrum analyzer should exclude DC component, a 30 pF capacitor is used to block the DC signal. While the 1 KΩ resistor is to isolate the spectrum analyzer from 12 Ω loading of the power converter. Therefore, instead of the actual signal magnitude, the measured signal amplitude in the spectrum analyzer is attenuated by the 30 pF capacitor and 1 KΩ resistor. The output signal spectrums are shown in Fig. 6.9a, Fig. 6.9b and Fig. 6.9c.

FIGURE 6.8. Power converter measurement setup.

FIGURE 6.9. Output spectrum with input frequency (a) 0.5 MHz; (b) 3.5 MHz; (c) 5 MHz
The measurement harmonic distortion is about -35 dBc. Compared to the simulation result shown in Fig. 5.33, the performance is degraded by about 20 dB. There are two reasons cause the degradation. The first reason is the signal delay. Chapter 5 indicates that when the delay is larger than 4 ns, the linearity performance will degrade rapidly. The extra delay comes from: a) the parasitic capacitance of the large area metal in the output buffer, the pads and the PCB. b) the structure of PMOS and NMOS in output buffer is a long train of transistor fingers. c) the resistance of the metal. d) the delay of the feedback path in the PCB line. The second reason of the performance degradation is due to the parasitics of the capacitor and inductor in the external low pass filter. Fig. 6.11 shows the low pass filter with parasitics. Fig. 6.10 shows the output signal spectrum with ideal block sim-
ulation. Fig 6.12 is the simulated output spectrum with the same ideal function blocks used in Fig. 6.10 except that the low pass filter in Fig. 6.11 is used instead. The results show that the parasitics in the low pass filter degrade the performance by about 15 dB.

The inductor and capacitor model of the low pass filter shown in Fig. 6.11 are extracted from HP Impedence Analyzer. The above simulation results show that the linearity performance of the power converter is very much affected by the parasitics of the external low pass filter. Simulation also shows that the linearity degradation caused by the parasitics can be reduced by tuning the inductor and capacitor values. However the practical model of the low pass filter (includes the parasitics from the PCB) is very complex and difficult to be extracted. In practice, the only way to tune the inductor and capacitor is by trial and error. However, it takes a lot of time and requires a sequence of different values of inductors and capacitors.
Fig. 6.13 compares the power efficiency from simulation, calculation, measurement and estimation. All curves show that the power efficiency decreases as input signal frequency increases. The reason for this trend is explained in next page. The measured power efficiency deviates more from both the calculation and simulation results as the input frequency increases. This is due to other sources of parasitic resistances and capacitances such as the metal layers, bond wires and PCB. The parasitic resistance estimation curve is to estimate the total parasitic resistance through calculation using the formula in the next page. A value of 1.8 $\Omega$ is chosen so the curve fits the measurement results. Therefore, excluding 0.9 $\Omega$ turn-on resistance (see next page), the parasitic resistance is 0.9 $\Omega$.
The efficiency of the power converter is determined by the output stage since most power is consumed here. Fig. 6.14 is a symbolic output stage with the transistors modeled as a turn-on resistor in series with an ideal switch. The power efficiency is calculated as:

\[
\text{power efficiency} = \frac{\text{output power}}{(\text{output power} + \text{power dissipation})}
\]

where

\[
\text{output power} = \frac{V_o^2}{2R} + \frac{K^2}{R}
\]

\[
\text{power dissipation} = \text{turn-on power} + \text{dynamic power} + \text{short circuit power}
\]

(EQ 6.1)

The turn-on power is the power loss in the turn-on resistance of the buffer transistors. And the turn-on resistance is equal to

\[
R_{on} = \frac{V_{DD}}{\frac{K_p W}{2 L} (V_{DD} - V_{th})^2}
\]

(EQ 6.2)

For simplicity, we take the total turn-on resistance as the average of pmos and nmos turn-on resistances: \(R_{on} = \frac{(R_{onp} + R_{onn})}{2}\). For pmos, the size is 12000 \(\mu\)m / 0.8 \(\mu\)m and \(K_p = 100 \times 10^{-6}\); while for nmos, the size is 6000 \(\mu\)m / 0.8 \(\mu\)m and \(K_p = 35 \times 10^{-6}\). The threshold voltages for pmos and nmos are 0.7V and -0.7V respectively. Vdd is 5 V. Thus the average turn-on resistance is 0.9 \(\Omega\). The current flows through the turn-on resistance \(R_{on}\) is calculated as:

\[
I_{tot} = I_c + I_o
\]

\[
= C_d \frac{d}{dt} (V_o \sin \omega t + K) + (V_o \sin \omega t + K)/R
\]

\[
= CV_o \alpha \cos \omega t + (V_o \sin \omega t + K)/R
\]

(EQ 6.3)

Therefore, the turn-on resistance power loss is equal to:

\[
P_{R_{on}} = \frac{1}{T} \int_0^T (I_{tot} R_{on}) dt
\]

\[
= \frac{1}{T} \int_0^T (CV_o \alpha \cos \omega t + (V_o \sin \omega t + K)/R)^2 R_{on} dt
\]

\[
= \left( \frac{(CV_o \alpha)^2}{2} + \frac{1}{2} \left( \frac{V_o}{R} \right)^2 + \left( \frac{K}{R} \right)^2 \right) R_{on}
\]

(EQ 6.4)
And the dynamic power loss is:

$$P_{dyn} = CV_{dd}^2f_{sw}$$  \(\text{(EQ 6.5)}\)

where $f_{sw}$ is the buffer input switching frequency. Assume the handshaking function reduce the short circuit current power loss to zero, then the power efficiency is given as:

$$\eta = \frac{\left(\frac{V_o^2}{2R} + \frac{K^2}{R}\right)}{\left(\frac{(CV_o\omega)^2}{2} + \frac{1}{2}\frac{V_o^2}{R} + \frac{K^2}{R}\right)R_{on} + CV_{dd}^2f_{sw} + \left(\frac{V_o^2}{2R} + \frac{K^2}{R}\right)}$$  \(\text{(EQ 6.6)}\)

Assume the buffer input switching frequency is 50 MHz (see last chapter) and the parasitic capacitance is 30 pF in the buffer only. $V_o$ and $K$ are both equal to 2.4 volts. Then the results of the calculation is plotted in Fig. 6.13. From equation (6.6), it shows clearly that the efficiency is in opposite proportion to the square of the output signal frequency.

### 6.2.5 R.F. power amplifier

The RF power amplifier (ITT2206GJ) is a commercial product from GaAsTek. It is designed for use in 3.6 V DECT handsets with power added efficiency of more than 57% in the frequency band of 1.8 GHz to 2 GHz. Fig. 6.15 shows the implementation of the RF power amplifier. Fig. 6.16 is the measured performance of the power amplifier with different supply voltages. Fig. 6.17 shows the output signal amplitude at 50 ohms output loading when the supply voltage varies. The signal amplitude is calculated as $V_M = P_v \times 2 \times 50$. The deviation from linearity is due to the power loss in the matching network.

To see what is the linearity performance of using this RF PA in EER technique, a 5 MHz sine wave is generated from signal generator to control the Vdd of the PA, the output signal spectrum is measured and shown in Fig. 6.18. It demonstrates that the output signal is perfectly modulated by the Vdd signal and no harmonic distortion is produced. There-
Therefore, the RF power amplifier is a good choice to be used in E.E.R. linearization technique.

**FIGURE 6.15.** RF power amplifier circuit.

**FIGURE 6.16.** Output power and efficiency with different supply voltages.

**FIGURE 6.17.** Output signal amplitude with different supply voltages.
6.3 EER P.A. implementation

The EER power amplifier is implemented by using the power converter to control the supply voltage of the R.F. P.A.. Fig. 6.19 shows the measurement setup of the E.E.R. power amplifier. The input impedance in the Vdd terminal is calculated by dividing the supply voltage with supply current. The resulting impedance value is about 12 ohms. Fig. 6.20 shows the output signal spectrums using 1MHz, 3MHz and 5MHz sine waves for power converter inputs. The maximum distortion is less than -30 dBc which is higher than the results when the power converter is measured in stand alone (see Fig. 6.9). The reason is that the input impedance at RF PA voltage supply terminal is not only a pure resistor but also includes parasitic capacitance and inductance. The complexed input impedance makes the measurement results deviate more from the simulation.

**FIGURE 6.18. Output spectrum by direct modulation of Vdd using signal generator.**

**FIGURE 6.19. E.E.R. P.A. measurement setup.**
FIGURE 6.20. E.E.R. P.A. output spectrum with control signal freq. (a) 1MHz; (b) 3MHz; (c) 5MHz

For comparison, a 40 KHz AM signal (a maximum AM bandwidth for signal generator) is directly input to the RF P.A. The output signal frequency spectrum is given in Fig. 6.21. There are more harmonic distortions than the results when EER linearization technique is used. The conclusion is that the EER technique successfully linearize the RF PA.

FIGURE 6.21. R.F. P.A. output frequency spectrum by directly input an 20 KHz AM signal.

The power added efficiencies of EER P.A. and the R.F. power amplifier with different
output power levels are compared in Fig. 6.22. The input signal to the RF PA is 40 KHz AM signal. While, for the EER PA, the inputs are 6 MHz and 2 MHz bandwidth AM signal respectively. At high power region, the RF power amplifier is already saturated and cannot be used as a linear power amplifier. Except for this region, the EER power amplifier gives higher power efficiency than the original RF power amplifier.


6.4 Performance comparison

Previously, two well-known EER PA were implemented. The first one was designed by F.H. Raab in 1994. The second one was by Davide Su in 1997. The following table compares the performance of the above two PAs with the one designed in this project.

<table>
<thead>
<tr>
<th>Project</th>
<th>Carrier frequency</th>
<th>R.F. signal bandwidth</th>
<th>Modulation signal</th>
<th>Max. distortion</th>
<th>Max. power efficiency</th>
</tr>
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<tr>
<td>F.H. Raab, Rupp 1994</td>
<td>3.5 MHz</td>
<td>20 KHz</td>
<td>Amplitude modulation</td>
<td>-34 dBC</td>
<td>60%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>60 KHz</td>
<td></td>
<td>-22.4 dBC</td>
<td></td>
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<tr>
<td>David Su, 1997 ISSCC</td>
<td>850 MHz</td>
<td>30 KHz</td>
<td>π/4 QPSK</td>
<td>-30 dBC</td>
<td>40% for 3.6 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>50% for 4.8 V</td>
</tr>
<tr>
<td>This project 2000</td>
<td>1.9 GHz</td>
<td>10 MHz (double side band)</td>
<td>Amplitude modulation</td>
<td>-30 dBC</td>
<td>48%</td>
</tr>
</tbody>
</table>
Since the E.E.R. P.A. in this project is tested using simple AM signal, the linearity and power efficiency does not accurately represent the real performance of the PA when modulation signal like OFDM is applied. The performance may be worse when modulation signal is applied.
7.1 Introduction

After finishing the measurement, we find that there are improvements which can be made to increase the linearity performance and power efficiency. The following sections give brief introduction on power efficiency and linearity improvement by using circuit techniques and more advanced process.

7.2 Power efficiency improvement

7.2.1 Advanced process and larger buffer size

The power loss in the power converter is mainly through the parasitic resistance, the short circuit current and the dynamic power loss. From chapter 6, it is known that the average turn-on resistance of the output buffer is 0.9 Ω. Therefore, one tenth of the power is loss through turn-on resistor as the output loading is only about 12 Ω. It is clear that larger buffer size can reduce the turn-on resistance power loss. However, as mentioned in chapter 5, the buffer size is limited by the total signal delay requirement (Larger delay causes larger distortion). But from measurement results, we find that the linearity of the
power converter is dominated by the parasitic effects in the external low pass filter instead of the signal delay. Thus, we can increase the buffer size for the benefit of the power efficiency, and at the same time, little degradation is caused on the linearity performance. However, increasing the buffer will increase the dynamic power loss. So there exists trade-off on dynamic power loss and turn-on resistor power loss.

The power converter was fabricated by 0.8 \( \mu \text{m} \) process with only two metal layers. The resulted huge capacitors cause higher signal delay and dynamic power loss. Reducing the parasitic capacitor by using more advanced process (like 0.25 \( \mu \text{m} \) process) will certainly increase the over-all performance of the power converter.

![FIGURE 7.1. Number of switching cycles with different clock frequencies.](image)

### 6.2.2 Smaller the clock frequency

The comparator is controlled by 500 MHz clock frequency. From Fig. 5.12, the clock frequency is chosen for optimum linearity performance. However, as shown in Fig. 6.12, the linearity of the power converter is limited by the parasitics of the external inductor and capacitor. Therefore, if a smaller clock frequency is chosen, the linearity is not much degraded. But, from Fig. 7.1, the number of switching per second in the output buffer is reduced as the clock frequency decreases. The dynamic power loss is proportional to the
switching frequency and the capacitor. The parasitic capacitance in the output buffer is more than 50 pF (30 pF from the two transistors and 20 pF from the metal layers). If the switching frequency is 50 MHz, the dynamic power loss is about 63 mW. Therefore, reducing the clock frequency can increase the total power efficiency.

7.3 Linearity

The harmonic distortion of -30 dBc just meets the marginal requirement. To increase the linearity, the envelope feedback as mentioned in chapter 4 can be added into the power converter. The envelope feedback not only increase the linearity but also reduce the envelope and phase signal time mismatch effects.
REFERENCES


References


[29] AMS 0.8um BiCMOS process documents
Appendix A: Photographs of the chips

The Switched mode power converter

Input stage & zero compensation.

Comparator

Clock

Driver, Handshaking and Output buffer
Appendix B: GaAsTek RF Power Amplifier

3.6V 0.5W RF Power Amplifier IC for DECT
ITT2206GJ

TYPICAL CHARACTERISTICS (Measured data from process nominal devices)

Figure 1. Maximum operating temperature ($T_0$) to maintain <150°C junction temperature.

Figure 2. Output power, power added efficiency, and input VSWR vs. frequency

Figure 3. Output power and power added efficiency vs. supply voltage

Figure 4. Harmonics

Specifications Subject to Change Without Notice

GaAsTEK
5310 Valley Park Drive
Roanoke, VA 24019 USA
www.gastaek.com
Tel: 1-540-563-3949
1-888-563-3949 (USA)
Fax: 1-540-563-8816
Appendix B: GaAsTek RF Power Amplifier

3.6V 0.5W RF Power Amplifier IC for DECT ITT2206GJ

**TYPICAL CHARACTERISTICS** (Measured data from process nominal devices)

**Figure 5.** Output power and drain current vs. temperature at $V_{DD}$=3.0V

**Figure 6.** Output power and drain current vs. temperature at $V_{DD}$=3.2V

**Figure 7.** Output power and drain current vs. temperature at $V_{DD}$=3.6V

Specifications Subject to Change Without Notice

GaAsTEK
5310 Valley Park Drive
Roanoke, VA 24019 USA
www.gastek.com
Tel: 1-540-563-3949
1-888-563-3949 (USA)
Fax: 1-540-563-8416

Power Amplifier Linearization for OFDM Signal
3.6V 0.5W RF Power Amplifier IC for DECT
ITT2206GJ

APPLICATION INFORMATION

Figure 8. Evaluation Board Schematic

Transmission Lines (Grounded Coplanar Waveguide)

List of components:
- C1 = 0.7 pF multilayer ceramic chip capacitor
- C2 = C3 = C4 = C6 = 100 pF multilayer ceramic chip capacitor
- C5 = 2.2 pF multilayer ceramic chip capacitor
- L1 = 2.7 nH chip inductor
- L2 = 3.3 nH chip inductor
- L3 = 27 nH chip inductor
- R1 = 300 Ω chip resistor
- 60 mil GETEK Board

Figure 9. Evaluation Board Layout

Figure 10. 50 Ω Lead Transition
### Technology Reference Guide

#### BiCMOS Technology Selection Guide

<table>
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<th>BYE</th>
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<td>0.66/0.75</td>
<td>0.66/0.75</td>
<td>1.0/1.1</td>
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<td>270/120</td>
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<td>Base Resistance [Ohm/µm]</td>
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<td>1100</td>
<td>500</td>
<td>1200</td>
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Appendix C: AMS 0.8 µm BiCMOS process

Data Sheet

BYB / BYE 0.8µm BiCMOS Process

Schematic Cross Section (BYE)

Structural Process Characteristics

Core Process ......................................................................... 0.8 µm p-Epi Twinwell CMOS Process
Interconnect Layer ........................................................................... 2 unrestricted Metal Layers
Capacitor Structures / BYE .............................................................. Second Poly Layer for Linear Poly/Poly Capacitors
Capacitor Structures / BYB .............................................................. Poly over Sinker Capacitors
Bipolar Transistors ......................................................................... Vertical NPN / Lateral PNP Poly Emitter / Deep Collector Structure
Buried Layer ................................................................................ N+, p+
Doping .......................................................................................... NLDD&PLDD
Isolation Method ............................................................................ Semi Recessed Oxide Isolation
Drawn / Effective Channel Length ....................................................... 0.8 / 0.65 µm
Gate Oxide Thickness ..................................................................... 16 nm
Field Oxide Thickness ................................................................... 550 nm
n+, p+ Junction Depth .................................................................. 0.4 µm
Epitaxial Layer Thickness ............................................................... 1.4 µm
Well Junction Depth ...................................................................... 0.8 µm
Metal 1 / 2 Pitch ........................................................................... 2.4 / 2.8 µm
Poly Pitch 1 / 2 ............................................................................ 1.8 / 3.4 µm
Isolation Pitch ................................................................................ 7 µm
Min Emitter Size ........................................................................... 3 x 0.8 µm
Min. Active Area Bipolar ............................................................... 11.8 x 9.0 µm
Mask Levels .................................................................................. 15 BYB / 16 BYE

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Power Amplifier Linearization for OFDM Signal 90
OFDM MODULATION

function d=ofdm1()

% simulation parameters
clear
N=1024
dt=0.5
st=0.5
m1=N
l=8
p=1
fc=0
block=6
m = st/dt;
fn =1/(N*st);
intrlef=64

fid=fopen('/afs/ee.ust.hk/staff/ee/eelwf/eesof/rfpa2_prj/data/bindata6.dat','r');
datain=fscanf(fid,'%g',[1,inf]);
status=fclose(fid);

% convolution coing
for n=1:2,
    for b=1:block,
        r=zeros([1,6]);
y=1;
for i=1:2*N,
    bind(1)=datain((b-1)*N*4+y);
    bind(2)=datain((b-1)*N*4+y+1);y=y+2;
    o(1)=xor(xor(xor(bind(2),r(2)),xor(r(3),r(4))),r(5));
    o(2)=xor(xor(xor(xor(bind(1),r(1)),xor(r(3),r(4))),r(6));
    decout((b-1)*N*6+(i-1)*3+1)=o(1);
    decout((b-1)*N*6+(i-1)*3+2)=o(2);
    decout((b-1)*N*6+(i-1)*3+3)=o(3);
    for shft=6:-1:3,
r(shft)=r(shft-2);
    end
    r(2)=bind(1);
    r(1)=bind(2);
end
end
% interleaving
for n=1:2,
    for b=1:block,
        for i=1:intrlef,
            for j=1:(6*N/intrlef),
                k=k+1;
            end
    end
end

% ofdm modulation
for a=1:(N+50)*p*block,
vout(2,a)=0;
vout1(2,a)=0;
end
for x=0:(block-1),
    for i=0:(p*(N+50)-1),
        for j=(-N/2):((N/2)-1),
        phase=0; % pi*(j^2)/N;
        vout(2,(N+50)*p*x+i+1)=vout(2,(N+50)*p*x+i+1)+(vin(1,x*N+j+N/2+1)*cos(2*pi*i*(fn*j+fc)*st/p+phase)+vin(2,x*N+j+N/2+1)*sin(2*pi*i*(fn*j+fc)*st/p+phase))/N;
        vout1(2,(N+50)*p*x+i+1)=vout1(2,(N+50)*p*x+i+1)+(vout(1,x*N+j+N/2+1)*cos(2*pi*i*(fn*j+fc)*st/p+phase)+vout(2,x*N+j+N/2+1)*sin(2*pi*i*(fn*j+fc)*st/p+phase))/N;
        end
    end
end

% clear data and status
clear datain;
clear decout;
fid=fopen('../eesof/rfpa2_prj/data/qamdata6.dat','w');
fprintf(fid,'%3.5f   %3.5f
',vin);
status=fclose(fid);

% fid=fopen('../eesof/rfpa2_prj/data/qamdata.dat','w');
% fprintf(fid,'%3.5f   %3.5f
',vin);
% status=fclose(fid);
% fid=fopen('/afs/ee.ust.hk/staff/ee/eelwf/eesof/rfpa2_prj/data/qamdata.tim','r');
% vin=fscanf(fid,'%g',[2,inf]);
% status=fclose(fid);
% fid=fopen('/afs/ee.ust.hk/staff/ee/eelwf/eesof/rfpa2_prj/data/qamdata.tim','r');
% vin=fscanf(fid,'%g',[2,inf]);
% status=fclose(fid);

for a=1:(N+50)*p*block,
vout(2,a)=0;
vout1(2,a)=0;
end

% sqrt(N) matrix initialization
k=1
for i=1:6:6*N*block-5,
    bd(1,1)=bind(i);
    bd(2,1)=bind(i+1);
    bd(1,2)=bind(i+2);
    bd(2,2)=bind(i+3);
    bd(1,3)=bind(i+4);
    bd(2,3)=bind(i+5);
    dec=bd(1,1)+bd(1,2)*2+bd(1,3)*4;
    vin(1,1)=bin2q(dec);
    dec=bd(2,1)+bd(2,2)*2+bd(2,3)*4;
    vin(2,1)=bin2q(dec);
    k=k+1;
end

% clear data and status
clear datain;
clear decout;
fid=fopen('../home/uman1/eelwf/datacn6.tim','w');
fprintf(fid,'BEGIN TIMELAG
');
fprintf(fid,'# T ( USEC V R 50.)
');
fprintf(fid,'%3.3f   %3.7f
',vout);
fprintf(fid,'END
');
status=fclose(fid);

fid=fopen('/home/uman1/eelwf/datasn6.tim','w');
fprintf(fid,'BEGIN TIMELAG
');
fprintf(fid,'%3.3f   %3.7f
',vout1);
fprintf(fid,'END
');
status=fclose(fid);
Appendix D: Matlab programmes

```
fprintf(fid,'# T ( USEC V R 50.)\n');
fprintf(fid,'%3.3f %3.7f\n',vout1);
status=fclose(fid);

OFDM demodulation

function w=test() %%add new Phase%%
N=1024
block=2
fid=fopen('/afs/ee.ust.hk/staff/ee/eelwf/eesof/rfpa2_prj/data/outc.tim','r');
x=fscanf(fid,'%g',[2,inf]);
status=fclose(fid);
delay=1004
fid=fopen('/afs/ee.ust.hk/staff/ee/eelwf/eesof/rfpa2_prj/data/outs.tim','r');
y=fscanf(fid,'%g',[2,inf]);
status=fclose(fid);
for b=0:block-1,
    for n=(-N/2):((N/2)-1),
        i(2,b*N+n+N/2+1)=0;
        q(2,b*N+n+N/2+1)=0;
        if (n+N/2+b*N)<0.2,
            i(1,b*N+n+N/2+1)=(n+N/2+b*N)*0.2;
            q(1,b*N+n+N/2+1)=(n+N/2+b*N)*0.2;
        else
            phase=0;%pi*((n-1)^2)/N;
            for k=0:(N-1),
                i(2,b*N+n+N/2+1)=i(2,b*N+n+N/2+1)+((x(2,50*(k+b*(N+50))+delay)*cos(2*pi*k*n/N+phase)-y(2,50*(k+b*(N+50))+delay)*sin(2*pi*k*n/N+phase))/N);
                q(2,b*N+n+N/2+1)=q(2,b*N+n+N/2+1)+((y(2,50*(k+b*(N+50))+delay)*cos(2*pi*k*n/N+phase)+x(2,50*(k+b*(N+50))+delay)*sin(2*pi*k*n/N+phase))/N);
            end
        end
    end
end
fid=fopen('../eesof/rfpa2_prj/data/datai1.tim','w');
fprintf(fid,'BEGIN TIMEDA TA\n');
fprintf(fid,'# T ( USEC V R 50.)\n');
fprintf(fid,'%%  t   data\n');
fprintf(fid,'%3.5f   %3.5f\n',i);
fprintf(fid,'END\n');
status=fclose(fid);
 fid=fopen('../eesof/rfpa2_prj/data/dataq1.tim','w');
fprintf(fid,'BEGIN TIMEDA TA\n');
fprintf(fid,'# T ( USEC V R 50.)\n');
fprintf(fid,'%%  t   data\n');
fprintf(fid,'%3.5f   %3.5f\n',q);
fprintf(fid,'END\n');
status=fclose(fid);

Error Decoding

%function w=stameric

clear

fid=fopen('/afs/ee.ust.hk/staff/ee/eelwf/eesof/rfpa2_prj/data/datai1.tim');
x=fscanf(fid,'%g');
status=fclose(fid);

fid=fopen('/afs/ee.ust.hk/staff/ee/eelwf/eesof/rfpa2_prj/data/dataq1.tim');
y=fscanf(fid,'%g');
status=fclose(fid);
totalerr1=0;
errcnt=0;
```
Appendix D: Matlab programmes

Power Amplifier Linearization for OFDM Signal

for k=1:3,
  ind=ind+1;
  r(n,ind)=(ty/2-floor(ty/2))*2;
  ty=floor(ty/2);
end
end
end

%%%%%%%%%%% interleaving decoding

k=1;
for i=1:block*3*N,
  bd(k)=r(1,i);
  bd(k+1)=r(2,i);
  k=k+2;
end

k=1;
%for n=1:2,
for b=1:block,
  for i=1:6*N/intrlef,
    for j=1:intrlef,
      dintrdata(k)=bd((b-1)*6*N+(j-1)*6*N/intrlef+i);
      k=k+1;
    end
  end
  end
%end
A=[];

%%%%%%%%%%% convolution decoding

function [B] = NewVit(G,Z, k, C)
%B = NewVit(G, Z, k, C)
%  G is the generator matrix.
%    For "k/n" code with constraint length K, its size is [n, k*K].
%  Z is the input codeword.
%  k is the "k" of "k/n" code. Default is "1".
%  C is the number of states to be combined in the Trellis. Default 1.

G =[1 0 0 1 1 1 1 0;0 1 0 1 1 0 0 1;1 0 1 1 1 0 1 1];
% if nargin<3, k=1; end;
% if nargin<4, C=1; end;
% [n, K] = size(G);   K = K / k;
if isempty(find(Z(:)==0 & Z(:)==1)), Z=2*Z-1; end;
L = length(Z) / (n*C);
Z = reshape(Z, (n*C), L);
[out, next, prev] = NewTrel(G, C, k);
out = 2*out-1;   % map to +/- 1.

% Set Initial PM
PM0 = [0, -Inf*ones(1, 2^(k*(K-1))-1)];
% build the Path matrix
for i = 1 : L,
  for br = 1 : 2^(k*(K-1+C)),
    BM(br) = out(:,br)' * Z(:,i);
  end;
  for s = 1 : 2^(k*(K-1))         %% s: state.
    b1 = find(next==s);     %% b1: branches ends at
    state "s"
    s1 = prev(b1);          %% s1: starting states of
    branches b1
    [PM(s), ib] = max(PM0(s1)+BM(b1));
    Path(s, i) = b1(ib);
  end;
  PM0 = PM;
end;
MaxPM = find(PM==max(PM));
B(L) = MaxPM(1);        % choose the first one if there are
                       % a few, or can just
                       % use the "0" state if tail bits are utilized.
if MaxPM ~= 1, disp(sprintf(’warning: MaxPathMetric=state#%d
’, MaxPM)); end;
B(L) = 1;
for i = L:-1:2,
  B(i-1) = prev(Path(B(i), i));
end;

MaxPM = find(PM==max(PM));
B(L) = MaxPM(1);        % choose the first one if there are
                       % a few, or can just
                       % use the "0" state if tail bits are utilized.
if MaxPM ~= 1, disp(sprintf(’warning: MaxPathMetric=state#%d
’, MaxPM)); end;
B(L) = 1;

fid=fopen('/afs/ee.ust.hk/staff/ee/eelwf/eesof/rfpa2_prj/ data/bindata63.dat','r');
orgdata=fscanf(fid,'%g',[1,inf]);
status=fclose(fid);
n1=0;n2=0;
errcnt=0;
%for n=1:2;
for i=1:block*4*N,
  if orgdata(i)==datao(i),
    errcnt=errcnt+1;q(errcnt)=i;
  end
end
%end
errcnt

Viterbi decoding