CMOS Radio Frequency Integrated Circuit Design for Direct Conversion Receivers

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by

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ABSTRACT

The semiconductor industry continues to challenge analog and RFIC designers with a demand for higher performance and better compatibility with the digital world. It is desirable to use a single mainstream digital CMOS process for all IC products, especially for a system on a single chip. To achieve the highest integration, direct conversion for the analogue part is the most expedient candidate of all architectures because of its simplicity, and image-free and low power operation. However, the design of CMOS direct-conversion transceivers entails many difficulties: self-mixing induced DC offset, flicker noise, even-order distortion, I/Q mismatch, substrate noise, and so on. The aim in my research was to study these issues and to implement a prototype of direct-conversion receivers with the proposed solutions.

On-chip crosstalk and substrate noise were studied firstly through simulations. It is shown that physical separation is pointless if no shielding schemes are adopted. Some effective shielding methods to reduce the crosstalk are proposed. Shielding achieved a 20~40dB improvement on crosstalk. The flicker noise under switching conditions was studied experimentally for the first time. Methods to reduce flicker noise are discussed. The proposed simple noise model makes it possible to predict and optimize the circuit flicker noise performance. The severe self-mixing induced DC offset problem is circumvented completely by a proposed CMOS harmonic mixing technique. Two kinds of harmonic mixers in a CMOS process were designed and fabricated. The CMOS harmonic mixer achieved a 44dB DC-offset lower than do conventional mixers. Based on the harmonic mixing technique, the lateral bipolar mixer suppresses the flicker noise successfully and achieves less than 18dB noise figure at 10kHz frequency. They are totally DC offset free and suitable for direct-conversion receivers. Finally, a fully-integrated CMOS direct conversion pager receiver is demonstrated for the first time.
To My Dear Family
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CHAPTER 1
Introduction

The revolutionary advances in solid-state devices and integrated circuits (ICs) has brought the world of wireless communications into a completely new era. System-on-chip (SOC) is no longer a dream. New technologies acting as a driving force have pushed the personal wireless communications market into today’s boom. The market motivates low-cost low-power high performance circuit designs. To meet these requirements, communication system considerations, receiver/transceiver architecture innovations play a most essential role. Direct conversion is a very promising architecture for high integration. However, some severe drawbacks prevent its wide use. In this dissertation, we discuss about the design issues and provide possible solutions.

1.1 Direct Conversion Receivers

Since its introduction, the superheterodyne system has been adopted in virtually every radio receiver. The idea of down-converting the interested spectrum to one or more intermediate frequencies (IFs) makes it possible to process the signal under well-controlled conditions. High selectivity is achieved by inserting high quality filters at each IF strip. With the need to suppress the image, an image-rejection filter is required at the radio frequency (RF) front-end.
The amount of image being rejected depends on the first IF frequency. Therefore, conventional superheterodyne receivers have to work at a relatively high IF. As a result, in addition to the RF image-rejection filter, high quality band-pass IF filters must be used for an acceptable selectivity. As the transfer characteristics of these filters are usually well beyond the capability of today’s IC technology, discrete passive devices have become the most common choice. On the positive side, the performance is guaranteed. On the negative side, however, the drawbacks are higher cost, a lower integration level, and higher power consumption.

These points become very unfavorable when price and size are issues. A lot of effort has been expended seeking an alternative or modified architecture to the conventional one so that the requirements of the image-rejection and IF filters can be relaxed. The ultimate goal is to completely eliminate these off-chip filters. The RF filter may be realized in some applications in its simplest form by utilizing the band-pass properties of the antenna and the low-noise amplifier (LNA) without the burden of the image-rejection specification. The IF filters should be replaced by their integrated counterparts.

Several receiver architectures have been developed to implement the idea. Each has its advantages and disadvantages. Low-IF and direct-conversion (or zero-IF) are the two most well-known.

The low-IF solution is based on the fact that, theoretically, the image frequency can be removed using a specially designed mixer (the image-rejection mixer). This allows the IF frequency to be lowered to enable the use of monolithic filters. The problem associated with this type of architectures is the limited image rejection ratio which is due to the mismatch in the image-rejection mixer.

Direct-conversion is believed to be the most simple and straightforward way to build a radio receiver. By converting the RF signal directly to the base band, the image frequency no
longer exists. The benefits are obvious: no circuitry is needed to do the task of image-rejection. IF filtering could be performed by low pass filters (LPFs) in the form of Gm-C or switched-capacitor (SC). Nevertheless, the idea did not seem to be very useful in practical applications until the 1980’s when it proved its value in the POCSAG radio paging receiver [1][2].

The merits and drawbacks of direct-conversion have been investigated intensively since its success. Common design issues and their possible solutions have been identified and summarized [3][4]. The biggest concern is known to be the DC offset related problem. Undesired DC components originate mainly from two different mechanisms: self-mixing and even order distortion. In a fully balanced design, the latter is a result of device mismatch. When referred to the output of the mixer, the offset level can easily reach the order of 10 mV. This is more than enough to corrupt the weak signals (10 to 100 µV) and saturate the following stages. To avoid this scenario, some kind of offset-cancellation strategy is necessary. In the pager example, AC-coupling capacitors are used to block the DC offset. Receivers working in the time-division multiple access (TDMA) system can make use of the idle time slot to measure the offset and perform the cancellation in the coming operation mode.

DC offset is not the only problem. Trouble also comes from flicker or 1/f noise which is found in all active and some passive devices, especially those in the CMOS technology. Just like the offset, flicker noise can dominate weak signals before enough amplification is provided. Device size and bias conditions affect the flicker noise spectral density level and, thus, should be tuned when necessary. More advanced techniques such as chopper stabilization and correlated double sampling (CDS) are very effective in reducing offset and low-frequency noise at the price of increased complexity, higher power consumption, and larger thermal noise.

Other things like the local frequency (LO) leakage must also be treated carefully but DC
offset and flicker noise are the main barriers which limit the direct-conversion to only a few types of practical applications.

1.2 Contributions

Different kinds of issues in regard to direct conversion receivers were studied in my research. Using proposed solutions, a pager receiver was demonstrated. The main contributions include:

- On-chip crosstalk was studied and several shielding schemes are proposed. An improvement of more than 20 dB improvement was achieved.

- Flicker noise under switching condition was investigated experimentally and a simple noise model is proposed. The model makes circuit noise optimization possible without any measurement.

- Harmonic mixing principle has been proposed to solve self-mixing induced DC offset successfully. A CMOS harmonic mixer was fabricated and it provides more than 44dB DC offset suppression over conventional mixers.

- Lateral bipolar transistor is used to improve the flicker noise performance of harmonic mixer. A flicker-noise-free and DC-offset-free harmonic mixer was designed and fabricated. Less than 18dB noise figure at as low as 10kHz was achieved. The input-referred second order intercept (IIP2) improvement will be discussed.

- A fully-integrated pager receiver which uses CMOS direct conversion architecture was demonstrated successfully for the first time. The external components were minimized. A low-cost low-power system-on-chip (SOC) is possible.
1.3 Thesis Layout

In Chapter 1, a brief introduction to direct-conversion issues is given. Crosstalk and substrate noise are discussed in Chapter 2. Flicker noise under switching conditions is explored in Chapter 3. The DC offset problem is discussed in the following chapter. The CMOS harmonic mixer and lateral bipolar (LBJT) harmonic mixer are both described in Chapter 5 and Chapter 6. In Chapter 7 the fully-integrated pager receiver is presented. Future work, and the conclusion are given finally.
CHAPTER 2

On-Chip Crosstalk and Substrate Noise

With higher levels of integration, or even system on chip (SOC), the importance of limiting undesirable interactions between different circuits fabricated on a common Si substrate is increasing. Such interaction, referred to as cross-talk, is more problematic in mixed-mode (analog-digital) integrated circuits.

In this chapter, we first present an analysis of the electromagnetic interferences in silicon RFICs that can be an impediment to achieve higher integration. In the analysis, we (1) compare the effectiveness of four shielding solutions in a triple layer metal technology, (2) contrast the interference on both heavily doped and lightly doped substrates, and (3) study the impact of physical separation and geometrical variations. After studying electromagnetic coupling, substrate noise and its prevention approaches are discussed.

2.1 Introduction

On-chip crosstalk is an important issue in RF circuit integration. It leads to signal leakage, crosstalk, phase error, DC offset, phase noise, signal blocking, and so on. For example, in the direct-conversion mixer, crosstalk between the local oscillator (LO) and RF input introduces a severe DC offset problem which prevents the practical use of direct conversion architecture.
Differential circuitry would help, but is limited by device mismatch, small common-mode rejection ratio (CMRR) at high frequencies, and increased power consumption and noise.

Crosstalk, according to its source, can be divided into two types. The first is electromagnetic interference, which is introduced by passive coupling above the substrate, such as line-to-line crosstalk. The second is substrate noise which is introduced by active device, junction capacitor, and resistive substrate network. At a lower frequency range, the substrate noise is dominant. When the frequency rises, electromagnetic interference becomes more and more important, especially for advanced submicron technology in which the thickness of the metal even can be larger than the metal width.

The mutual coupling between lines becomes comparable to or even more dominant than, substrate noise at higher frequencies. A considerable energy flow takes place through the mutual coupling, the oxide and even through the package. The quasi-TEM model is not very accurate any longer. A full-wave analysis is necessary. Three options are normally available to RF PCB layout designers to minimize interference: (a) ground shield, (b) separation by distance, and (c) a metallic shield box. The integration of RF components has dramatically lessened the effectiveness of these options. As integration technology improves, more and more metal layers will be available in integrated circuits. It is possible to shield a circuit block inside RFICs. However, no research has been done in this area [5].

On the other hand, substrate noise has been studied for almost a decade [6]-[16]. Both heavily doped bulk [7] and lightly doped bulk [10] were investigated. Inductor induced substrate noise was reported in [11]. Different techniques have been applied in order to reduce the substrate noise ranging from the advanced SOI process, guard rings [8], or novel circuit design approaches [13]-[15]. These techniques have been discussed in detail individually but a general overview is not available. In the second part of this chapter, we will analyze the source of
the substrate noise, the effect on the circuit performance, and will study some shielding schemes. Finally, guidelines to reduce the substrate noise are proposed.

2.2 On-Chip Electromagnetic Crosstalk

Interference in a radio-frequency printed circuit board (RFPCB) is less problematic than that in RFICs because of two reasons: (1) There are more metal layers implemented in an RFPCB. State of the art silicon-based ICs offer three to seven layers of metals; double of that can be found in the PCB layout. Shielding in PCB is more practical. (2) Ground planes in PCBs are relatively closer to the signal layer compared to the separation distance, and it is more efficient in reducing crosstalk. The simple model of crosstalk between signal lines in an RFPCB at low frequencies is shown in Figure 2.1. Here $C_{ox}$ stands for the dielectric capacitor in the RFPCB instead of the oxide capacitor in the RFIC. $C_m$ is the mutual capacitor between two signal lines.

A normal RFPCB is simulated with a full wave analyzer – Sonnet [17]. The results are shown in Figure 2.2 and are compared with the analytical formula in [18]. The mutual capacitance $C_m$ between two signal lines, a dominant factor in the crosstalk, is proportional to $\ln(1+(2h/d)^2)$. The crosstalk is less than -50dB if $h/d$ is less than a quarter. It increases very
sharply with the ratio of $h/d$ when $h/d$ is less than 0.5. If $h/d$ is more than 1.0, separation does not improve it greatly. Unfortunately, for an RFIC, this is the case. The effective $h/d$ ratio can be very large since the bulk layer is in the order of 500 $\mu$m thick while minimum metal line separation distance can be only microns away.

Moreover, the situation becomes more complicated in RFIC. The metal is lossy, the substrate is lossy, the fringing effect is worse when the technology is continuously scaling down, and the substrate network is too complicated to model. Therefore, a full-wave electromagnetic analysis is necessary to gain an understanding of the crosstalk in RFIC.

### 2.2.1 Simulation Setup

Sonnet software was used to study near-end and far-end crosstalk in RFICs. Two kinds of substrates are usually used in both digital and analog integrated circuit design, heavily doped bulk, and lightly doped bulk. The cross sections are shown in Figure 2.3. In the early days, lightly doped bulk was widely used for digital circuit design. To prevent latch-up issues induced by parasitic bipolar devices in lightly doped bulk, heavily doped bulk was developed, and is now popular especially for analog circuit design since it provides better ground. It is

![Figure 2.2. Near end crosstalk S21 of RF PCB ($t=0.0028''$, $w=0.025''$, $L=0.4''$, $\varepsilon_r=4.5$, $f=300MHz$).](image)
often called epi bulk. For clarification, an actual doping profile of the heavily doped bulk is given in Figure 2.4.

Figure 2.3. Cross section of heavily doped bulk and lightly doped bulk. (Si: \( \varepsilon_r = 11.8 \), \( \varepsilon_r = 3.9 \), Al: \( \rho = 3.7 \times 10^{-8} \text{ohm/m} \))

Figure 2.4. A spreading resistance measurement of the doping profile of a 0.8 \( \mu \text{m} \) 3-layer CMOS process is shown here. Heavily doped substrate is used.

To analyse the crosstalk, the port definitions of interconnect lines are shown in Figure 2.5; 50 \( \Omega \) based S parameters are used here. The signal is injected at port 1, the signal received at the near end is called near-end crosstalk (port 2), expressed by \( S_{21} \), and the signal received at the far end is called far-end crosstalk (port 4), expressed by \( S_{41} \).
2.2.2 Simulation Results

Figure 2.6 and Figure 2.7 give the crosstalk versus separation distance when no shielding is applied. Both near end crosstalk and far end crosstalk vary less than 6 dB within 20 µm of physical separation distance. This is because the shielding ground is so far from the signal lines that \( h/d \) is very large. Physical separation does not work at all as Figure 2.2 shows. In addition, crosstalk in lightly doped bulk is worse than that in heavily doped bulk. However, the difference is very small, within 2 dB especially at the lower frequency. This implies that the substrate network dominates the crosstalk at low frequencies while mutual capacitance dominates when frequency becomes higher. As frequency increases, heavily doped bulk exhibits higher noise immunity due to more conductive bulk and a smaller fringing effect, and the difference between the two bulks increases. For GHz range applications, there is only around 40 dB isolation between the signal lines. When the process is scaling down, the crosstalk worsens rapidly.

2.2.3 Shielding Schemes

In order to reduce the crosstalk, shielding schemes are very necessary. High speed PCB layout techniques demonstrate that the nearer the ground (smaller \( h/d \)), the better the crosstalk. Four possible shielding methods are proposed here. In Method I (Figure 2.8), a ground line is
inserted in between. In Method II (Figure 2.9), a ground plan at the top is put to provide a nearer ground. In Method III (Figure 2.10), a ground plan at the bottom of the signal lines is put to isolate the substrate network. Method IV (Figure 2.11) involves the combination of two previous methods. However, the ground plan is not necessarily solid practically. It can be a mesh ground which can make the signal lines go up and down. The mesh ground is as efficient as a solid ground as long as the aperture size is much smaller than the operating wavelength.
2.2.4 Shielding Effects

2.2.4.1 Comparison between heavily doped bulk and lightly doped bulk

For a comparison, we applied Shielding Method II (Figure 2.9) and contrasted that with the
interference under no shielding (Figure 2.3). By placing a metal ground plane 3 µm above the signal path, the coupling is reduced by 20 dB in heavily doped substrate and by 10 dB in lightly doped substrate as shown in Figure 2.12. The difference in effectiveness can be attributed to the confined fringing field. The mutual capacitance reduces a lot after shielding.

With the added ground plan, the effective $h/d$ reduces. The separation between two lines becomes effective. The heavily doped substrate brings the bottom ground plane closer to the signal lines and reduces the fringing field more effectively than the lightly doped one. As the line width increases, the advantage of the heavily doped substrate is more prominent due to the larger metal to backside ground contact, the more compact electrical field confinement, and the

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**Figure 2.11.** Shielding Method IV: Both top and bottom shielded.

**Figure 2.12.** Comparison between two types of bulk ($L=100\mu m, f=2.0GHz$)
decreasing ratio of the fringing capacitor to the capacitor to ground. However, in lightly doped bulk, it is somewhat different. With an increasing line width, the mutual capacitance increases more than the effective capacitance to ground does. Therefore the crosstalk becomes worse with the signal line width.

### 2.2.4.2. Frequency characteristics

Comparisons of crosstalk versus frequency are given in Figure 2.13. By placing a metal ground line in between (Figure 2.8), the coupling is reduced by 5 dB at 1 GHz (Figure 2.13). Placing a large ground plane either above or below the signal lines (Figure 2.9–Figure 2.10) helps reduce the coupling by another 10 dB. Double ground shielding (Figure 2.11) provides 8 dB more reduction. As frequency increases, the need to eliminate the fringing field increases and the ground plane needs to be closer. At 1 GHz, the effectiveness of the ground plane at 1 µm or 3 µm away are the same. However, at 3 GHz, a ground plane of 1 µm away cuts down the coupling by more than 5 dB compared to having a ground plane 3 µm away. The situation is the same for both near end and far end coupling (Figure 2.14). The reason why they are so similar is that the operating frequency is not so high, and the signal line length is much smaller than the wavelength. Therefore the phase shift introduced by the line length is very small. It is worth noting that in Method I, if the middle line is not grounded, there is no improvement on the crosstalk at all.

An interesting phenomenon is that crosstalk even decreases a little with operating frequency when shielding method IV is used. There are two effects: One is that the skin effect of the metal lines worsens with the frequency and this leads to the decline of the crosstalk. The other is that electromagnetic coupling increases with the frequency. Therefore we may expect that there is a valley beyond 3 GHz. Other approaches do not show this because the loss is not
2.2.4.3. Effect of physical separation

The most dramatic improvement in coupling occurs when the fringing field is completely eliminated with a ground plane both above and below the signal line (Figure 2.11). The coupling capacitance becomes fringe field limited as physical separation increases, approaching the 2 pF/cm limit as suggested in [18]. The near complete shielding thus has the largest impact so severe.

Figure 2.13. Near end crosstalk $S_{21}$ vs. frequency, $(w=3\mu m, d=9\mu m, L=100\mu m)$: a: no shielding, b: method I, c: method II, d: method III, e: method IV.

Figure 2.14. Far end crosstalk $S_{41}$ vs. frequency, $(w=3\mu m, d=9\mu m, L=100\mu m)$: a: no shielding, b: method I, c: method II, d: method III, e: method IV.
as physical separation increases (Figure 2.15 and Figure 2.16). While the solution is extremely area intensive, it only helps to elucidate the characteristics of the coupling. It is consistent with the early conclusion that crosstalk drops dramatically if \( h/d \) is small. When the ground is near the signal lines, the field is well confined and the fringing effect is eliminated. To allow a trade-off between the crosstalk and area/metal layer penalty, Method II and Method III are possible solutions. They also provide very good crosstalk suppression. While for no shielding or Method I, separation is pointless. This is mainly due to the mutual coupling and substrate coupling through substrate resistive network.

![Figure 2.15](image)

**Figure 2.15.** Near end crosstalk S21 vs. separation distance. (\( w=3\text{um}, L=100\text{um}, f=2.0GHz \)) a: no shielding, b: method I, c: method II, d: method III, e: method IV.

### 2.2.4.4. Effect of signal line length

Figure 2.17 and Figure 2.18 show the coupling as a function of line length. As expected, coupling becomes increasingly linear (flat on a log scale) as the line length increases since the mutual capacitor increases linearly with the length. To reduce the crosstalk introduced by a long signal line, in a digital circuit the long line is usually cut into pieces and the repeaters are inserted in stages; In the analog case, the long lines should be avoided especially for high frequency signal lines or a low-voltage low-swing amplifier should be inserted.
2.2.4.5. Effect on transmission line impedance

Unlike a conventional transmission line in RFPCB, a transmission line in RFIC is lossy. Both the metal lines and the substrate are lossy material. Since $R$ and $G$ in (2.1) cannot be neglected compared to the imaginary part, the characteristic impedance is a complex value rather than a real value.
where $R$, $L$, $G$, $C$ are the effective resistance, inductance, conductance and capacitance respectively in a unit length. As shown in Figure 2.19, $Z_0$ in lightly doped bulk is larger than in heavily doped bulk. With more grounded metal layer, $Z_0$ continues to decrease.

### 2.2.5 Discussion

The proposed shielding methods provide excellent crosstalk immunity. However, the disadvantage perhaps is an area/metal layer penalty. However, because today’s technology can support five to seven metal layers, the sacrifice of one layer allows the reduction of the severe crosstalk between critical circuit blocks, especially in analog circuits. In addition, with shielding, the separation distance becomes much smaller than when no shielding given the same crosstalk requirement. This may save area sometimes.

Furthermore, even when using the metal ground shield (Method II, III or IV), active devices and circuits can be placed underneath. Since the thickness of the gate oxide ($<10\text{nm}$) is
much smaller than the distance to the ground shield (~1\µm), the introduced parasitic capacitance is much less than one per cent of the total gate capacitance if we make an approximate calculation. Moreover, the backside contact will become less effective due to the skin effect as the frequency increases. The additional shielding layer can provide more substrate noise suppression due to a more confined electric field to the better ground.

Practically, mesh ground can be used instead of solid ground. Due to the weaker electric field confinement, a meshed-shielding configuration generally exhibits a higher crosstalk level than a solid structure. This crosstalk can be reduced by increasing the line separation. $Z_0$ increases a little bit too.

### 2.3 Substrate Noise

Substrate noise, the kind of noise current that is injected into the substrate from an active
device, has received considerable attention in mixed signal circuit design. In this section, an analysis of the noise sources and paths, noise impacts, and noise prevention methods is given. Guidelines to reduce the noise are given also.

2.3.1 **Noise injection, transmission and reception**

2.3.1.1. Noise injection

1. Hot carrier effects in MOS devices are more severe in NMOS devices because of the higher electron ionization-coefficient [16]. $I_{\text{sub}}$ is proportional to $|V_{ds}-V_{\text{dsat}}|$. So, the larger the $|V_{\text{dsat}}|$, the smaller the current injection. Hot-electron induced substrate currents may be the dominant cause of substrate noise in NMOS up to at least one hundred megahertz. Shorter device channel lengths are likely to worsen this problem due to increased channel fields and smaller $t_{ox}$ and $x_j$. This is different from capacitive coupling because the hot-electron induced currents are always injected into the substrate, and this introduces a DC component and even-harmonics into the substrate. Capacitive coupling introduces odd-harmonics. This causes a drift in threshold voltages and leads to an increase in the minority-carrier injection into the substrate due to the partial forward-biasing of device-to-substrate junctions. At the same time, it will lower the output impedance of the transistor.

2. Junction capacitance to the substrate (diode), such as source/drain diffusion, N-Well. The larger the reverse bias voltage, the smaller the junction capacitance, and the better the substrate noise.

3. Parasitic bipolar transistors. They are formed by the PMOS source/drain, N-Well and P type substrate, including the parasitic lateral bipolar and the parasitic vertical bipolar.
Dedicated bias should be used in order to ensure the parasitic transistors DO NOT work in the forward-active region. A sufficiently low impedance path must be provided near the device in order to collect the current.

4. Steady DC leakage current of reverse-biased pn junctions. This is a kind of majority-carrier drift current. Electrons are injected into the n-region and holes into the p-region under the action of the field. This may change the substrate voltage potential.

Of the noise injection sources, impact ionization current and capacitive coupling from the drain and source junctions are found to be the most significant contributors to substrate current injection.

2.3.1.2. Noise transmission

1. Oxide capacitance. The interconnections or passive components such as resistors, capacitors and inductors can introduce crosstalk to the substrate through the silicon dioxide. Using a higher layer leads to a smaller oxide capacitance which reduces the substrate noise injection. Using a shielding layer can isolate the components from the substrate. However, this layer should be very well grounded.

2. Resistive substrate network. This is another important transmission path of the substrate noise. To shorten the propagation path, the use of a proper guard ring can absorb current leakage and provide low impedance path for the substrate noise to the ground. However, if not designed properly, the guard ring may inject very high levels noise into the substrate as they act as the ground on the substrate, and any voltage bounce on the guard ring may be conveyed throughout the chip through a very low impedance path.

3. Package/bondwire inductance or package/substrate capacitance. Switching noise is often
injected to the substrate by $Ldi/dt$ mechanism while package/substrate capacitance couples the interference directly to the substrate. Chip on board and short or paralleled bond-wires may be used to reduce the coupling.

### 2.3.1.3. Noise Reception

1. Body effect. Any voltage bounce at the body of MOS transistor will introduce current at the drain through $g_{sub}$.

2. Capacitive sensing. Diodes, parasitic bipolar, MOS transistors, interconnections and all passive components are all capable of this.

The body effect in MOSFETs makes the devices especially vulnerable to substrate noise reception. While the capacitive pickup, exhibited by most other devices, becomes significant only at relatively high frequencies, the body effect can be an issue at low frequencies [16].

### 2.3.2 Impacts on devices and circuits

There are many impacts introduced by substrate noise as follows:

1. The body effect in MOSFETs. Differential configurations can help to eliminate this problem since the body is common-mode. The lower the substrate noise, the less the body effect. In addition, the body itself should be well shielded or grounded.

2. Power loss in the substrate. Silicon substrate is lossy in nature and is modeled as distributed resistors. Loss in the substrate lowers the efficiency of the circuit components and must be minimized. For example, the Q of the inductor largely depends on the substrate loss. The leakage current will lead to a DC power loss in the substrate.

3. Degradation of circuit noise performance, SNR. For example, LNA noise performance
can be degraded due to resistive loss in the substrate. Inserting a ground plan under the input pad of LNA is necessary.

4. Changes in circuit bandwidth. This is mainly due to the parasitic capacitance and substrate resistive network as a feedback path.

5. Changes in circuit gain. This occurs for the same reason as given above. In addition, the body potential changes also with the substrate leakage current and changes the transconductance $g_{mb}$.

6. Worsening of the phase noise. The phase noise of an oscillator can be degraded by the thermal noise of the substrate resistor or substrate noise injected by other circuits.

7. Oscillation with proper positive feedback introduced by resistive substrate.

8. LO leakage, DC offset. This is due to severe coupling between the LO and LNA/Mixer input.

9. Signal blocking. Severe substrate coupling may block the small input signal at the LNA/Mixer input.

### 2.3.3 Guard ring noise reduction schemes

Guard rings can be placed around the noise injector, the noise sensor, or on both sides to reduce the substrate noise. Several kind of guard rings, such as the P+ guard ring, the N-well guard ring, the N+ guard ring, or any combination of three are usually used. The P+ guard ring collects injected electrons while N-type guard ring only can collect injected holes. However, very few studies compare their performance on substrate noise reduction. In this section, the effectiveness of possible guard ring schemes at high frequency is discussed.

The device simulator Medici [19] was used in our research. Figure 2.20 shows the simula-
tion setup. The size is not well scaled as it is only for illustration purposes. Heavily doped bulk was studied and only 48µm thickness was assumed to save simulation memory and time. The following conditions were assumed: 0.15µm junction depth, 2µm N-well thickness, around 60µm separation distance between the noise injector and noise sensor. The AC signal was ac coupled and injected through the pn junction. The noise voltage was measured at NMOS drain output. Only the noise injector is protected by different guard rings (a-c), where an N+ guard ring can be replaced by an N-well guard ring. Guard rings can be either biased at the fixed DC voltage or floated when simulated.

![Medici simulation setup.](image)

It is well known that using a guard ring reduces the substrate noise at low frequencies. It can lead to a 40dB noise improvement, say at 100MHz. The guard ring performance at 1GHz was simulated and the relative amplitudes under different guard ring shieldings are shown in Figure 2.21. 0 stands for floated guard ring and 1 means the biased guard ring. The order is from (a) to (c) in Figure 2.20. A single P+ guard ring had the best performance. That is to say, the use of more guard rings do not mean a greater suppression of the substrate noise. The
nearer the p+ guard ring, the better the noise performance. Using an N+ guard ring is always better than using an N-well guard ring due to smaller junction capacitance and lower impedance. Compared to the case where all rings are floated (no ring 000), the P+ guard ring (100) improves around 14dB at 1GHz. If there is no P+ guard ring before the N+ or N-well guard ring, the noise performance degrades by 8dB. This is mainly due to the fact that there is no current leakage absorption.

One test chip was fabricated in an AMS BiCMOS process for substrate noise measurement. The die photo is shown in Figure 2.22. On the left side is a power amplifier driver (PAD) which operates at 900MHz [20]. The guard taps (P+/N+/P+) were controlled by floating or bonding to the fixed voltage. A noise sensor was made by paralleling a MOS transistor (80µm/1µm) and a bipolar transistor with separated gate/base input and a 1kΩ resistor load on chip. Only one transistor was on at any one time. By doing so, the substrate noise absorption or injection efficiency of both devices was compared. The noise injector is the same as the noise sensor and it is surrounded by P+/N+/P+ guard rings. A bipolar mixer similar to [21] was
placed after the noise injector to test its performance in a noisy environment. By combining PAD with the guard taps and the noise sensor, the effectiveness of the guard taps can be measured. In addition, we combined the noise injector and the noise sensor to test different guard ring schemes, as in the simulation above. By injecting signal to the noise injector, we could also measure the mixer performance in the substrate noise environment. Unfortunately, due to fragile bonding PAD of the process, the die could not be bonded to the PCB successfully. Therefore, no test results can be presented here.

2.3.4 Guidelines to reduce substrate noise

To reduce substrate noise and to get high integration, some guidelines for circuit design and layout need to be followed.

2.3.4.1. Quiet the talker.

1. Avoid switching large transient supply current. Shut down all switching functions or drivers not in use; ramp the clocks or reduce their rise time; reduce the clock feed through; low-voltage low-swing signals are preferred; use differential if possible.

2. Lower switching function bus impedance. Provide low resistance and low inductance power bus; use paralleled bondwires or multiple pads for power supply; provide distribu-
uted on-chip decoupling since off-chip capacitors self resonate at much lower frequencies.

3. Use guard rings around the noise injector to provide the low impedance path to absorb noise current.

2.3.4.2. Isolate the listener.

1. Well-grounded substrate for heavily doped bulk. The backplane inductance must be as small as possible. If the substrate is well grounded, all currents will flow directly and vertically to the ground, not through the lateral low impedance path. That is, the lateral current flow is restricted. If this is not done, the substrate noise will be extremely high due to lateral current flow. In this kind of low-resistivity substrate, the most effective way of improving isolation is to provide a very good ground contact to the backplane. Surface isolation structures similar to guard rings are not so effective in these substrates.

2. Substrate taps or guard rings should be used in lightly doped bulk. The guard ring is effectively a current sink for the surface component of the current. Unlike that in heavily doped bulks, the isolation in lightly doped substrates is weakly dependent on the value of the backplane inductance. This is due to significant surface conduction. Consequently, substrate taps or guard rings can be expected to be more efficient in lightly doped bulks compared to heavily doped substrates. In addition, put the guard ring or other low impedance path as close as possible to the circuits. However, it is not true that the wider the guard ring width, the better the isolation. As a rule of thumb, several microns is enough. Moreover, the inductance from the guard ring to the ground should also be as small as possible.
3. Separate the noise injector and the noise sensor by a certain distance. This is more effective in lightly doped bulk; it is not so sensitive to the distance in heavily doped bulk. For heavily doped bulk, above 30 microns separation is recommended between circuits, about four times the epi thickness [11].

4. Physically separate the package/chip power supply and ground pins for noisy and sensitive circuits to avoid common resistor/inductor induced power bounce noise at the power pins.

5. Reduce all kind of parasitics. Chip on board with conductive epoxy is highly recommended. The signal path must be as narrow as possible or use higher metal layer to reduce the oxide capacitance. However, the line resistance and inductance increases, especially at high frequencies. Therefore, long signal lines should be avoided also.

6. Using a grounded metal/poly/active layer to cut off the path to the substrate is necessary in order to reduce the noise and the loss as we mentioned in the above section, especially for LNA and on-chip inductor application.

7. Avoid any kind of floating geometries. Packages with any form of floating metal can dramatically increase radiated emissions as well as chip crosstalk. Floating metal increases capacitive effects and increases electromagnetic effects.

2.3.4.2. Close the listener’s ears.

1. It is better to use guard rings both at the noise source and at the noise receiver. Every guard ring must be connected to the ground separately with a low inductance. If only one guard ring is used, then it is preferable to put it around the noise injector. If this is done,
20dB improvement can be achieved. This is better than it was put around the noise receiver.

2. Reduce the loading if possible. The isolation scales linearly with the load when the pole at the load is far larger than the interested frequencies. The larger the load, the worse the isolation.

3. Differential circuits and symmetrical layout will provide excellent isolation, especially in heavily doped bulk due to the low impedance path in the substrate. In addition, the isolation is not sensitive to the backplane impedance in both kinds of bulks when differential is used.

4. Design circuits for high common mode rejection ratio (CMRR) and power supply rejection ratio (PSRR).

5. Use minimum required bandwidth for the sensitive circuits if possible.

2.4 Conclusion

Two kinds of crosstalk were presented in this chapter. It was shown that physical separation is pointless if no shielding schemes are adopted. Proper shielding can ensure a 30dB better noise immunity to electromagnetic interference. To reduce substrate noise, guard ring shielding schemes were investigated. A single P+ guard ring provides the best noise suppression. Guidelines for circuit design and layout were also discussed.
CHAPTER 3

Flicker Noise

The crosstalk and substrate noise discussed in the last chapter are common issues for all kind of single-chip solutions. For direct conversion receivers, there are some special issues which do not exist in other system architectures. Of them, flicker noise associated with CMOS device is one of the biggest concerns. In this chapter, through measurements, flicker noise mechanism under both DC and large signal conditions are discussed.

3.1 Introduction

Low frequency noise in silicon MOSFET’s is dominated by flicker noise. It is commonly known as 1/f noise since the noise spectral density is inversely proportional to frequency. Because MOSFETs have large flicker noise, this sets a lower limit to the level of signal that can be processed by analogue circuits. Much effort has been put on understanding and reducing the noise to ensure a better performance in analogue circuits. In the last half century, a considerable number of papers have been published dealing with 1/f noise in MOSFETs [22]-[43].

Two different theories have been put forward to explain the physical origins of flicker noise. In the carrier number fluctuation theory [23]-[28], originally proposed by Mc-Whorter [29], flicker noise is attributed to the random trapping and detrapping processes of charges in
the oxide traps near the Si-SiO$_2$ interface. The charge fluctuation results in fluctuation of the surface potential, which, in turn, modulates the channel carrier density. It is assumed that the channel can exchange charges with the oxide traps through tunneling. For a uniform oxide trap distribution in the energy gap, the theory predicts an input referred noise power which is independent of the effective gate voltage, $V_g - V_{th}$, but inversely proportional to the square of the gate capacitance, $C_{ox}$. The number fluctuation model is supported by the widely observed correlation between the flicker noise power and interface trap density [25], [26], [30]-[34]. The mobility fluctuation theory [35]-[37], on the other hand, considers flicker noise as a result of the fluctuation in bulk mobility based on Hooge's empirical relation for the spectral density of flicker noise in a homogeneous sample. It has been proposed that the fluctuation of bulk mobility in MOSFET’s is induced by fluctuations in phonon population through phonon scattering [38], [39]. The input referred noise shows strong gate bias dependence. Chang [40] proved that input referred noise from the $n$-channel transistors very often is independent of gate bias and can be modeled as carrier density fluctuation while that of $p$-channel devices is dependent of gate bias and can be modeled as mobility fluctuation. Hung [41] [42] unified two kind of models with more fitting parameters and explained the flicker noise very well compared with experimental data. The current spectral density and input referred noise are expressed by

$$S_{vd}(f) = \frac{kT\mu^2}{\gamma fWL^2} \int_0^L N(E_{fn}) \left[ \frac{1}{N(x)} \right]^{\pm \alpha \mu} dx$$  \hspace{1cm} (3.1a)

$$S_{vg}(f) = \frac{kT}{\gamma fWL} N(E_{fn}) \left( \frac{q}{C_{ox}} \right)^2 \left[ \alpha \mu (V_g - V_{th}) \right]^p$$  \hspace{1cm} (3.1b)

where $E_{fn}$ is quasi-Fermi level, $N(E_{fn})$ is the distribution of the traps, $\alpha$ is scattering coefficient, $\mu$ is the mobility, $p$ is a bias-dependent parameter with a value varying from 0 to 2. When $p=0$ the model reduces to the conventional number fluctuation model. At higher gate bias
(when \( p = 1 \)) it predicts a flicker noise behavior similar to that predicted by the bulk-mobility fluctuation theory. The formula is based on uniform distribution of the oxide trap. In reality, it is non-uniform and the slope changes from 0.7 to 1.2 with the gate bias [28][43].

Most studies mentioned above focus on flicker noise under the static DC bias condition. However, except for the case in which the circuits operate at a static DC bias, in RF applications, the transistors often move rapidly from one operating region to another. In an ordinary mixer or an oscillator, the transistors go from the off state to the saturation region or linear region. In a new type of harmonic mixer [44], the transistors switch within the saturation region only. The effect of \( 1/f \) noise in these rapidly changing environments is rarely reported [45]-[47]. Gierkink [45] has observed the difference between static DC conditions and switching conditions and utilized it to improve the noise performance of the circuit. But the property and mechanism of flicker noise under switching conditions has not been deeply studied. Darabi [46] analyzed theoretically, the switching case in a mixer from the linear region to the off state, and gave a simple model under some assumptions. An understanding of noise in other switching transitions is still necessary. T. Melly [47] used the same model as in [46] to formulate gilbert mixer noise equations but without any experimental evidence on the noise model also. Wel [48] studied flicker noise in switched bias conditions but gave no detailed spectrum analysis or deep insight into the \( 1/f \) spectral composition. He ignored the noise spectral peaks although they are important to oscillator applications and noise harmonic composition.

Flicker noise appears in more complicated ways at the output of mixers or oscillators. In voltage-controlled oscillators, flicker noise up converts into close-in phase noise [51][52]. In current commutative mixers, flicker noise in the switches appears at the output at baseband [46][53]. This can significantly raise the noise figure in a direct conversion receiver. Unlike the thermal noise, flicker noise is a kind of correlated noise and is difficult to study especially in
large signal conditions. There are several reasons for this. It is hard to evaluate with the circuit simulator due to its correlated property. Nonlinear operation of the circuit adds more complexity. Usually the high frequency spectrum analyzer is single-ended and the common-mode signal and noise from the circuit cannot be suppressed easily. Therefore, the flicker noise part is buried in the signal spectrum.

In this chapter, we focus on the characteristics, the model, and the impact of $1/f$ noise in various switching conditions. In the following section, flicker noise measurement under a static DC bias condition is discussed. Then the measurement setup in a switching condition is given. The methodology used to analyze the noise spectrum is described and the measurement results are shown. In addition, methods to reduce the flicker noise are discussed. Based on the measurements, the flicker noise model is proposed. This is validated by simulations and measurements. An application is demonstrated and, finally, a conclusion is drawn.

## 3.2 Flicker Noise under Static DC Biases

To understand flicker noise more clearly, flicker noise under static DC biases was first measured. Figure 3.1 shows the flicker noise measurement setup. The BTA noise measurement system was used in our research [54]. After system noise floor calibration, the current noise of the device under test (DUT) was amplified by BTA9603 and was analyzed using a dynamic signal analyzer SR780 [55]. The noise current spectrum was sampled and averaged and sent to the computer using the HPIB bus. The input-referred gate noise was derived according to corresponding transconductance of the device. Two important issues need to be considered when measuring flicker noise. One is effect of the thermal noise floor of the device; the other is the effect of the output impedance of the transistor. When measuring the slope of the flicker noise,
the thermal noise floor should be deembedded out. This can be done by fitting the sum of flicker noise and thermal noise with measured data. The output impedance is also very important. The BTA measurement system assumes that DUT has large output impedance so that all noise current can flow through the load impedance of the BTA system and the machine can calibrate the system accurately. However, this is not true in a practical situation especially when the DUT operates in linear region. Therefore, when measuring noise in linear region, it is better to use an SR780 with very high input impedance to measure the total output noise voltage rather than to use the BTA system to measure the total output noise current. After considering both the output impedance and the transconductance of the device, it is easily to refer the output noise voltage to the input-referred gate voltage noise.

The drain current noise spectrum of the pmos and nmos device fabricated in the TSMC0.35\(\mu\) process are given in Figure 3.2. The noise increases with the drain current. With the same bias current and the same size, noise in nmos can be ten times larger than that in pmos. The corner frequency of pmos under a lower bias current can be clearly seen while that of a nmos device is larger than 100kHz. The corner frequency can be simply determined by

![Diagram](image-url)
equaling flicker noise to thermal noise floor:

\[ S_{v_g}(f_c) = \frac{K_f}{WLC_{ox}f_c} = 4kT\gamma \frac{1}{g_m} \]  

(3.2a)

\[ f_c = \frac{K_f}{4kT\gamma} \cdot \frac{f_T}{WL} \]  

(3.2b)

The simple Hspice flicker noise model is used here. The corner frequency is proportional to the unity-gain frequency \( f_T \). With the same transistor size, a larger drain current, a larger \( f_T \), a larger corner frequency can be seen in the figure.

To understand flicker noise more easily, we may start from the simple current equation without looking at complicated equation (3.1):

\[ I_d = W\mu qNE_x \]  

(3.3)

The fluctuation of both mobility \( \mu \) and number carrier \( N \) causes the fluctuation of output current. The fluctuation of mobility \( \mu \) may be modeled by drain current noise, while the fluctuation of carrier number \( N \) may be modeled by gate voltage noise. NMOS and PMOS devices have different noise mechanisms which depend on which factor is dominant. As described in the introduction section, the flicker noise of n-channel transistors can be modeled as carrier
density fluctuation while that of p-channel devices can be modeled as mobility fluctuation. After referring the drain current noise back to the gate voltage input in Figure 3.3, it can be seen that noise in pmos is much more bias dependent than that in nmos. For nmos transistors, the input-referred gate noise keeps almost constant in the whole saturation region as predicted by the carrier number fluctuation. This phenomena significantly simplifies the flicker noise model in circuit simulators. For pmos transistors, the minimum input-referred noise appears in medium inversion region. In addition to low flicker noise in this region, the maximum available voltage gain of the transistor is available near this region while $f_t$ of the device does not degrade very much. However, the linearity of the circuit suffers a little bit.

In conclusion, to reduce the flicker noise under static DC bias condition, a long channel device is preferred for smaller $\gamma$ and larger area; reducing drain current can help reduce flicker noise significantly since the output current noise is proportional to $I^2$; and a thinner oxide thickness helps also from the point of view of process; a smaller effective gate voltage ($V_g-V_{th}$) is preferred, if linearity requirement permits; buried-channel pmos devices can be used instead of nmos ones in special kind of circuits to reduce flicker noise.

![Figure 3.3. Input-referred gate voltage noise spectrum density $S_{vg}$](image-url)
3.3 Flicker Noise under Switching Condition

Having discussed flicker noise under the static bias condition, we now explore a more complicated case, switching flicker noise.

3.3.1 Measurement Setup

To study correlated flicker noise in a nonlinear environment, measurement was done with a setup shown in Figure 3.4. Well-matched differential transistors with their gates and sources connected together were fabricated in the same process and with the same device size as in Figure 3.3. The photo of this is shown in Figure 3.5.
The transistor size selection was important. It is well known that flicker noise is an integration of random telegraph noise [56]. If the transistor size is too small, the $1/f$ shape cannot be observed. On the other hand, if the transistor size is too large, the noise amplitude is too small to detect. A long channel device was chosen to eliminate the short-channel effect on the flicker noise and to minimize device mismatch. Note that the circuit and the spectrum analyzer are fully differential and the CMRR of the analyzer is around 90dB. This eliminated the uncertainty and common-mode noise of the input signal that are usually associated with a single-ended test setup. Although the measurement was sensitive to the power supply noise due to high CMRR of differential analyzer, a very good power supply from Agilent was used to further eliminate the influence of supply noise and a series of decoupling capacitors were used at the power supply track. Variable resistors were used to compensate for the device mismatch and to suppress the common mode signal and noise generated by the function generator. Their values were chosen to ensure proper transistor operation region and sufficient bandwidth for differential output. Any device mismatch would not affect the total flicker noise from the devices at the output and only the common-mode rejection to the signal leakage was affected. A low frequency differential dynamic signal analyzer SR780 with very high frequency resolution and low noise floor was used to analyze the noise spectrum. The input impedance of the analyzer is as high as 1MΩ so that it does not affect the whole switching system. The valid frequency range is within 102kHz.

How this setup was used to study high frequency switching such as in a mixer or an oscillator is depicted in Figure 3.6. A complicated non-linear system can be divided into a frequency-independent non-linear system and a frequency-dependent linear system, such as a mixer. A frequency-independent non-linear system can be studied through a low frequency non-linear system under enough output bandwidth. This was done easily using our measurement setup.
We consider the linear part such as low-pass effect later on. However, the study is based on a big assumption, a frequency independent non-linear system. Fortunately, this assumption is true given enough output bandwidth as will be seen in the following section.

To study the effect of the rising and falling edge of the input signal on the output noise, an important consideration for mixers and oscillators, and the correlation of spectrum harmonics and total noise output, different waveforms was applied, as shown in Figure 3.7. $V_{GSeff}$ is the static DC bias which obtains the same DC current as that in the switching case. The value of $V_{PK}$ was used to tune the transistors into different operating regions.

To study the effect of the rising and falling edge of the input signal on the output noise, an important consideration for mixers and oscillators, and the correlation of spectrum harmonics and total noise output, different waveforms was applied, as shown in Figure 3.7. $V_{GSeff}$ is the static DC bias which obtains the same DC current as that in the switching case. The value of $V_{PK}$ was used to tune the transistors into different operating regions.
3.3.2 Spectrum Analysis and Experimental Result

The output bandwidth of the measurement system was determined by the resistor load and the input capacitance of the analyzer and set at around 8MHz. Less than 1MHz switching input was applied so that there was no waveform distortion at the output. The thermal noise floor of the devices and resistors plus the system noise floor were well below -150dBm/Hz. This did not affect our flicker noise measurements. The spectrum window between 1k to 100kHz was chosen in order to shorten the integration time and noise average time. Annoying 50Hz related interferences from power supply never appear at this frequency range. The switching was set from the off region to the saturation region with a 50% duty-cycle square wave input. Such switching is the usual case for mixers and oscillators.

![Figure 3.8. Baseband noise under fast switching. Input: Square Wave VGS=0.6V VPK=0.5V (OFF-SAT).](image)

Fast switching case was first studied, as shown in Figure 3.8. ‘Fast’ means the switching frequency was larger than the analyzer bandwidth 102kHz. At the same time, it was near or larger than the corner frequency of the flicker noise so that there was small noise folding inside the analyzer spectrum. We were pleased to see that the output baseband noise was switching
frequency independent given enough output bandwidth. This phenomena is also consistent with the assertion in [46]. As a result, a quiet and versatile generated waveform was used at the input to simulate the effect of switching at a higher frequency and to study the flicker noise spectrum composition under a non-linear environment.

While earlier studies have postulated that the correlated flicker noise could not respond to switching, Figure 3.9 shows that there are large noise peaks at the harmonics. A superposition of flicker noise at each harmonic component of the output current is seen. At the lower frequency end, the noises in different switching frequencies converge. It is clear that the noise contribution from the DC harmonic is the same. This is consistent with the observation in Figure 3.8. The limited common-mode rejection leads to signal harmonic leakage superimposed on the output noise.

Based on the switching frequency independence property of the baseband flicker noise observed above, the noise contribution from the DC component of the current can be approximated by the noise under fast switching. To study the relationship of the noise harmonics, the

![Figure 3.9. Baseband noise under slow switching.](image-url)
flicker noise at DC was subtracted out. The noise at the harmonics is shown in Figure 3.10. The symmetrical noise spectrum can be clearly observed. A kind of flicker noise upconversion is evident.

To be more precise, the spectrum was further processed by shifting the right-side band noise at the switching frequency to zero frequency, as plotted in Figure 3.11. The spectrum in the higher switching frequency such as 50kHz is exactly parallel to that of the DC harmonic noise response. When the switching frequency is low, the noises at higher harmonics are superimposed on the side band. The parallel relationship cannot be seen clearly. A conclusion that the output noise is a superposition of upconverted flicker noise at each harmonic component of the output current can be drawn. The exact numerical relationship between the dc component induced noise and harmonic noise can be measured from the figure.

Figure 3.12 shows the comparison between constant DC bias and switching conditions. A more than 6 dB noise reduction under switching was achieved compared to their static on state (1.1V). This reduction comes from smaller effective transconductance. When the on state volt-
age is fixed, the smaller the off state voltage is, the smaller the flicker noise, and the smaller is the slope. This phenomena is also observed in [48]-[50]. However, noise reduction was not so obvious in our measurements. There was only around a 0.3dB reduction. It is usually thought that the traps which cause flicker noise do not respond to fast switching. However, the possibility of the traps being charged or discharged is lowered during switching due to an increased number of collisions. This is especially true for deep traps which have long time constants [45]. They need a larger voltage bias to activate the traps. During switching, the effective gate voltage becomes smaller and the number of deep traps decreases, and so they contribute less noise at the low frequency band and the slope becomes smaller. When the on state voltage is fixed, the off state voltage influences the effective gate voltage and the number of traps to attend the charging and discharging process. The energy to active the traps becomes larger as the off state voltage decreases although the time-varying current and tranconductance do not change. In other words, the input-referred noise and slope do not keep constant with different

Figure 3.11. Single side band harmonic noise response compared to noise contribution from DC component.
switching conditions even for nmos transistors. The above analysis allows a natural explanation as to why the slope in linear region is usually larger than that in saturation region. Relatively, more deep traps contribute noise in the linear region since the channel is uniform. The channel is not uniform in the saturation region and a smaller number of deep traps attend the trapping and detrapping process.

Figure 3.12. Noise comparison between static DC and switching conditions (VGSon=1.1V).

The trap response under switching is studied. Figure 3.13 gives a close-up of the noise spectrum with different switching frequencies. The right-side band noise is larger than the left-side band noise when the switching frequency is low. This means that, in addition to the superposition of upconverted noise, some traps with short time constants which respond to the switching signal also contribute noise to the output. Moreover, the lower the switching frequency, the larger the right-side band noise. Consequently, the total noise spectrum may include two parts, harmonic noise response, and the response of traps with small time constants. As switching frequency increases, the latter reduces and diminishes, and the upconverted harmonic noise dominates. For nonlinear circuits, usually the switching frequency is
much higher than the flicker noise corner frequency. The corner frequency corresponds to almost the smallest trap time constant, and this part of noise can be ignored.

![Figure 3.14 showing measured baseband output noise with different switching transitions compared to static DC bias conditions. Current switching includes saturation to saturation (SAT-SAT), saturation to linear (SAT-LIN), and linear to linear (LIN-LIN). Voltage switching includes off to saturation (OFF-SAT), and linear to off (LIN-OFF) transitions. The peak of static DC noise is the transition from the saturation to the linear region. The baseband noise is close to static DC noise except LIN-OFF when the switching amplitude is small.](image)

Figure 3.14 shows the measured baseband output noise with different switching transitions, compared to static DC bias conditions. Current switching includes saturation to saturation (SAT-SAT), saturation to linear (SAT-LIN), and linear to linear (LIN-LIN). Voltage switching includes off to saturation (OFF-SAT), and linear to off (LIN-OFF) transitions. The peak of static DC noise is the transition from the saturation to the linear region. The baseband noise is close to static DC noise except LIN-OFF when the switching amplitude is small.

OFF-SAT and LIN-OFF are often used in normal mixer and oscillator applications. SAT-SAT can be used in a specific current switching mixer [44]. LIN-LIN and SAT-LIN may be used in current-mode circuits. The figure indicates that different transitions have different properties. For OFF-SAT and LIN-LIN, the larger the swing, the larger the output noise. This is different from OFF-LIN and SAT-LIN. In the case of OFF-SAT, the noise variation with the
switching swing decreases with $V_{GS}$. To reduce the output noise, a small $V_{GS}$ and a small swing should be chosen. When entering SAT-SAT, the output noise, which keeps almost constant, is very close to the static DC bias condition. LIN-OFF and SAT-LIN have the same tendency. The minimum output noise can be achieved by biasing the $V_{GS}$ at the transition point from the saturation to linear region with the largest switching swing for these two cases. The conclusion is of significance to mixer output baseband noise. In addition, for LIN-OFF and SAT-OFF, if the on state voltage is fixed, lowering the off state voltage also reduces the noise.

The spectrum composition of the output noise under switching and different transitions was discussed. The measurement and analysis were based on the fact that enough output bandwidth is ensured. However, the output bandwidth definitely influences the results because it affects the harmonic composition of the output current when it is smaller than the switching frequency. For down conversion mixers, the switching frequency is much larger than the output bandwidth. The output noise is dependent on the switching frequency. Having looked at the

![Figure 3.14. Measured baseband noise with different transitions. Volts indicated inside the graph are switching swing VPK. Input: Sine Wave @ 1MHz.](image-url)
non-linear process of flicker noise under switching, in the next section we will discuss the
effect of output bandwidth using the noise model, and combined the model with a linear filtering
system.

### 3.3.3 Flicker Noise Modelling

Based on the flicker noise spectral composition obtained from experimental results dis-
cussed above, flicker noise under switching can be modeled by amplitude modulation (AM) as
shown in Figure 3.15. $G(t)$ is periodic time-varying transconductance, where $g_k$ is discrete Fou-
rier series coefficient. $g_0$ reflects the baseband noise which is important to a downconversion
mixer and $g_1$ reflects the harmonic noise at switching frequency which is important to oscilla-
tor. $w_0 = 2\pi \times$ switching frequency $f_0$. $R_0$ and $C_0$ are the effective output impedance and capaci-
tance of the transistor. These two components combined with the loading in the circuits form a
linear filtering system which affect the total output current noise.

\[
G(t) = \sum_{k = -\infty}^{\infty} g_k e^{jkw_0t} = g_0 + 2 \sum_{k = 1}^{\infty} g_k \cos(kw_0t) \tag{3.4}
\]

The total current noise spectral density can be calculated by

\[
S_{id}(f) = \sum_{k = -\infty}^{\infty} \left| g_k \right|^2 F^2(kf_0) S_{vg}(f - kf_0) \tag{3.5}
\]

where $S_{vg}(f)$ is the effective flicker noise gate noise power and $F(kf_0)$ is the transfer function
of the linear filtering system.

Using the proposed model, it is possible to calculate or simulate the noise level at the output of a nonlinear circuit. The method involves applying a small signal at the gate of the
switching transistor, and simulating its gain at the harmonics of the switching frequency
including DC. The total noise at the output is the superposition of upconverted noise at each harmonic. However, it was found that the model could not be applied to LIN-OFF transition. The LIN-OFF case can be modeled by pulse width modulation (PWM) due to its sharp edge and large swing. A theoretical formulation was given in [46] under certain assumptions.

The proposed model was verified using different switching waveforms through measurement and Hspice simulation. After applying both the large switching signal and a small ac signal at the gate, gains at each harmonic of switching frequency were measured in the Hspice simulation. Directly measured baseband noise outputs are shown in Figure 3.16.

The comparison between the simulation and measurement results given in Table 3.1 indicates that the results agreed well. One interesting result is that the output noise depends on the signal feed-through gain $G_0$ rather than on the slope of the waveform. The capital $G$ means the voltage gain rather than the transconductance gain $g$. It was expected that square wave switching should show lower flicker noise rather than sine wave switching due to its sharp slope. But the measurement result is opposite to what was expected. Conventional thought on flicker noise seems not to be correct.
Different switching transitions are also presented in Figure 3.17. The solid line stands for the simulation and the symbols for processed data from the measurement. The noise response at the switching frequency is very small for both SAT-LIN and SAT-SAT. This implies that flicker noise upconversion can be ignored and only baseband noise is dominant. This shows flicker noise is more correlated for these two kind of transitions. The harmonic noise at the
switching frequency increases very rapidly with the switching amplitude for LIN-LIN transition, while it is relatively large for OFF-SAT but not so sensitive to the swing. OFF-SAT transition exhibits the more uncorrelated properties as thermal noise.

However, LIN-OFF is a different story. Figure 3.18 shows the difference between LIN-OFF and other transitions. As predicted in [46], the noise appears only at the even harmonics for LIN-OFF transitions while other transitions have odd-harmonic noise components. The peak at the switching frequency and its odd harmonics in the spectrum for LIN-OFF is switching signal leakage which is due to non-ideal common-mode rejection. From the sideband of the peak it can be easily seen which peak is flicker noise upconversion and which peak is signal leakage. However, this is not always true if the input waveform is ramp wave under hard switching in the LIN-OFF case. The smooth edge contributes AM-type noise and the steep edge contributes PWM-type noise. The total noise is the combination of both, and the noise peaks appear at all harmonics. Fortunately the ramp wave is not often used in the real world. It was used here for research purpose.

![Figure 3.17](image-url)  
Figure 3.17. Model verification by different transitions. Solid line stands for simulation and symbols for measurements. Input: Sine Wave.
The spectrum analysis in Figure 3.19 is consistent with the formula given in [46] that the noise response at double switching frequency is the same as the DC harmonic noise response. Unfortunately, for this hard-switching case, our Hspice simulation does not agree with our measurement as seen in Table 3.2 although simulations on $G_1/G_0$ are pretty good. It implies that LIN-OFF transition should be modeled by PWM model rather than our proposed AM model.

**Figure 3.18.** LIN-OFF transition has a different mechanism from other transitions. Input: Sine Wave.

The spectrum analysis in Figure 3.19 is consistent with the formula given in [46] that the noise response at double switching frequency is the same as the DC harmonic noise response. Unfortunately, for this hard-switching case, our Hspice simulation does not agree with our measurement as seen in Table 3.2 although simulations on $G_1/G_0$ are pretty good. It implies that LIN-OFF transition should be modeled by PWM model rather than our proposed AM model.

**Table 3.2** Comparison of LIN-OFF switching (Input: Sine Wave, VGS=1.6V)

<table>
<thead>
<tr>
<th>VPK(V)</th>
<th>Simulated gain at double switching frequency relative to gain @ DC ($G_1/G_0$) (dB)</th>
<th>Measured (same as theory in [46]) harmonic noise at double switching frequency relative to DC noise ($g_1/g_0$) (dB)</th>
<th>Simulated gain at switching frequency relative to gain @ DC ($G_1/G_0$) (dB)</th>
<th>Theoretical harmonic noise at switching frequency relative to DC noise ($g_1/g_0$) (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.2</td>
<td>-4</td>
<td>0</td>
<td>-19.1</td>
<td>-∞</td>
</tr>
<tr>
<td>1.4</td>
<td>-2.9</td>
<td>0</td>
<td>-23.1</td>
<td>-∞</td>
</tr>
</tbody>
</table>
It is worth pointing out that the transconductance linearization procedure of SpectreRF periodic-steady-state (PSS) simulation in Cadence is similar to our AM model. Darabi [46] also shows discrepancies between the theory, and the simulation results. The discrepancies tell us that simulations for PWM in both Hspice and SpectreRF are not so accurate as AM modulations since PWM is a kind of strong non-linear modulation, and linearization for periodic time-varying circuits is not so easily done in the simulators. However, it can be used to optimize the noise performance of the circuit because it can be approximated using an AM modulation when it is not so strong.

In conclusion, in most switching cases, it is possible to predict and optimize the flicker noise performance at the baseband and at the switching frequency using our AM flicker noise model, and flicker noise measurement is unnecessary.
3.3.4 An RF Application

Switching flicker noise has been studied under enough bandwidth. Combined with the linear filtering effect, it was modeled in the last section. However, high frequency switching such as found in an RF mixer is more common than low frequency switching. In this section, we will discuss how we apply our model to study and optimize the noise performance of the RF circuits.

For direct-conversion receivers, the mixer is the key component for directly converting the RF signal to a baseband signal. The flicker noise at the same frequency band is usually a serious issue which dominates the noise spectrum and severely degrades the noise performance. Noise analysis and optimization are extremely necessary.

The single-balanced Gilbert mixer is shown in Figure 3.20. Its noise performance is related to the total baseband noise at the output and the RF signal gain. For simplification, only flicker noise was considered. The flicker noise at the RF transconductance stage was upconverted and had no contribution at the baseband. Only switching transistors contribute flicker noise at the output. Therefore, the ratio of the flicker noise gain to the RF signal gain is the measure of the noise performance. The smaller the ratio, the better the noise performance. Using the proposed flicker noise model, the output noise will be the superposition of upconverted flicker noise at the switch gate input. The flicker noise gain was measured from the LO input to the mixer output with 0.1mV voltage source @ $f_{IF2}$ at the gate. Another voltage source with 0.1mV amplitude @ ($f_{LO} + f_{IF1}$) was injected at the gate of RF transconductance stage to measure the signal gain.

Firstly, the effect of the output bandwidth and switching frequency was studied. The transistors switch from the off state to the saturation region. The width of the switch transistor was used to change the output bandwidth and its effect on the input-referred flicker noise was not
considered. As shown in Figure 3.21, when the switching frequency is much less than the output bandwidth, the output flicker noise is switching frequency independent. This is consistent with what we observed previously. As the switching frequency increases, the linear filtering effect starts to play a role, and the output flicker noise gets larger and the signal gain becomes smaller. Subsequently the input-referred noise gets much larger. For better noise performance, higher output bandwidth or lower switching frequency is preferred.
The LO swing is another important factor. Figure 3.22 shows that the larger the LO swing, the better the noise performance. In this case, the on-state gate voltage almost keeps constant due to the fixed biasing current. The off-state gate voltage of the switch decreases with the swing. As mentioned before, to reduce flicker noise, a lower off-state gate voltage is needed. In other words, the large LO swing improves the noise performance.

![Figure 3.22. Effect of LO swing ($f_{LO}=500$MHz)](image)

The effect of the bias current of the mixer is also shown in Figure 3.23. Both the flicker noise gain and the RF signal gain increase with lowered bias current. The difference between them also increases. That means the smaller the current, the better the flicker noise performance. This is opposite to the thermal noise. Therefore, the bias current should be as small as possible as long as the thermal noise performance is satisfied.

Finally, we studied the effect of the transistor size of the switch. Since the input-referred flicker noise is inversely proportional to the transistor size, its effect on the flicker noise gain was incorporated. There is an optimal transistor width for the signal gain and the effective flicker noise keeps decreasing with the size, as shown in Figure 3.24. The output flicker noise
The larger the width of the transistor, the better the noise performance. However, when the width is too large, the output bandwidth effect will be dominant and the noise performance will become worse. Also, VCO cannot afford a very large capacitive loading. That is to say, the upper limit is bounded by the LO driving ability and the output.

Figure 3.23. Effect of bias current

Figure 3.24. Effect of transistor width of LO switch
3.4 Conclusion

In this chapter, we explored through measurements, the flicker noise mechanism under switching conditions. The noise spectrum analysis showed that under most switching conditions, baseband flicker noise is a superposition of upconverted gate flicker noise at each harmonic of the output current. For a non-linear circuit, flicker noise should be modelled as the noise voltage at the gate rather than as the noise current at the drain. The baseband flicker noise is independent of the input switching frequency when the switching frequency is greater than the corner frequency of the flicker noise and a sufficient output bandwidth is guaranteed. The slope of the noise spectrum becomes smaller compared to that in static DC bias conditions. Noise reduction methods were discussed. Switching flicker noise can be modelled using AM modulations for most kind of transitions and LIN-OFF should be modelled by PWM modulation. The model is validated by both simulation and measurements. The noise prediction and optimization of non-linear circuits by a simple simulation is possible. An RF application example, using the proposed model, was given to show the noise optimization for direct conversion receivers.
CHAPTER 4

DC Offsets and LO Leakage

Besides the flicker noise issue discussed in the last chapter, there are other big problems for direct conversion receivers, LO leakage and DC offsets. Issues related to these problems will be discussed in this chapter.

4.1 Introduction

The explosive growth in the demand for wireless products in recent years has resulted in intensifying efforts to develop single chip transceiver designs to reduce cost, power consumption and size. Of the many proposed architectures, direct conversion (homodyne) is perhaps the most promising architecture for low complexity, low power and low cost monolithic integration. Both unavoidable off-chip image rejection filters, and IF channel selection filters, in a heterodyne receiver are avoided by using a homodyne architecture. However, in a direct conversion topology the downconverted band extends to zero frequency, extraneous offset voltages and any low frequency noise can corrupt the signal and, more importantly, saturate the following stages. Therefore, flicker noise and DC offset have been recognized as the two most problematic issues for CMOS direct conversion receivers [57][58].

As shown in Figure 4.1, the isolation between the LO port and the inputs of the mixer and
the LNA is not infinite; that is, a finite amount of feedthrough, called ‘LO leakage’, exists from the LO port to the LNA input and mixer input. This effect arises from capacitive and substrate coupling and bond wire coupling if the LO signal is provided externally. This leakage is harmful for a homodyne receiver since the LO frequency is within the same RF signal band. Any leakage to the air will form an interferer to both itself and others. In addition, it is the main source of the time-varying dc offset as will be described in the following.

The leakage signal appearing at the inputs of the LNA and the mixer mixes with the LO signal, thus producing a DC component at mixer output. This phenomenon is called ‘self-mixing’. A similar effect occurs if a large interferer leaks from the LNA or mixer input to the LO port and is multiplied by itself. The resultant DC offset can be divided into a static and a time-varying component. Coupling of the LO to the LNA and RF port of the mixer causes static or fixed offset, also called ‘LO self-mixing’. When a strong interferer leaks from the RF to the LO port (interferer self-mixing) or the LO couplings to the antenna, radiates and then reflects off moving objects back to the antenna, a time-varying or dynamic offset is created in the mixer. However, both kinds of DC offsets originate from finite isolation between LO port and
RF signal port, so they are called the self-mixing problem.

Static DC offset also originates from other sources such as device mismatch. Although its impact can be minimized with the help of specific circuit design and layout techniques, mismatch itself can never be eliminated.

### 4.2 Self-Mixing

Dynamic DC offset is much more problematic than static DC offset and is more difficult to solve. Both existing solutions and a proposed solution are described in this section. Some methods can also be applied to static DC offset.

#### 4.2.1 The Severity of Self-mixing

To further appreciate how severe the self-mixing problem is, a rough numerical estimation is now given. The total gain of a receiver from the antenna to baseband output before ADC is typically around 80 to 100dB so as to amplify the microvolt input signal to a level that can be digitized by a low-cost, low-power ADC. Of this gain, typically 25 to 30 dB is contributed by the LNA/mixer combination. Suppose in Figure 4.1, the LO signal has a peak-to-peak swing of 0.63V (≈0dBm in a 50Ω system) and experiences an attenuation of 60dB as it couples to the LNA input port. If the gain of the LNA/mixer combination is 30dB, then the offset produced at the output of the mixer is in the order of 10 mV. Note that the desired signal level at this point can be as low as approximately 30µVrms [59]. There can be tens of dB larger than the real signal. Thus, if directly amplified by the remaining gain of 50 to 70 dB, the offset voltage saturates the following circuits, such as AGC, thereby prohibiting the amplification of the desired signal.

More seriously, self-mixing induced dc offset often varies with time. This occurs when the
LO signal leaks to the antenna and is radiated, and subsequently reflected from moving objects back to the receiver. For example, when a car moves at a high speed, the reflections may change rapidly. The bandwidth of this time-varying offset can be in the order of kilo-hertz for a rough calculation. In these conditions, it may be difficult to distinguish the time-varying offset from the actual signal.

The down-converted signal spectrum with, and without the time-varying offset, are shown in Figure 4.2. In order to get rid of time-varying DC offset and flicker noise, a high-pass-filter (HPF) is usually inserted between the downconversion mixer and the following stages. For the broad band signal, a smaller effect is expected since the percentage of energy loss is smaller than that of a narrow band signal. The higher the corner frequency, the better DC offset cancellation. However, the more the signal energy lost, the worse the bit-error-rate (BER) performance. Moreover, the steeper the filter slope, the better the receiver performance. However, if there is time-varying DC offset free with the circuits, then the high pass corner can be as low as possible and BER performance of the system will be improved significantly.

![Figure 4.2. Signal, DC offset, and filtering](image-url)
4.2.2 Existing Solutions and Discussions

As is obvious from the above discussion, offset cancellation solutions in a homodyne receiver should be found to avoid saturating downstream gain stages which desensitize the receiver and destroy performance. Approaches to remove the offset have so far mostly been focused on the following classes:

4.2.2.1. Post-processing based approaches – Dealing with the existing DC offsets

1. AC coupling. For modulation formats that have no or little spectral power at DC, AC coupling at the mixer output, or at some downstream stage, can be used to remove the offset. To avoid unacceptable distortion due to tracking the lower frequency spectrum of the signal, the AC coupling requires large capacitor values that are not realizable on-chip [78][79]. However, the spectrum of many commonly used signals exhibits a peak at the zero frequency; that is, the spectrum contains substantial energy (information) near dc. For a 200-kHz channel, if the high pass filter removes only the band from 0 to 20Hz, the bit error rate rises to above $10^{-3}$ [58], indicating the need for a very low corner frequency. In addition, the use of prohibitively large capacitor values often results in a failure to track fast variations in the time-varying offset voltage, performing only a coarse cancellation.

2. Autozeroing, correlated double sampling, or high pass filtering [60]. This usually works in a two-phase manner. During the sampling phase, the offset is measured and memorized. There then comes the cancelling phase during which the stored offset is subtracted from the signal. Most auto-zeroing circuits belong to this class. The sampling point can be after the mixer, after the AGC, or even after ADC. This depends on the magnitude of the DC offset and the requirements of the circuit blocks. The earlier the stage, the more relaxed requirement. However, the more severe the substrate noise effect and the more increased complexity.

3. Chopper stabilization [60]. This avoids DC offset and low frequency noise by up-con-
verting the signal to a safer frequency band, amplifying it, and down-converting it back to the base-band for further processing. This is called the chopper stabilization technique. Both solutions demand considerable amount of complexity and inevitably raise the white noise floor. These are the costs of an improved performance as the DC offset and flicker noise are now rejected.

4. Digital cancellation (Open loop). DC offsets are cancelled in the digital domain. This approach is often applied to the sampled signal before the decision device [61][62]. In this approach the offset is detected and removed digitally by time-averaging or by using more complex methods such as differentiating the received signal [61]. However, digital cancellation requires the analog baseband stages following the mixer to have enough spurious-free dynamic range (SFDR) to tolerate the DC offset. It also requires as many as five or six more bits in the ADC to achieve the same sensitivity and bit error rate (BER) when the offset is not present.

5. Digitally controlled analog cancellation (Feedback) [63]-[65]. Adaptive dual-loop cancellation is based on the Gilbert mixer combined with dual-loop algorithm. Offset are cancelled by dynamically varying the biased current on the loads which is designed to provide constant impedance independent of the load cancellation current with common mode feedback. The bias control is regulated via an adaptive dual-loop (gear-shifting) algorithm [64]. The offset is converted to the digital domain by ADC and processed by both coarse and fine offset cancellation filters and the output controls the DAC to vary the bias currents in the mixer load. This method can track the time-varying DC offset more quickly than previous two approaches since there are no large capacitors and the feedback point is the mixer itself which leads to shorter time delay. However, it is also not applicable to the signal spectrum which contains low frequency energy since it is also high-pass in nature. In addition, its complexity is high.
6. Non-linear cancellation with peak-detectors. Chen [66][67] proposed another possible DC offset cancellation method which need no AC coupling. It is easy to verify that for two equal-amplitude (sinusoidal) signals, the difference between their DC levels is equivalent to the difference between their envelopes. As the positive and negative components of a differential signal are of equal-amplitude in nature, a peak detector has the potential to function as an offset detector. The offset can then be subtracted off the signal easily. This approach is very similar to high-pass filtering but it is, intrinsically, a nonlinear process. They both have a slow response problem due to the very low corner frequency or large time constant requirement, and both cause finite low frequency power loss. But, due to the nonlinear operation of the peak detector, a higher harmonic distortion is expected. For a 4-FSK FLEX pager system, within one symbol period, the location of zero-crossings will be more or less altered but the total number does not change. The distortion, therefore, has only a limited impact on the demodulation. However, off-chip capacitors for peak detectors are still unavoidable.

4.2.2.2. System based approaches - The systematic avoidance and elimination

1. Coding or spectrum spreading. The baseband signal in the transmitter can be encoded so that, after modulation and downconversion, it contains little energy near the DC. This is called ‘DC-free coding’. This is particularly suited to wideband channels, for example, in DECT, where a few kilohertz of the channel can be wasted with no significant drop in the data rate. Wide-band spectrum spreading is a similar method used to reduce the high-pass effect on BER performance. It does not affect the BER very much if only a fraction of very wide-band spectrum is truncated such as wide-band CDMA applications [78]. These two approaches should be combined with the AC coupling approach.

2. Time division approach. It is to exploit the idle time intervals in digital wireless standards to carry out offset cancellation [57]. In a TDMA system, each mobile periodically enters
an idle mode so as to allow other users to communicate with the base station. This idle time can be used to measure the offset with a capacitor and subtract the value during the reception of the consecutive burst, introducing a virtually zero corner frequency during the reception of data. This approach only works if the offset can be assumed constant during the reception of at least two bursts. For a typical TDMA frame of a few milliseconds, offset cancellation is performed with sufficient frequency to take into account variations due to moving objects. However, while the timing of the actual signal (the TDMA burst) is well defined, interferers can appear any time. During the reception of a burst, the burst of an alien system can start. This causes a jump change in DC offset due to interferer self-mixing. Measuring the offset during idle time cannot therefore provide an accurate offset measurement. A possible approach to alleviate this issue is to sample the offset (and the interferer) several times and average the results. In addition, large capacitors are also unavoidable for noise consideration (kT/C noise).

3. Protocol based cancellation. DC offset is not simply a circuit issue but also a system-related problem. Therefore, other solutions should be sought in the system protocol and signal structures in the time domain [66].

4.2.2.3. LO based approaches – The reduction of self-mixing from the LO leakage side

1. Double LO frequency and local LO driver. The idea is that the integrated VCO operates at double the center frequency of the RF signal and is divided by two locally, followed by a LO buffer to drive the mixer so that there is less LO leakage to the air through the antenna. This alleviates the self-mixing problem [68]. However, the improvement is not good as expected because severe substrate coupling still leads to LO leakage from the local LO buffer, and interferer self-mixing due to other mobiles still exists.

2. Phantom oscillator topologies [69]. In this type of transceiver architecture, the effects of two or more spread-spectrum oscillators combine to produce a desired ‘phantom’ oscillator
useful for frequency translation. The phantom oscillator technique is particularly applicable to the up-conversion and down-conversion paths in integrated transceivers since spread spectrum oscillator leakage does not create problematic DC offsets. Any local oscillator leakage into the RF band appears as a spread spectrum signal to receivers; there is an inherent avoidance within the signal path of $1/f$ noise. Unfortunately, severe aliasing of unwanted signals into the desired signal’s spectrum can occur.

4.2.2.4. Mixer based approaches – The reduction of the self-mixing from the offset origin

1. Dynamic matching technique proposed by E. Bautista [71] in 2000. It is a kind of chopper stabilization technique combined with spectrum spreading which is applied on the mixer. Dynamic matching is utilized to mitigate circuit imbalances by frequency translating or frequency spreading the undesirable spectral components out of or within the frequency band of interest. The RF signal is first spread and sent to the Gilbert mixer switch core and, after down-conversion, it is despread back to the real IF signal. Note that this is done under the assumption that all imbalances and all non-idealities happen at the LO switch stage. For flicker noise this is true. Therefore, this approach has very good flicker noise suppression. However, for IP2 and DC offset, this may not be true. Bad IP2 is usually introduced by device mismatch at the RF transconductance stage which was not shown in [71]. The measured results were done using an ideal signal source. Results would be different in a real case in which RF transconductance transistors are used. Also any LO leakage to the RF input port will go through both spreading and despreading stages. Therefore, there would be not very much improvement for both the IP2 and DC offset. Furthermore, the circuit needs a low impedance voltage source to drive the mixer. This would consume a very large current. Maybe a source follower is needed to insert between LNA and the mixer. However, this would degrade the noise performance and increase the power consumption. Also a long spreading sequence needs to be created at moderate fre-
quency and its large swing may affect the LNA performance. Frequency planning may also be necessary.

2. Pulse-width-modulation based harmonic mixing. T. Yamaji [21][72] proposed a new kind of bipolar harmonic mixer based on pulse-width modulation. This is totally free from self-mixing and reduces the self-mixing induced DC offset down to the noise level. However, the mixer core cannot be directly applied to a CMOS counterpart due to different I-V transfer characteristics.

3. Multi-phase reduced frequency conversion technique [70]. The basic idea is that the effect of mixing the signal with a single-phase high-frequency periodic signal can be obtained by multiplying by a set of multiphase reduced-frequency periodic signals. To be specific, assuming sine signals in RF systems, the sine signal with frequency $\omega_{RF}$ is equivalent to N-phase low-frequency sine signals whose frequencies are $2\omega_{RF}/N$, as shown in the following equation. Therefore the LO signal of the conventional mixer can be constructed by several low frequency signals with different phases which are different from the center frequency of the RF input signal. There are no self-mixing problems. However, it is a little bit more complicated and self-mixing from the RF port to the LO port has not been eliminated for strong interferers.

$$\sin \omega_{RF} t = 2^{N/2} \prod_{k=0}^{N-1} \sin \left( \frac{2\omega_{RF}}{N} \cdot t - \frac{2k\pi}{N} \right)$$ (4.1)

In many applications DC offset cancellation costs so much in terms of induced substrate noise and complexity that people choose the more conventional and more mature superheterodyne architecture rather than direct-conversion. Moreover, as the major offset could appear at very early stages (i.e. the mixer output), circuits that can only cancel their own offsets do not help much. There are still other issues which limit the use of an offset cancelling approach.
Thus, the high cost and feasibility problem of offset cancellation explains why most, if not all, successful direct-conversion receivers are designed to handle only signals with negligible frequency components near zero frequency. It should also be noted that the problem of DC offset is much less severe in heterodyne architectures. Since the first LO frequency is not equal to the input carrier frequency, self-mixing may arise only for interferers, and dc offsets thus generated can be removed because the IF signals are far from zero frequency.

The first two groups of methods are little help in regard to time-varying DC offset since there is no step on self-mixing source. The other two groups are a little bit more complicated when put to a real use. There is an urgent need to find a new and simple solution.

4.2.3 Proposed Solution: Harmonic Mixing Principle

It is well known that the problem arises because the RF carrier and LO signal run exactly at the same frequency band, as shown in Figure 4.3(a). This can be overcome by using harmonic mixing as shown in Figure 4.3(b) in which the second harmonic of the LO signal takes part in the mixing process. As a result, LO leakage generates no DC component. The mixing output due to LO leakage is still situated at the LO frequency and can be easily filtered out. It is similar for RF leakage to the LO port. In other words, the conversion gain of the LO leakage is different from that of the RF signal since their conversion paths are different. However, they are exactly the same for the conventional mixer. Ideally, the LO leakage generates no baseband components and results in a zero conversion gain. However, due to device mismatch and other non idealities, there still can be very small portion of LO leakage which can be self-mixed.

Figure 4.4 shows the principle circuit of proposed harmonic mixer. The LO signal is converted from voltage to the current domain which contains the even harmonics of the LO frequency. The odd harmonics are cancelled. The current controls the mixer switches and
performs the downconversion. Since the switching process is done in the current domain, there is no coupling between RF port voltage and the switching current and, therefore, no self-mixing problem. Any RF/LO leakage will be mixed by its second harmonic.

In addition to being self-mixing free, the LO frequency is now half the RF signal frequency. There are several advantages in this. Firstly, the VCO can be realized more easily with a satisfactory phase noise at a low frequency since it is inversely proportional to the operating frequency. At the same time, power is saved. Secondly, the substrate coupling becomes smaller than before and has smaller effect on other circuits. Thirdly, any LO signal leakage to the air
will not be an interferer to others due to the half RF carrier and will be filtered by the antenna’s selectivity. However, the potential problem is a linearity problem as will be discussed in the next chapter because of a kind of current switching. When the switching current is smaller, the effective gate voltage is smaller too. Then linearity is degraded.

4.3 Static DC Offset

Static DC offset is mainly due to device mismatch. The input-referred offset voltage of a simple differential pair with resistive load is

\[ V_{OS} = \frac{V_{GS} - V_{th}}{2} \left[ \frac{\Delta R_L}{R_L} + \frac{\Delta (W/L)}{(W/L)} \right] - \Delta V_{th} \]  

(4.2)

A 10 mV level can be easily achieved. When a current mirror is used as the active load, the equation will be

\[ V_{OS} = \frac{V_{GS} - V_{th}}{2} \left[ \frac{\Delta (W/L)_L}{(W/L)_L} + \frac{\Delta (W/L)}{(W/L)} \right] - \frac{(g_m)_L}{g_m} (\Delta V_{th})_L - \Delta V_{th} \]  

(4.3)

Here the subscript “L” denotes the loading devices. The additional threshold voltage mismatch term and the usually worse (compared to the resistive load) active load dimension mismatch term results in an even larger offset component.

In addition to increasing the transistor size and the bias current, the first group of cancellation approaches discussed in Section 4.2.2 can be directly applied to static DC offset cancellation. With the help of our proposed harmonic mixing, the effective high pass corner can be set as small as possible so as to enlarge the system BER performance.

4.4 LO Leakage

LO leakage refers to the portion leaking to the air which, potentially, can be an interferer to
other mobiles for conversional receivers. It is mainly due to substrate coupling and parasitic
coupling from the LO. However, if a harmonic mixer is used, this will be no longer a problem
since it is out of the RF signal band.

4.5 Conclusion

LO leakage and the DC offset problem were discussed. Using the proposed harmonic mix-
ing, both LO leakage and the self-mixing induced DC offset problem have been solved sucess-
fully. Combined with static DC offset cancellation, harmonic mixing would be a versatile
solution for direct conversion receivers.
5
CMOS Harmonic Mixer

In the last chapter, self-mixing induced DC offset was solved, in principle. In this chapter we introduce the circuit implementation of a new kind of CMOS harmonic mixer based on the harmonic mixing principle.

A 900MHz balanced harmonic mixer for direct conversion receivers was fabricated in a 0.35 µm standard digital CMOS process. The self-mixing-induced DC offset is about 44dB lower than that of the conventional mixer. The input-referred offset is reduced to the noise level. Specific techniques of flicker noise reduction are also discussed in this chapter. At 3V power supply and -15.4dBm LO power, it achieves a 13dB conversion gain, 24.5dB noise figure at 10 kHz, 14.8dB noise figure at 1MHz, -10dBm third-order input intercept point and +36 dBm second-order input intercept point. The total power consumption is about 5mW.

5.1 Introduction

In recent years direct conversion architecture has gained much attention as a possible solution for a single-chip radio due to its low power, low complexity and easy-to-integrate properties. However, there are various design issues to be resolved, of which the DC offset generated by self-mixing is the most critical [57], [58]. Efforts to solve the problem have been reported,
and different solutions, varying from DSP-based offset cancellation algorithms to RF front-end design techniques, have been introduced. As most modulation schemes contain significant DC and low frequency components, base band offset cancellation is generally not a viable option, especially in the case of narrow band modulation. The bipolar balanced harmonic mixer proposed by T. Yamaji [21] has the ability to reduce the offset down to the noise level. Nevertheless, no CMOS mixer which solves the self-mixing problem has been reported in the literature. The dynamic matching technology proposed by E. Bautista [71] helps improve IIP2 and reduces flicker noise, but the self-mixing problem still exists and the circuitry is much more complicated.

In this chapter, a novel CMOS harmonic mixer with a unique working principle for DC offset and flicker noise reduction is introduced. In the following section the circuit implementation of the mixer is described. The theoretical analysis is presented in section 5.3. Experimental results are then given in section 5.4. Finally, a discussion on linearity improvement and flicker noise reduction is provided in section 5.5, followed by the conclusion.

5.2 Circuit Implementation

A CMOS balanced harmonic mixer which achieves a performance comparable to that of the bipolar version is shown in Figure 5.1. The second harmonic is easily obtained because of the inherent square-law operation of the CMOS transistor. The LO stage is actually a frequency doubler which converts the differential LO voltage to a time-varying current which only contains even harmonics of the LO frequency.

Figure 5.2 gives the time-varying current-controlled transconductance. The second harmonic of the LO signal can be seen clearly. Unlike conventional switches, the transconduct-
tance is controlled by the current rather than the voltage. This avoids the direct coupling from the LO stage to the RF stage which is the origin of the self-mixing. In principle, the fundamental and all odd harmonics of the LO are cancelled out at the connected drain terminal and the DC offset problem is mitigated.

![Figure 5.1. Principle CMOS harmonic mixer](image)

Both the DC offset and flicker noise are big concerns in CMOS direct-conversion receiv-
ers. Unlike traditional pager receivers that are based on the POCSAG protocols, the newer FLEX receiver uses 4-FSK and not 2-FSK. The result is a higher bandwidth efficiency but the signal has significant DC components. For MOS transistors working in the saturation region, the corner frequency of the flicker noise can be as high as hundreds of kHz. In the FLEX paging receiver where the band of interest is only at tens of kHz range, the $1/f$ noise and DC offset corrupt the signal, and the result is an unacceptable sensitivity.

To better understand the $1/f$ noise issue in the MOSFET, some separately laid out transistors were fabricated in the same run for testing purposes. The experimental results in Figure 3.3 show that there is a minimum point for input-referred flicker noise. This is consistent with [40]. However, when the transistor size is increased, it is found that the optimal point moves towards the weak inversion region. To reduce flicker noise, the RF part can be biased near this region. At a biasing current, a larger W/L ratio drives the device toward the moderate or weak inversion region. This is very different from conventional mixers and it offers the following advantages: the gain is increased because transconductance increases with the W/L ratio and the maximum value will be achieved in this region; the thermal noise is decreased; the $1/f$ noise also decreases because of the large transistor size and the optimal bias region; the inductive load of LNA is smaller; and the $f_T$ of the device, as shown in Figure 5.3, does not degrade very much in this region. The lower $1/f$ noise in the mixer helps relax the gain requirement of the LNA and is good for the linearity improvement of the RF front-end. However, this leads to a certain linearity degradation of the mixer itself. A kind of noise-linearity trade-off exists.

The complete harmonic mixer is shown in Figure 5.4. The LO stage is a frequency doubler. Any mismatch at this stage will lead to an uncanceled LO fundamental component in the current which will mix with the LO leakage and, therefore, degrade the self-mixing suppression performance. To minimize mismatch, transistors were carefully laid out with multi-fingered
structure. The RF part is a differential pair the transconductance of which is controlled by the current from the doubler. There is no coupling between the RF port and the current which contains the second harmonic of the LO signal. Polysilicon resistors were used instead of active loads for better matching, linearity, lower noise and a CMFB-free implementation. An improved-cascode-type current source was used to increase the output impedance and output swing. In addition, the smaller transistor size for the current source was chosen to reduce the parasitic capacitor at the injection node.

![Figure 5.3. $f_T$ of Long channel and short channel device](image)

![Figure 5.4. Current injection method](image)
The current injection method was utilized to reduce the flicker noise. The injected current $I_0$ reduces the current in the two upper transistors driven by the RF input and pushes them to the optimal bias region. With the current injection, the RF gain (RF/BB) increases, the DC gain (RF feedthrough BB/BB) decreases. Therefore, the input-referred noise improves significantly without any increase in power consumption. The injected current itself does not introduce any noise in this balanced structure. Unlike the normal Gilbert-type mixer, the two RF transistors change their currents simultaneously and any noise at their common source node is completely cancelled out at the differential output. At the same time, the load of the mixer is increased to raise the mixer conversion gain. The method is compatible with the low voltage application as there are only three stacked transistors. With the help of the injected current, more than 20dB noise improvement is achieved.

5.3 Performance Analysis

To gain a deep insight into the harmonic mixing mechanism and circuit design, a theoretical analysis was performed. The long channel square-law large signal current model shown in (5.1) is assumed.

\[ I = \frac{\mu C_{ox} W}{2L} (V_{gs} - V_{th})^2 = k \Delta V^2 \]  

where $k$ is the current coefficient, $k=\mu C_{ox} W/(2L)$, $\Delta V$ is the effective gate voltage.

Assuming that LO signal $v_{lo}=a_{lo} \cos(\omega_{lo}t)$, it can be derived [see Appendix] that the time-varying transconductance in RF stage equals

\[ G_m(t) = a_{lo} \cdot \frac{k_{rf}k_{lo}}{2} \sqrt{x_0 + \cos 2\omega_{lo}t} \]  

1. Please see Appendix I for detailed formulation.
where $a_{io}$ is the applied differential LO amplitude, $k_{rf}$ and $k_{lo}$ are the current coefficients of transistors in RF and LO stage respectively as defined in (5.1), $x_0$ is expressed by

$$x_0 = 1 + \frac{8k_{lo}\Delta V_{lo}^2 - 4I_0}{k_{lo}a_{io}^2} \tag{5.3}$$

where $\Delta V_{lo}$ is the effective gate voltage of LO part. As shown later, $x_0$ is an important parameter which controls the signal gain, linearity and noise performance. It can be adjusted by the aspect ratio of LO stage, LO amplitude, effective gate voltage of LO stage and the injected current.

Using Taylor’s expansion, it is observed that the output spectrum contains $f_{rf} \pm 2n f_{lo}$ harmonic components, where $n=0, 1, 2, \cdots$. The signal gain of the harmonic mixer $G_{f_{rf} \pm 2n f_{lo}} (n=1)$ is given by

$$G_{f_{rf} \pm 2n f_{lo}} \approx a_{io} R_L \cdot \frac{k_{rf} k_{lo}}{2} \cdot \frac{1}{4 \sqrt{x_0}} = \frac{a_{io}^2 R_L}{4 \sqrt{a_{io}^2 + 8\Delta V_{lo}^2} - 4I_0} \cdot \frac{k_{rf} k_{lo}}{2} \tag{5.4}$$

It is inversely proportional to $x_0$ and increases with LO amplitude $a_{io}$, the load $R_L$, and the injected current $I_0$. To have a sufficient gain with a specific LO power requirement, a large $W/L$ ratio up to 2000 was chosen for the RF stage transistors. The minimum gate length was chosen. Such a large transistor size also lowers the flicker noise. For the LO stage, proper transistor size needs to be selected to satisfy the LO loading and bandwidth requirements.

The DC gain $G_{f_{rf}} (n=0)$ is

$$G_{f_{rf}} = a_{io} R_L \cdot \frac{k_{rf} k_{lo}}{2} \cdot \sqrt{x_0} = R_L \sqrt{a_{io}^2 + 8\Delta V_{lo}^2} - \frac{4I_0}{k_{lo}} \cdot \frac{k_{rf} k_{lo}}{2} \tag{5.5}$$

Opposite to the signal gain $G_{f_{rf} \pm 2n f_{lo}}$, the feed-through gain $G_{f_{rf}}$ is proportional to $x_0$. Note that output bandwidth of the mixer is not considered. The RF signal can feed through directly to the
mixer output and is filtered out by the low pass characteristics at the output and low pass filter in the following stage. However, noise components at low frequency are amplified directly to the output.

To lower the noise, this DC gain should be set as small as possible. The input-referred noise is calculated by referring total output noise to the RF input port. Therefore the ratio of this DC gain to the signal gain largely reflects the level of input-referred noise. It is approximately proportional to $x_0$ as shown in the following equation,

$$\frac{G_{rf}}{G_{rf-2f_{lo}}} \approx 4x_0$$  \hspace{1cm} (5.6)

The smaller $x_0$, the larger the signal gain, the smaller the DC gain, and the better the noise performance. However, the linearity may degrade a certain amount.

The self-mixing induced DC offset suppression is evaluated by the conversion gain ratio of the RF signal and the LO leakage to the base band. For a conventional mixer, the ratio equals the unity. For this harmonic mixer, ideally, the gain of LO leakage to the baseband output is zero. However, due to an unavoidable mismatch at the LO stage, an LO fundamental frequency exists in the frequency doubler output current. It mixes with the LO leakage at the RF input and creates a small DC offset. The offset rejection is defined as:

$$R_{offset} = \frac{G_{rf-2f_{lo}}}{G_{LOleakage-flo}} = \frac{SignalGain}{LOleakageGain}$$  \hspace{1cm} (5.7)

The larger the ratio, the better the offset suppression performance.

The input-referred IP3 of the mixer is approximately given by

$$IIP3 \approx 10 + 20\log\left(a_{lo} \frac{x_0}{3} \cdot \frac{k_{lo}}{k_{rf}} \cdot \frac{4 - \frac{17}{32x_0^2 + 5}}{x_0}\right) \text{ dBm}$$  \hspace{1cm} (5.8)

The effect of the drain voltages of RF stage transistors is not considered here. It is clear that
the linearity degrades when $x_0$ decreases. Figure 5.5 shows the calculated linearity versus the injected current and LO power according to the above equation. It degrades with the injected current due to lowered effective gate voltage. The large LO amplitude helps improve the linearity. The penalty is that more DC current is created in the frequency doubler and this leads to a larger power consumption. There is a trade-off between linearity and power.

\[ \text{NF} = 10 \log \left( 1 + \frac{2R_L(\gamma G_{fj} + 1) + \frac{G_{fj}^2 K_f}{2KT(WL)r_fC_{OX}}}{G_{fj-2f_0}^2 R_s} \right) = 10 \log \left( \frac{8x_0^2 K_f}{KT(WL)r_fC_{OX}R_s} \right) \] (5.9)

Where flicker noise dominates and other noise contributions such as noise from $R_s$ and $R_L$ are ignored. $K_f$ is flicker noise coefficient, $\gamma$ is thermal noise coefficient and $K$ is Boltzmann’s constant. Since the transistors at RF stage switch simultaneously, noise from the LO stage and the current source become common mode signals, and are cancelled at the differential output. Only the transistors of the RF part and resistor loads contribute noise. Unlike the usual Gilbert-
type mixer, the RF part of the harmonic mixer works in current switching and always operates in the saturation region. Section 3.3 shows that the flicker noise coefficient keeps almost constant when the transistor switches from saturation region to saturation region. A very large device is good for small $1/f$ noise. The PMOS device has smaller flicker noise than the NMOS and can be used for better flicker noise performance with a compromise in gain. It can be seen that the noise figure largely depends on the parameter $x_0$. To improve the noise figure, $x_0$ should be set as small as possible, as long as the linearity requirement is satisfied.

5.4 Experimental Results

Figure 5.6 shows the mixer measurement setup. A differential dynamic signal analyzer, SR780 [55], was used to measure the signal and noise spectrum. The low frequency buffer was fabricated together with the mixer on the chip, and one individual buffer was also fabricated for deembedding and calibration using equations for cascaded circuits [59].

![Measurement setup](image)

Figure 5.6. Measurement setup

Figure 5.7 shows the mixer conversion gain and the offset rejection ability. When measur-
ing the LO leakage gain, a signal near LO frequency rather than RF frequency was used as the input. When the LO power increases, the contribution of the device mismatch becomes less, and there is more improvement in the offset cancellation. As predicted by the formula in the above section, signal conversion gain improves with LO input power due to increased current. At -15.4dBm LO power delivered to each side of the LO port, 37.5dB offset rejection is achieved. With lower LO frequency, harmonic mixing also renders higher LO to RF port isolation. Assuming a 20dB per decade roll off, a 6dB improvement can be gained. With this advantage, the offset performance of our mixer is 43.5 dB better than that of a conventional mixer. More improvement is achieved with an integrated differential local oscillator. More than 50dB LO to RF port isolation at 450MHz under different bias conditions was measured. Assuming the worst case 50dB isolation, with -15.4dBm LO input, the effective DC offset at the input of the mixer is about -96.9dBm, almost the same as the noise level within 25kHz channel bandwidth if LNA provides 20dB gain and 5dB noise figure.

![Figure 5.7. Offset cancellation](image)

In Figure 5.8 the conversion gain with respect to the injected current and LO power is plotted. The RF gain increases with the injected current until the device is pushed into the weak
inversion where the square-law relationship does not hold any longer. The maximum value can be achieved by tuning the injected current. Moreover, the higher the LO power, the larger the conversion gain.

![Figure 5.8. Conversion gain](image)

However, the linearity degrades with the injected current, as shown in Figure 5.9 and Figure 5.10. This is due to the lowered effective gate voltage of the RF stage and the smaller voltage drop at resistor load. This is consistent with our prediction in Figure 5.5. When LO power increases, linearity also degrades. This differs from the prediction. This is because the voltage drop on the resistor load increases with LO power and the headroom for the transistor to stay in the saturation region becomes smaller. However, this effect is not considered in (5.8). This can be improved by using higher power supply. There are trade-offs between conversion gain or noise and linearity. To have a large gain and good noise performance, a large LO power and a large injected current are needed. However, the linearity suffers. Fortunately, most receivers use frequency or phase modulation. Therefore, the linearity requirement is not so stringent and some compromises can be made.

The measured input-referred IP2 and IP3 under the best noise performance are shown in
Figure 5.11. IIP2 is important for direct conversion receivers. In addition to well-matched devices using a dedicated layout, the performance could be further improved by adding some auxiliary circuits to compensate for the mismatch as done in [72].

The noise performance of the harmonic mixer is depicted in Figure 5.12. As predicted by the formula, with the current injection technique, the noise is greatly reduced. This is due to a lowered flicker noise level in the moderate inversion region and the smaller $x_0$ which is
reduced by the injected current. Increased LO power also greatly improves noise performance because $x_0$ decreases with LO amplitude and the conversion gain increases with the LO power.

The output noise power spectrum density is shown in Figure 5.13. Flicker noise is obviously dominant at a low frequency band. The noise flattens out at high frequency due to the increased portion of thermal noise. For direct-conversion applications, flicker noise is not avoidable, while only the thermal noise performance of the mixer is usually reported in other
applications. At frequencies as low as 10kHz, 24.5dB NF is achieved for this mixer. This is much better than conventional CMOS mixers [46].

Unlike conventional mixers, the power consumption of the harmonic mixer varies with LO power because the LO contributes part of the DC current as a result of the square law relationship. Figure 5.14 gives the mixer current consumption levels in different LO power conditions.

The die photo of the CMOS harmonic mixer is shown in Figure 5.15 and its performance is
summarized in Table 5.1. Figure 5.16 shows the photo of the buffer for calibration after the mixer.

<table>
<thead>
<tr>
<th>Table 5.1</th>
<th>Summary of measured NMOS harmonic mixer</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power supply</td>
<td>3V</td>
</tr>
<tr>
<td>Single-ended LO power</td>
<td>-15.4dBm</td>
</tr>
<tr>
<td>LO frequency</td>
<td>450MHz</td>
</tr>
<tr>
<td>RF frequency</td>
<td>900.05MHz</td>
</tr>
<tr>
<td>Conversion gain</td>
<td>13dB</td>
</tr>
<tr>
<td>1dB compression point</td>
<td>-19.9dBm</td>
</tr>
<tr>
<td>IIP3</td>
<td>-10.6dBm</td>
</tr>
<tr>
<td>IIP2</td>
<td>+35.7dBm</td>
</tr>
<tr>
<td>Noise figure @10KHz</td>
<td>24.5dB</td>
</tr>
<tr>
<td>Noise figure @1MHz</td>
<td>14.8dB</td>
</tr>
<tr>
<td>DC offset rejection</td>
<td>37.5dB</td>
</tr>
<tr>
<td>DC current</td>
<td>1.72mA</td>
</tr>
</tbody>
</table>

Except noise performance at very low frequency, the results meet the requirements for the direct conversion FLEX paging receiver, which were derived in a previous work [73]. Note that flicker noise was not considered in that simulation. Some trade-offs of different specifications need to be done for a real CMOS implementation.
5.5 Discussion

The proposed harmonic mixer has a superior DC offset immunity but a inferior linearity. The dynamic range of the overall receiver might suffer. A special double balanced structure [67] which cancels more intermodulations helps improve the linearity. However, the power dissipation and the noise doubles. Source degeneration with paralleled resistors and capacitors may help. In addition, RF/IF isolation also could be improved. A larger power supply could be a possible solution too. Designers can trade-off these specifications. For the targeted paging receiver [73], the linearity is not a stringent requirement and the result is still satisfactory.

The author would also like to point out that there are other possible schemes which would be implemented to reduce the flicker noise in CMOS technology. One option is to make use of lateral bipolar transistors [74]. The $f_T$ of this kind of transistor becomes a little worse due to the large parasitic capacitance at the base, but the corner frequency can be below 1kHz. $4\text{GHz}f_T$ is achieved from the measurement on the same chip. Combined with this work or [21], both the DC offset and the flicker noise problems would be solved.

While it is not possible in the paging application, certain system changes could also help.
From a system perspective, if a sufficiently high bandwidth was used for the offset cancellation loop, the flicker noise and DC offset problems would be largely overcome. Certainly, if one can use a DC-free coding of a modulated signal, the problem mentioned above could be greatly alleviated. The by-product is usually a reduction in bandwidth efficiency, however.

5.6 Conclusion

In conclusion, the proposed CMOS harmonic mixer achieves the goal of DC offset free with the additional advantages of low complexity, low power consumption, and low LO driving power. Two main problems in direct conversion receivers are alleviated. It is suitable for low cost highly integrated direct conversion receivers.
Lateral Bipolar Harmonic Mixer

A CMOS harmonic mixer for direct-conversion purpose was proposed in the last chapter. However, the noise performance dominated by flicker noise means that it is not possible to put into a practical usage. In this chapter, a possible solution to overcome this problem will be described.

A lateral bipolar harmonic mixer for direct-conversion receivers was proposed and fabricated in a CMOS process. It is immune from both flicker noise and self-mixing induced DC offset. Using the lateral bipolar transistor and the harmonic mixing technique, it achieves a +15dB gain, 17.8dB NF at 10kHz frequency, -8.2dBm IIP3, +44dBm IIP2 and more than 30dB DC offset suppression. It only consumes 2.2mW power at 3V.

6.1 Introduction

The semiconductor industry continues to challenge analog and RFIC designers with a demand for higher performance and better compatibility with the digital world. It is desirable to use a single mainstream digital CMOS process for all IC products, especially for a system on a single chip. To achieve the highest integration, direct conversion for the analogue part is the most expedient candidate of all architectures because of its simplicity, image-rejection-free
and low power operation.

However, the design of CMOS direct-conversion transceivers entails many difficulties: self-mixing induced DC-offset, flicker noise, even-order distortion, I/Q mismatch, and so on [57]. The first two are the most problematic. The DC-offset can be as large as 10mV at the mixer output while the desired signal level can be only tens of µVs. Thus, the offset voltage saturates the circuits following the mixer, thereby prohibiting the amplification of the desired signal. As for the flicker noise, it not only degrades the noise performance of mixers and the phase noise of oscillators, but also adds noise directly to the baseband at the output of the mixer. As most modulation schemes contain significant DC and low frequency components, baseband offset cancellation is generally not a viable option, especially in the case of narrow-band modulation. Therefore, the bottleneck is in the mixer and a solution regarding this component should be sought. A good mixer can solve almost all the problems associated with direct conversion architecture.

The dynamic matching technology proposed by E. Bautista [71] helps improve IIP2 and reduce flicker noise but it is very complicated and is not suitable for low voltage operations. Zhang [44] solves the DC offset problem, but the noise performance is still not satisfactory due to the intrinsic flicker noise associated with MOS devices.

Lateral bipolar transistors are important for CMOS based technology because they can be easily integrated into the process to achieve a BiCMOS technology without added cost. Therefore, the lateral bipolar is a good candidate for lowering the flicker noise [75].

In this chapter, a novel harmonic mixer based on lateral bipolar devices to solve flicker noise and the DC-offset problem is introduced. Firstly, a lateral bipolar transistor was characterized. Using this device, a mixer based on harmonic mixing was built and measured. IIP2 improvement is discussed. Finally a conclusion is drawn.
6.2 Lateral Bipolar Transistor

There are two kinds of lateral BJT available, the pure bipolar [75] and the hybrid device [76]. The hybrid BJT has a very large common-emitter current gain. However, flicker noise still exists because the internal MOS device is still on. For the pure bipolar device, the MOS transistor is switched off completely so it is flicker noise free. Typically, the corner frequency of flicker noise is lower than 100Hz.

In a bulk n-well CMOS process, only a lateral p-n-p (LPNP) can be constructed. The n-well serves as the base, and the minimum polysilicon gate length sets the base width. A p-diffusion emitter is surrounded by a p-diffusion lateral collector. To reduce the unavoidable parasitic vertical collector current, the transistors are laid out as multi-emitter devices [75], in which each emitter is a minimum area p-diffusion contact surrounded by a polysilicon gate as shown in Figure 6.1. By doing this, the ratio of lateral collector current to vertical parasitic collector current is maximized and the lateral collector current efficiency is improved. Each device is surrounded by a p+ substrate guard ring to provide the sinking ground for the parasitic current. The die photo of the device is shown in Figure 6.2.

![Figure 6.1. Layout and symbol of minimum lateral bipolar transistor cell fabricated in a bulk CMOS process.](image-url)
Physically the LPNP can be modelled using one lateral bipolar transistor and two vertical bipolar transistors paralleled with a PMOS transistor (Figure 6.3). To have a pure bipolar action to eliminate the flicker noise, the gate is zero-biased with respect to the emitter to prevent M1 from turning on. Both junctions of Q3 are reverse-biased, so this device is also off. However, it is impossible to directly measure the internal currents flowing in each device [77]. Using the assumption that the base currents of the internal lateral and vertical bipolar transistors are the same, it becomes possible to derive both the lateral and vertical $\beta$ required for the model.

![Figure 6.2](image.jpg)

**Figure 6.2.** Die photo of the device.

![Figure 6.3](image.jpg)

**Figure 6.3.** Model of lateral bipolar device. Normal pure BJT operation: M1, Q3 OFF; Q1, Q2 ON.

The $I_c-V_c$ characteristics of the lateral BJT in a common emitter configuration with an
0.35μm base width can be seen in Figure 6.4. The Early voltage is around 10V. The Gummel plot showing the collector $I_c$, base $I_b$, and substrate $I_{sub}$ currents for the same device is presented in Figure 6.5. For low collector current levels, an ideal exponential current-voltage behavior is observed (i.e., 60mV/decade). This indicates that the dependence of $I_c$ on $V_b$ is similar to that of a conventional BJT. Since the thickness of the n-well is much larger than the minimum gate length, the vertical substrate current is much smaller than the lateral collector current.

![Figure 6.4. I-V curve of lateral bipolar device.](image1)

![Figure 6.5. Gummel plot of the lateral bipolar transistor.](image2)

Figure 6.6 shows the lateral $\beta$, vertical $\beta$ and the current efficiency $\eta$. At low current densi-
ties, lateral $\beta$ is as high as 500. High level injection leads to the $\beta$ roll off. At the mA range of the collector current, it is larger than 40 which is still large enough for the applications. Vertical $\beta$ is much flatter and smaller than the lateral one due to a larger base width. When the current $I_c$ is within a useful range, the lateral efficiency is larger than 0.6. This represents a significant improvement over the typical lateral efficiency of 0.25 to 0.50 [75].

![Graph of current gain $\beta$ and lateral efficiency of the device.](image)

The ac characteristics of the Lateral BJT device are also measured and the $f_T$ of the lateral bipolar is around 4GHz at 1mA. The $f_T$ can be largely improved with a silicided process and a smaller minimum gate length.

### 6.3 Harmonic Mixer

The conventional CMOS Gilbert mixer has a large gain and good linearity but has a bad flicker noise performance and an inherent self-mixing problem. A CMOS harmonic mixer was proposed by Zhang [44] to solve the self-mixing induced DC offset problem. It utilizes the LO’s harmonics to mix down the RF signal. Any LO leakage to the RF port is mixed by the second harmonic of the LO to the same LO frequency and it is filtered out at a later stage. The-
oretically no DC offset is created. However, its noise performance is still greatly degraded by severe flicker noise. To eliminate the effect of flicker noise, lateral bipolar devices were used to replace MOS transistors at the RF stage of the mixer as shown in Figure 6.7. The LO stage (m1, m2) has no flicker noise contribution at the mixer output due to the noise upconversion and common-mode operation while RF stage (q1, q2) has a very low flicker noise corner due to the bipolar mode. Consequently, the new harmonic mixer is flicker-noise-free and DC-offset-free. The current source was introduced to further improve the noise performance.

![Proposed harmonic mixer circuit.](image)

To measure the mixer performance accurately, the mixer is followed by an on-chip PMOS buffer which has a smaller flicker noise effect than does the NMOS one. The same buffer was fabricated separately on the same die and measured for calibration and deembedding. It has 7.8 dB gain and +6dBm IIP3. The mixer performance next reported on excludes the buffer except the noise figure.

The RF signal gain is depicted in Figure 6.8. Given the same bias current, a bipolar device gives a larger transconductance than an MOS transistor. Therefore, the mixer achieves a larger signal gain than do conventional MOS mixers. As the LO power increases, the gain increases dramatically due to increased time-varying transconductance. An increased injected current
leads to the gain decreasing due to larger transconductance clipping when a smaller LO power is applied. However, when the LO power is large enough, the injected current helps increase the gain.

Conventional mixers have no DC-offset suppression ability because the LO leakage and RF signal lie in the same frequency band and their conversion gains are the same. But, in the harmonic mixer presented in this chapter, they belong to different frequency bands and have different conversion paths and different gains. For the RF signal, the signal is mixed by the second harmonic of the LO. The LO leakage is mixed by the LO itself. If the transistors at the LO stage are exactly the same and if the inputs are exactly differential, there is no LO frequency component created in the time-varying transconductances and the gain of LO leakage is zero. But device mismatch is unavoidable. It can be seen from Figure 6.9 that more than 30dB DC-offset suppression is achieved. The output spectrum was measured at the buffer output.

The noise performance is shown in Figure 6.10. The minimum noise figure at 10kHz is below 18dB, while a Gilbert mixer gives around 30dB NF at this frequency. There is a 10dB improvement compared to [44]. The larger the LO power, the larger the transconductance, and the better the noise performance. Current injection also improves the noise at a large LO power.

Figure 6.8. Measured mixer gain.
since the RF gain increases while the DC component of time-varying transconductance decreases.

Figure 6.10. Measured spot noise figure at 10kHz.

Figure 6.11 shows the linearity performance. The larger the LO power, the worse the linearity. There is a trade-off between the linearity and the signal gain or the noise performance.

The input-referred IP2 is very important for direct conversion applications. Two high-frequency interferers can generate a low frequency beat in the interested band in the presence of even-order distortion. Any asymmetry in the RF stage of the mixer may lead to the degradation
of the IP2 performance. In order to compensate for the device mismatch in the RF stage, different DC biases were applied to the differential RF port separately. As seen from Figure 6.12, if this is not done, only +18dBm IIP2 is obtained. After mismatch compensation, more than +40dBm IIP2 is achieved. The bias voltage difference is within several mVs. The spectrum was measured at the buffer output.

Figure 6.11. Measured input-referred IP3 performance.

Figure 6.12. Two-tone test: before and after device mismatch compensation at RF stage. IIP2 is greatly improved. Pin=-33dBm.

A possible bias circuit on IIP2 improvement is shown in Figure 6.13. Both external tuning and digital tuning are possible. By controlling digital pin S1, S2, S3 and analogue pin Vctrl, the bias voltage to the RF input port VRF+ and VRF- are different. It is worth pointing out that
it is possible to use analogue control Vctrl to realize auto-IIP2 calibration through feedback information from the mixer output.

![Figure 6.13. Possible bias circuitry for IIP2 improvement.](image)

The overall mixer performance is summarized in Table 6.1 and the die photo is presented in Figure 6.14. At a +3V power supply, the mixer achieves 15dB gain and only consumes 2.2mW. The input RF bandwidth is larger than 300MHz. It can be further improved by reducing the size of the lateral bipolar devices.

<table>
<thead>
<tr>
<th>Table 6.1</th>
<th>Mixer performance summary</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>TSMC 3M2P CMOS0.35µm</td>
</tr>
<tr>
<td>VDD</td>
<td>3V</td>
</tr>
<tr>
<td>Signal gain</td>
<td>+15dB</td>
</tr>
<tr>
<td>DC offset suppression</td>
<td>&gt; 30 dB</td>
</tr>
<tr>
<td>Noise figure @ 10kHz</td>
<td>&lt; 18dB</td>
</tr>
<tr>
<td>1dB compression point</td>
<td>&gt; -20dBm</td>
</tr>
<tr>
<td>Input referred IP3</td>
<td>&gt; -9dBm</td>
</tr>
<tr>
<td>Input-referred IP2</td>
<td>&gt; +40dBm</td>
</tr>
<tr>
<td>Power consumption</td>
<td>&lt;2.2mW</td>
</tr>
</tbody>
</table>

### 6.4 Conclusion

A high-gain low-power harmonic mixer in a CMOS process was fabricated using lateral bipolar and harmonic mixing techniques. Both flicker noise and self-mixing induced DC offset
were circumvented successfully. It is suitable for low power and low cost direct-conversion receivers.

*Figure 6.14.* Die photo of LBJT harmonic mixer
Direct Conversion Pager Receiver

Direct-conversion, while having the potential of achieving high integration and low cost, is plagued by various issues ranging from DC-offset and flicker noise as discussed in the early chapters. While most of the recent integrated single-chip direct conversion receivers have focused on wideband applications in which flicker noise and DC offset can be filtered out without affecting the performance [78][79], we, in our research, focused on a narrow band application using CMOS technologies. In this chapter an effort to fully integrate an RF and baseband modulation circuitry for a narrow band application such as a high speed pager which uses a 4-FSK modulation scheme is discussed. The receiver described here, using a harmonic mixing technique and a baseband DC-offset cancellation scheme, successfully overcomes the problems.

The application background will be first introduced. In Section 2 the implementation of the building blocks is discussed. The measurement results are presented in section 3. Finally, a conclusion is drawn.

7.1 Introduction

The growing demand in recent years for wireless products has resulted in intensive efforts
to develop single chip transceivers in order to reduce cost, power dissipation and chip size. Of all the possible architectures, direct conversion is the most promising one for low complexity, low power and low cost single chip integration [80][81]. However, it is plagued by the problem of large, time-varying offsets that are induced by self-mixing in the mixer. Self-mixing arises from insufficient on-chip isolation between the LO port of the mixer and the RF input port of LNA and the mixer. In addition to the static DC offset introduced, a time-varying or dynamic offset is also created when a time-varying strong interferer leaks to the LO port of the mixer or the LO leakage radiates and reflects off the moving objects back to the antenna. This changing offset is unpredictable and very difficult to get rid of. The magnitude of the offset created at the mixer output can be several tens of dB larger than the desired signal level. This may greatly degrade the receiver BER performance, especially in those kind of modulation schemes which contain significant energy at or near the DC component.

With the rapid growth of new paging markets, the FLEX\(^1\) protocol was developed to replace POCSAG\(^2\) for a more efficient and faster system [66]. It was designed as an adaptive protocol with the ability to adjust its date rate and modulation level according to the channel loading. The idea is to achieve the best quality in low-traffic hours and/or territories and to maximize the channel capacity when the traffic goes up. Unlike POCSAG, the FLEX system incorporates a four-level FSK modulation scheme with a much higher data rate. Consequently, significant energy is created in the vicinity of the DC as shown in Figure 7.1. It is a big challenge to use a direct-conversion architecture for low-cost, low-power and high integration.

Figure 7.2 shows the simulated effect of the DC offset on the BER performance of a 4-FSK receiver [82]. When the offset level is strong enough, the demodulator is eventually out of

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1. An acronym for “FLEXible wide area paging protocol”, also a trademark of Motorola Inc.
2. Post Office Code Standardization Advisory Group
function. The harmonic mixing proposed in the above chapters is a potential solution for self-mixing induced DC offset. After eliminating this dynamic DC offset, baseband DC offset cancellation with very low corner frequency can be incorporated.

The second challenge is how to demodulate the zero-IF 4FSK signal. Demodulation in the direct-conversion POCSAG receiver employs a phase-comparison method which makes a decision by simply observing the phase difference between the quadrature I and Q components of the down-converted signal. Unfortunately, it works only with the binary FSK. A general M-ary FSK demodulator can be constructed by combining the phase-comparator with a zero-
crossing counter [84]. This calculates the number of zero-crossings in a symbol period. Its accuracy can be improved by using a technique (termed zero-crossing interpolation) which generates additional zero-crossings for detection. It has been demonstrated [67] that as more additional zero-crossings are generated the error probability approaches that of the discriminator type demodulator.

7.2 Building Blocks

The direct-conversion receiver block diagram is shown in Figure 7.3. Differential structures are used throughout the design. To minimize the DC offset induced by self-mixing, harmonic mixers [44] were used to replace the conventional ones. The two LO signals driving the mixer pair have a 45° phase difference rather than the quadrature phase used in standard structures. The AGC circuitry adjusts the VGA gain to increase the dynamic range, and the DC offset due to device mismatch is removed at this stage. This is followed by a fifth order gyrator-C low pass filter. Output signals of the filters are processed by the 4-FSK on-chip demodulator.

![Figure 7.3. Direct-conversion 4-FSK receiver block diagram](image-url)
7.2.1 LNA

At the RF frequency range, the non-quasi-static (NQS) phenomenon of the MOS transistor is important. The input impedance of the transistor has a significant, but not-well-modelled, real part, making it difficult to completely perform on-chip matching [86]. In addition, the on-chip inductor consumes a large area and is sensitive to noise coupling. In our design, the matching network is done off-chip with one single inductor and a balun to convert the single-ended signal to differential. The inductive loading of the LNA is realized both off-chip (Q=30) and on-chip (Q=3) so that there is a trade-off between the noise, gain, and linearity of the system. The off-chip version boosts the gain and provides better band pass filtering while the on-chip version provides better linearity performance.

To simplify the design, as shown in Figure 7.4, a common source configuration of LNA was used in our research. The cascaded differential LNA provides more than 20dB gain with the off-chip inductive load. This large gain allows the reduction of the effect of flicker noise in the following stages although it does somewhat degrade the linearity of the receiver. The variable resistor was used to provide the mixers with a proper bias point. In order to minimize off-chip matching inductor value to get higher quality factor, a long channel transistor (256µm/1.2µm) was chosen instead of a short channel device. The optimal bias point was chosen for minimum noise figure according to device characterization results.

7.2.2 Mixer and buffer

The self-mixing induced DC offset is more problematic than the static DC offset caused by device mismatch. It changes with operating conditions and incoming signals. Unlike conventional mixers, the harmonic mixer described above utilizes LO harmonics to mix down the RF signal and is, theoretically, free of self-mixing. Notice that there should be no coupling
between the second harmonic of the LO and the RF input since their relationship is one of current and voltage. It can be seen from Figure 7.5 that the LO stage (m1-m4) acts as a frequency doubler to convert the input differential LO voltage to the current form which contains the even harmonics of LO and controls the transconductance of the RF stage. Any LO leakage to the RF port is mixed to the LO frequency again and is filtered out at a later stage.

Since the switching is done in current domain, the input impedance at the RF port is no longer constant. To connect the mixer to the LNA, a double balanced structure is used to provide a constant impedance to LNA. The other advantage of a double balanced mixer is the elimination of more harmonic components and, consequently, an improvement in the linearity. It is interesting that a 90 degree phase shift LO is used instead of a 180 degree phase shift LO.
An injected current, $I_i$, helps reduce the flicker noise and improves the RF gain without introducing any noise because the transconductances of the RF stage change simultaneously. The noise due to the current source and the LO stage is a common-mode signal seen at the mixer differential output. Figure 7.6 shows this. The measured harmonic mixer is self-mixing free and achieves around a 12 dB gain. To provide enough gain to reduce the noise contribution from the baseband, a buffer with 16.5 dB gain is inserted after the harmonic mixer.

![Figure 7.6](image)

(a) Normal Gilbert-type mixer with current injection (b) Our harmonic mixer.

**Figure 7.6.** The noise advantage of current injection in the harmonic mixer.

### 7.2.3 Ring Oscillator

Unlike conventional mixers, a 45° phase shift is needed for the I/Q channel LOs rather than a 90° phase shift because of harmonic mixing. The RC-CR phase shifters combined with LC tank based VCO may be a possible solution [72]. However, the phase shifter is sensitive to the process variation and the parasitics which introduce severe amplitude and phase imbalance. Therefore, a four-stage differential ring oscillator as shown in Figure 7.7 was implemented by the source coupled logic circuit. One advantage of the harmonic mixer is that it only needs a small LO swing of less than 200mV. This helps minimize substrate coupling. Each output is followed by an amplifier similar to the delay cell circuit in order to isolate the oscillator and
the mixer, and a source follower to give the correct mixer input bias. Eight differential outputs provide the I/Q harmonic mixers with accurate 0°, 45°, 90°, 135° phase shifted LO differential input. The measured phase error is less than 2°.

![Figure 7.7. Differential 4-stage ring oscillator](image)

However, the phase noise of the ring oscillator is the biggest concern. In our research, the main focus was to eliminate the DC offset. Therefore we did not put effort into the phase noise performance. But it is worth mentioning that a lot of effort has been put into improving the ring oscillator phase noise [87]-[89]. The feasibility of a low noise CMOS ring oscillator comparable to the performance of monolithic oscillators has been proven. In addition, another advantage lies in the fact that our ring oscillator operates at the half carrier frequency. It is well known that phase noise performance is inversely proportional to the operating frequency. The lower the frequency, the better the phase noise.

Another alternate solution is to avoid to use this ring oscillator. A 90 degree phase shifter might be put in front between LNA and one of mixers. Therefore, the 45 degree phase shift of the LO is avoided. The ring oscillator might be replaced by high-performance LC oscillator. The drawback is that the attention of the 90 degree phase shifter leads to the degradation of the receiver noise performance.
7.2.4 AGC, LPF, and 4-FSK Demodulator

The AGC circuitry is shown in Figure 7.8. The differential variable MOS resistors were used to construct the variable gain amplifier (VGA) which provides a -14.5dB to 18.6dB gain. The linear resistor R0 was used to improve the linearity. It takes part of the input voltage drop so that the MOS resistors stay in the linear region even at relatively large inputs. The signal level is sensed by a peak detector and is compared with a reference voltage.

Besides self-mixing, the DC offset also emanates from other sources such as device mismatch. In some applications the offset can be removed by means of AC-coupling. Unfortunately, this is not possible for 4-FSK modulation schemes which contain significant DC and low frequency energy. In our research, the peak detector was used to perform DC offset cancellation. As shown in Figure 7.9, the difference between the DC levels of two equal-amplitude sinusoidal signals is equivalent to the difference between their envelopes. The peak detector acts as an offset indicator and the offset is then subtracted from the signal. This approach is very similar to high-pass filtering but it is, intrinsically, a nonlinear process. It is true that the non-linear operation causes a higher harmonic distortion. However, within one symbol period, although the location of zero-crossings of the demodulator are more or less altered, the total

1. Dr. Zhiheng Chen’s work [66].
number does not change. Therefore, the distortion has only a limited impact on the demodulation. The minimum input signal frequency needed by the peak detector to carry out DC offset cancellation is around 200Hz. With 100mV offset at the AGC input, less than 2mV offset at the output is achieved.

![Waveform Diagram](image1)

**Figure 7.9.** Waveforms of the zero-IF 4-FSK signal.

![LC Ladder Diagram](image2)

**Figure 7.10.** The 5th order gyrator-C elliptic low pass filter and its LC ladder prototype.

The channel selection is performed by a fifth order elliptic gyrator-C filter with a bandwidth of 9kHz. The implementation is depicted in Figure 7.10. The gyrator filter simulates an LC ladder using gyrators in place of inductors. LC ladder filters have low sensitivity to parameter variations and have good stability at high orders. These properties are inherited by the gyrator filter.
The demodulator incorporates a modified version of the zero-intermediate frequency zero-crossing demodulator (ZIFZCD) [84] with a clock recovery loop, as shown in Figure 7.3. The ZIFZCD technique, which was originally used for 2-FSK, was modified for the 4-FSK. Unlike that in 2-FSK for which only the sign needs to be known, in the 4-FSK, both the sign and the speed of the signal need to be known. The incoming signals I and Q together with the derived signals I1 and Q1 are converted into the digital domain by four hard-limiters. A series of pulses are then generated on the zero-crossings of the signals. Depending on the phase relationship of the I/Q or I1/Q1 components, the pulses are delivered to either the positive channel or the negative channel and are counted by the two counters PC and NC respectively. The speed decision block compares the outputs of the counters with a fixed threshold in order to determine the frequency offset of the current symbol. The direction decision block, on the other hand, makes a comparison between the two outputs and detects the I/Q phase difference and, thus, the phasor direction. The clock recovery circuit provides clocks for the pulse generator and the decision stage. The 4-FSK demodulation function has been verified experimentally.

7.3 Measurement Results

The measured cascoded device characteristics of LNA are shown in Figure 7.11. The optimal FMIN and optimal associated gain $Ga$ have different bias points. To minimize the noise figure, an optimal noise bias point with a small compromise on the gain was chosen.

Thanks to the contribution of the real part of device input impedance, good input matching is achieved as depicted in Figure 7.12. The reflection coefficient $S_{11}$ is less than -20dB at 930MHz.

Sweeping both the RF input frequency and the LO frequency, it is possible to measure the
LC tank performance at the LNA output. It can be seen from Figure 7.13 that the quality factor of an off-chip bond wire inductor is larger than 30. The result is a large gain and good noise performance of the front-end.

Figure 7.11. Device characteristics of LNA @ 930MHz.

Figure 7.12. Input matching of the front-end

Figure 7.13. Resonant frequency of LC tank
On the other hand, the measured Q of the on-chip inductor shown in Figure 7.14 is only around three at 930MHz. The measured inductance is 6.7nH. It is 0.3nH smaller than the ASITIC [90] designed value. The PADs at the left is an open ground-signal-ground (GSG) pad for deembedding purposes. The lumped model is depicted in Figure 7.15. The comparison between the model and the measurement shows that they agree very well.

Figure 7.14. On-Chip inductor characterization die.

![On-Chip inductor characterization die](image)

Figure 7.15. Lumped model of On-Chip inductor and comparison with measurement.

![Lumped model of On-Chip inductor and comparison with measurement](image)

Figure 7.16 shows the tuning curve of the ring oscillator. The oscillating frequency is proportional to the bias voltage and it operates at the half carrier frequency. Since the control voltage directly controls the bias current of the delay cell, the VCO gain is as large as 1500MHz/V.

AGC gain is measured at different input levels and frequencies. The results are shown in Figure 7.17. A close match between the measurement and the simulation can be observed. The simulated and measured performance of the low pass filter are depicted in Figure 7.18.

A differential 4-FSK signal was generated with the functional generator DS345 and was applied at the AGC input. The demodulated signal was measured at the final demodulator
The output indicates that the 4-FSK demodulator functions correctly.

The noise performance of the chip is shown in Figure 7.20. The front-end with off-chip
inductive loads achieves a 5.8dB noise figure including the balun loss at 100kHz. The high gain of the LNA helps suppress the flicker noise. At higher frequency bands, the flicker noise is smaller and thermal noise dominates. The result indicates that the noise in the mixer is the dominant part of the total noise spectrum. The input-referred noise at the AGC input is around $600nV/\sqrt{\text{Hz}}$.

The LO leakage gain is 54dB less than the RF signal gain. Since the measured isolation between the LO port and the LNA input is larger than 60dB, the front-end is self-mixing free. The receiver achieves a 14.5dB noise figure at 10kHz and the maximum gain is about 62dB.
The overall DC offset is less than 1mV. The receiver consumes 58mW power. The die photo of the receiver is presented in Figure 7.21. The characteristics of CMOS direct conversion 4-FSK pager receiver are summarized in Table 7.1.
### 7.4 Discussion

Since the front-end is for direct conversion receivers, flicker noise reduction is our biggest concern. Both LNA and the mixers were optimized for noise improvement while the linearity

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**Table 7.1** Receiver performance summary
was degraded due to large LNA gain and poor mixer linearity performance. Therefore it restricts this front-end on those applications in which the linearity requirement of the receiver is very relaxed.

In addition, the input-referred IP2 performance is not good enough for direct-conversion applications since there is no tuning for device mismatch at the mixer stage. It could be further improved by either using some kind of IM2 compensation circuitry as did in [72] or using the bias approach as suggested in the previous chapter.

7.5 Conclusion

The conventional self-mixing problem encountered in direct-conversion receivers was solved successfully. A CMOS self-mixing-free direct-conversion RF front-end was demonstrated.
CHAPTER 8

Future Work and Conclusion

8.1 Future Work

Design issues in direct conversion receivers were studied in detail and a direct conversion pager receiver was demonstrated. However, there is still a lot of research work to do in the future.

1. Crosstalk and substrate noise. Various shielding methods were proposed but all shielding layers were assumed to be solid grounds for the convenience of the simulations. This is not true in a real implementation. Firstly, a mesh ground should be used for the interconnections. The impedance of the transmission line will most likely become large due to reduced capacitance and increased inductance, and the loss will increase also. The crosstalk suppression performance of the shielding will be degraded. Secondly, the shielding ground is assumed to connect to the ideal ground directly, while bond wires are needed for the connection in a real case. The effect of ground bond wires was not discussed. In addition, the effect of shielding on an active device needs more deep study. This would be a good experiment if a whole receiver was implemented with our shielding method and compared to the case in which there is no shielding.
2. Flicker noise under switching conditions. The flicker noise model was proposed, and was used to optimize the mixer noise performance. It will be a good idea to use this model to analyze the flicker noise effect on the phase noise performance of the voltage-controlled-oscillators.

3. Harmonic mixer. Self-mixing induced DC offset and the LO leakage problem were solved successfully. However, the linearity performance needs to be improved if the mixer is to be used in some other systems where the linearity requirement are more stringent.

4. Lateral bipolar device and LBJT harmonic mixer. It is expected that the device performance such as $f_t$, current leakage can be improved with a more advanced process which has a shorter gate length. A shorter gate length would mean a narrower base width. The current gain and current efficiency could be improved further. The mixer constructed using this device would perform at higher frequencies and the performance would be much better.

5. The pager receiver. DC offset problem was solved successfully. To translate the results of this research into a product, more work regarding phase noise improvement of ring oscillator, noise, and IIP2 improvement needs to be done. One way to avoid using a ring oscillator is to have a 90 degree phase shifter before the amplified signals going to the I/Q harmonic mixers. The phase shifter could be realized using a two-stage poly-phase filter. The drawback is that the filter has a loss which may degrade the noise performance a little bit. In our pager receiver, the IIP2 improvement approach proposed in Chapter 6 was not implemented. If this was added, a good IIP2 performance is expected. In addition, using a good process such as TSMC0.25µm, an LBJT harmonic mixer could be
used instead of a CMOS one. Therefore, the noise performance could be improved further, especially the flicker noise suppression.

8.2 Conclusion

In conclusion, on-chip crosstalk and substrate noise were first studied through simulations. It is shown that physical separation is pointless if no shielding schemes are adopted. Some effective shielding methods to reduce the crosstalk were proposed. Shielding achieved a 20–40dB improvement on crosstalk. The flicker noise under switching conditions was studied experimentally for the first time. Methods to reduce flicker noise were discussed. The proposed simple noise model makes it possible to predict and optimize the circuit flicker noise performance. An RF application on mixer was demonstrated. The severe self-mixing induced DC offset problem was circumvented completely using the proposed CMOS harmonic mixing technique. Further, the use of this technique means that LO leakage is no longer a problem for direct conversion receivers. Two kinds of harmonic mixers in a CMOS process were designed and fabricated. The CMOS harmonic mixer achieved 44dB DC-offset lower than conventional mixer. Based on a harmonic mixing technique, the lateral bipolar mixer suppressed the flicker noise successfully and achieved less than 18dB noise figure at 10kHz frequency. The mixers are totally self-mixing free and are suitable for direct-conversion receivers. Finally, a fully-integrated CMOS direct conversion pager receiver was demonstrated for the first time. The total DC offset at the receiver output is less than 1mV while the signal level is as large as 400mV.
Harmonic Mixer Analysis

Square-law current equation is assumed as following.

\[ I = \frac{\mu C_{ox} W}{2L}(V_{gs} - V_{th})^2 = k\Delta V^2 \]  \hspace{1cm} (I.1)

At LO stage, we have:

\[ I_{lo}^- = k_{lo}(\Delta V_{lo} + v_{lo}^+)^2 \]  \hspace{1cm} (I.2)

\[ I_{lo}^+ = k_{lo}(\Delta V_{lo} + v_{lo}^-)^2 \]  \hspace{1cm} (I.3)

where

\[ k_{lo} = \frac{\mu C_{ox} W}{2L} \left( \frac{W}{L} \right) \]  \hspace{1cm} (I.4)

\[ \Delta V_{lo} = (VLO - V_{thlo}) \]  \hspace{1cm} (I.5)

\[ v_{lo}^+ = -v_{lo}^- = \frac{v_{lo}}{2} = \frac{a_{lo}}{2} \cos(\omega_{lo}t) \]  \hspace{1cm} (I.6)

where \( VLO \) is the DC bias voltage at the LO port and \( a_{lo} \) is the amplitude of LO signal.

At RF stage, we have:

\[ I_{rf}^+ = k_{rf}(\Delta V_{rf} + v_{rf}^+)^2 \]  \hspace{1cm} (I.7)
where

\[
\Delta V_{rf} = (VRF - VCOM - V_{thrf})
\]  
(I.10)

\[
v^+_{rf} = -v^-_{rf} = \frac{v_{rf}}{2}
\]  
(I.11)

where \(VRF\) is the DC bias voltage at the RF port and \(VCOM\) is the voltage at the common drains of the LO stage. Notice that \(\Delta V_{rf}\) is not a constant while \(\Delta V_{lo}\) is.

The total current in the mixer equals:

\[
I = I^+_{rf} + I^-_{rf} + I_0 = I^+_{lo} + I^-_{lo} = 2k_{lo}\Delta V_{lo}^2 + \frac{k_{lo}}{2}v_{lo}^2
\]  
(I.12)

The total output voltage is:

\[
v_{out} = (I^+_{rf} - I^-_{rf})R_L = 2k_{rf}\Delta V_{rf}R_Lv_{rf}
\]  
(I.13)

It can be derived that:

\[
\Delta V_{rf} = \sqrt{\frac{2k_{lo}\Delta V_{lo}^2 + \frac{k_{lo}}{2}v_{lo}^2 - I_0 - \frac{k_{rf}}{2}v_{rf}^2}{2k_{rf}}}
\]  
(I.14)

Then

\[
v_{out} = \sqrt{4k_{lo}k_{rf}\Delta V_{lo}^2 + k_{lo}k_{rf}v_{lo}^2 - 2k_{lo}I_0} - \frac{k_{rf}}{2}v_{rf}^2R_Lv_{rf}
\]  
(I.15)

It is a good assumption that \(k_{rf}v_{rf}^2 \ll (4k_{lo}k_{rf}\Delta V_{lo}^2 - 2k_{lo}I_0)\) since \(v_{rf} \ll v_{lo}\). So the time-varying transconductance equals:
\[ G_m(t) = \frac{V_{out}}{V_{rf}R_L} = \sqrt{4k_{lo}k_{rf}\Delta V_{lo}^2 + k_{lo}k_{rf}V_{lo}^2 - 2k_{rf}I_0 - k_{rf}^2V_{rf}^2} \] (I.16)

Substituting (I.6) to (I.16), we derive that:

\[ G_m(t) \approx \sqrt{4k_{lo}k_{rf}\Delta V_{lo}^2 + k_{lo}k_{rf}V_{lo}^2 - 2k_{rf}I_0} \] (I.17)

Set

\[ x_0 = 1 + \frac{8k_{lo}\Delta V_{lo}^2 - 4I_0}{k_{lo}a_{lo}^2} \] (I.18)

and

\[ x = \cos 2\omega_{lo}t \] (I.19)

Note that \( x_0 \) is larger than 1 in the normal operation to ensure there are currents flowing at the RF stage.

Using Taylor’s expansion:

\[ \sqrt{x + x_0} = x_0 + \frac{1}{2}x_0^{-\frac{1}{2}} + \left( -\frac{1}{4}\right)x_0^{-\frac{3}{2}} + \left( -\frac{3}{8}\right)x_0^{-\frac{5}{2}} + \left( -\frac{15}{16}\right)x_0^{-\frac{7}{2}} + \ldots \] (I.20)

\[ \approx \left( 1 - \frac{1}{16}x_0^{-\frac{1}{2}} - \frac{15}{1024}x_0^{-\frac{3}{2}} \right) \cos 2\omega_{lo}t + \left( -\frac{1}{16}x_0^{-\frac{3}{2}} - \frac{15}{768}x_0^{-\frac{5}{2}} \right) \cos 4\omega_{lo}t + \ldots \]

The equation indicates that there will be \( f_r \pm 2nf_{lo} \) (\( n=0, 1, 2, 3, \ldots \)) components at the output spectrum.

When \( n=0 \), there will be RF signal feed through at the output. The gain is:
When \( n = 1 \), the signal gain can be derived as:

\[
G_{frf} = a_{lo} \frac{k_{rf}k_{lo}}{2} R_L \left( \frac{1}{16} x_0^2 - \frac{15}{1024} x_0^2 \right) = a_{lo} \frac{k_{rf}k_{lo}}{2} R_L x_0^{\frac{7}{2}} \tag{I.21}
\]

The ratio of signal feedthrough gain to the signal gain is approximately proportional to \( x_0 \).

\[
\frac{G_{frf}}{G_{frf-2f_{lo}}} \approx 4 x_0 \tag{I.23}
\]

The smaller \( x_0 \), the larger the signal gain, and the smaller the signal feedthrough at the output.

To derive linearity equation, we cannot assume \( v_{rf} \) is small any longer. Then, the new \( x_0 \) is:

\[
x_0 = 1 + 8k_{lo} \frac{\Delta V_{lo}^2}{2} - 4I_0 \frac{v_{rf}^2}{k_{lo}a_{lo}^2} = 2k_{rf} \frac{\Delta V_{lo}^2}{k_{lo}a_{lo}^2 + k_{lo}a_{lo}^2 - 4I_0} - y^2 = c(y_0 - y) \tag{I.24}
\]

where

\[
c = \frac{2k_{rf}}{k_{lo}a_{lo}^2}, \ y_0 = \frac{8k_{lo} \Delta V_{lo}^2 + k_{lo}a_{lo}^2 - 4I_0}{2k_{rf}}, \ y = v_{rf}^2 \tag{I.25}
\]

Using Taylor’s expansion again, the coefficient of the second term in ((I.20)) becomes:
The first term is related to the first harmonic and the second term is related to the third harmonic. According to the formula by Razavi [59], we get:

\[
\frac{1}{2}x_0^\frac{1}{2} + \frac{3}{64}x_0^\frac{5}{2} = \frac{c_1}{2}(y_0 - y)^\frac{1}{2} + \frac{3}{64}c_2(y_0 - y)^\frac{5}{2}
\]

\[
\approx \left(\frac{1}{2}c_1y_0^\frac{1}{2} + \frac{3}{64}c_2y_0^\frac{5}{2} + \ldots\right) + \left(\frac{1}{4}c_1y_0^\frac{3}{2} + \frac{15}{128}c_2y_0^\frac{7}{2} + \ldots\right)y + \ldots
\]

\[
= c_1 + c_2y_{rf}^2 + \ldots
\]

The first term is related to the first harmonic and the second term is related to the third harmonic. According to the formula by Razavi [59], we get:

\[
A_{IIP3} = \frac{4c_1}{3c_2} \approx \sqrt{\frac{256c_2y_0^2 + 6y_0}{96c_2y_0^2 + 15}}
\]

\[
= a_{lo} \frac{x_0}{3} \frac{k_{lo}}{k_{rfN}} \left[4 - \frac{17}{32x_0^2 + 5}\right]
\]

\[
IIP3 = 10 + 20\log(A_{IIP3}) \text{ dBm}
\]
\[
NF = 10 \log \left( 1 + \frac{\Delta f}{4kT R_s} \right) 
\approx 10 \log \left( 1 + \frac{2R_L(\gamma G_{ff} + 1) + \frac{G_{ff}^2 K_f}{(WL)_{rf} C_{ox} 2kTf}}{G_{ff-2\beta a} R_S} \right)
\]

\approx 10 \log \left( \frac{8x_0^2 K_f}{(WL)_{rf} C_{ox} R_s kTf} \right)
\]
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Publication List


