Overview

- Reading
  B. Razavi Chapter 4.

- Introduction

  Offering many useful properties, differential operation has become the dominant choice in today's high-performance analog and mixed-signal circuits. This lecture deals with the analysis and design of CMOS differential amplifiers. It contains:

  - Review of single-ended and differential operation.
  - Analysis of the large-signal and small-signal behavior.
  - The common-mode rejection.
  - Differential pair with diode-connected and current-source loads as well as differential cascode stages.
Single-ended and differential operation

- Single-ended and differential signals

![Diagram of single-ended and differential signals](image)

- What are “common-mode” (CM) and “differential mode” (DM)?

Advantages of differential operation

- Reduction of coupling

![Diagram of reduction of coupling](image)

- Common-mode rejection occurs with noisy supply voltages

![Diagram of common-mode rejection](image)
Advantages of differential operation (cont’d)

- Reduction of coupled noise by differential operation
- Increase in maximum achievable voltage swing
- Simpler biasing
- Higher linearity

Simple differential circuit

(a) [Diagram]

(b) [Diagram]
Basic differential pair

- Schematic — source-coupled pair

The differential pair employs a current source $I_{SS}$ to make $I_{D1} + I_{D2}$ independent of $V_{in,CM}$. Thus, if $V_{in1} = V_{in2}$, the bias current of each transistor equals $I_{SS}/2$ and the output common-mode level is $V_{DD} - R_D I_{SS}/2$.

Basic differential pair (cont’d)

- Qualitative analysis

Input/output characteristics
Common-mode characteristics

- Common-mode schematic

- Common-mode input/output characteristics

Common-mode characteristics

- Input common-mode range – $M_1, M_2$ in saturation

$$V_{GS1} + (V_{GS3} - V_{TH3}) \leq V_{in,CM} \leq \min \left[ V_{DD} - R_D \frac{I_{DS}}{2} + V_{TH}, \quad V_{DD} \right]$$

- The small-signal differential gain of a differential pair vs. the input CM level
Output swing of a differential pair

- For $M_1$ and $M_2$ to be saturated, each output can go as high as $V_{DD}$ but as low as approximately $V_{in,CM} - V_{TH}$. In other words, the higher the input CM level, the smaller the allowable output swings. For this reason, it is desirable to choose a relatively low $V_{in,CM}$.

- An trade-off exists between the maximum value of $V_{in,CM}$ and differential gain. Similar to a simple CS stage, the gain of a differential pair is a function is a function of the dc drop across the load resistors. Thus, if $R_D IS / 2$ is large, $V_{in,CM}$ must remain close to ground potential.

Quantitative analysis

- Differential pair

\[
V_{out1} = V_{DD} - R_D I_{D1}, \quad V_{out2} = V_{DD} - R_D I_{D2}
\]

\[
[R_{D1} = R_{D2} = R_D]
\]

\[
V_{out1} - V_{out2} = R_D (I_{D2} - I_{D1})
\]

Assuming the circuit is symmetric, $M_1$ and $M_2$ are saturated, and $\lambda = 0$, $V_{in1} - V_{in2} = V_{GS1} - V_{GS2}$

For a square-law device, we have:

Therefore,

\[
V_{in1} - V_{in2} = \frac{2I_{D1}}{\mu C_{ox} W L} - \frac{2I_{D2}}{\mu C_{ox} W L}
\]

Recognizing that $I_{D2} + I_{D1} = I_{SS}$, we obtain
Quantitative analysis (cont’d)

\[ (V_{m1} - V_{m2})^2 = \frac{2}{\mu_c C_{ox}} \left( \frac{W}{L} \right) (I_{SS} - 2I_D) \]

\[ \frac{1}{2} \mu_c C_{ox} \left( \frac{W}{L} \right) (V_{m1} - V_{m2})^2 - I_{SS}^2 = -2I_D \frac{I_{D2}}{I_D} \]

Squaring the two sides again and

\[ 4I_D I_{D2} = (I_{D1} + I_{D2})^2 - (I_{D1} - I_{D2})^2 = I_{SS}^2 - (I_{D1} - I_{D2})^2 , \]

we arrive at

\[ I_{D1} - I_{D2} = \frac{1}{2} \mu_c C_{ox} \left( \frac{W}{L} \right) (V_{m1} - V_{m2}) \]  
\[ \sqrt{\mu_c C_{ox} \left( \frac{W}{L} \right) } - (V_{m1} - V_{m2}) \]

Denoting \( \Delta I_D = I_{D1} - I_{D2} \) and \( \Delta V_m = V_{m1} - V_{m2} \), we can show that

\[ \frac{\partial \Delta I_D}{\partial \Delta V_m} = \frac{1}{2} \mu_c C_{ox} \left( \frac{W}{L} \right) \frac{4I_{SS}}{\sqrt{\mu_c C_{ox} \left( \frac{W}{L} \right) } - 2\Delta V_m^2} \]

\[ - \frac{4I_{SS}}{\sqrt{\mu_c C_{ox} \left( \frac{W}{L} \right) } - \Delta V_m^2} \]

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Quantitative analysis (cont’d)

- For \( \Delta V_m = 0 \), \( G_m = \frac{\partial \Delta I_D}{\partial \Delta V_m} \bigg|_{\Delta V_m=0} = \sqrt{\mu_c C_{ox} \left( \frac{W}{L} \right) I_{SS}} \)

- Since \( \Delta V_{out} = V_{out1} - V_{out2} = R_D \Delta I_D = R_D G_m \Delta V_m \)

the small-signal differential gain is given as

\[ |A_m| = G_m R_D = \sqrt{\mu_c C_{ox} \left( \frac{W}{L} \right) I_{SS} \cdot R_D} \]

- \( G_m = 0 \) for \( \Delta V_m = \frac{2I_{SS}}{\sqrt{\mu_c C_{ox} \left( \frac{W}{L} \right) } \cdot \Delta V_m} \)

- Variation of \( I_D \) and \( G_m \) vs. \( \Delta V_m \)

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Analog-Circuit Design 4-13 Ching-Yuan Yang / EE, NCHU
Quantitative analysis (cont'd)

For a zero differential input, \( I_{D1} = I_{D2} = I_{DS} / 2 \), and hence

\[ (V_{GS} - V_{TH})_{1,2} = \frac{I_{DS}}{\mu C_{ox}} \frac{W}{L} = \frac{\Delta V_{in}}{\sqrt{2}} \]

Increasing \( \Delta V_{in} \) to make the circuit more linear inevitably increases the overdrive voltage of \( M_1 \) and \( M_2 \). For a given \( I_{DS} \), this is only by reducing \( W/L \) and hence the \( g_m \) of the transistors.

Quantitative analysis (cont'd)

- Input/output characteristic

- As \( W/L \) increases, \( \Delta V_{in} \) decreases, narrowing the input range across which both devices are on.

- As \( I_{DS} \) increases, both the input range and the output current swing increase.
Differential pair with small-signal inputs

- Scheme – $M_1$ and $M_2$ sat., small signals $V_{in1}$ and $V_{in2}$.

- Analysis

Differential pair sensing one input signal. Circuit viewed as a CS stage degenerated by $M_2$. Equivalent circuit.

Differential pair with small-signal inputs (cont’d)

- Replacing $M_1$ by a Thevenin equivalent

$M_2$ operates as a CG stage, exhibiting a gain equal to

$$\frac{V_x}{V_{in2}} = \frac{R_0}{g_m + \frac{1}{g_m}}$$

The overall voltage for $V_{in1}$ is $(V_X - V_Y)_{Due to V_{in1}} = -\frac{2R_0}{g_m + \frac{1}{g_m}}V_{in1}$

which, for $g_{m1} = g_{m2} = g_m$ reduces to is $(V_X - V_Y)_{Due to V_{in1}} = -g_mR_0V_{in1}$.

Similarly, $(V_X - V_Y)_{Due to V_{in2}} = -g_mR_0V_{in2}$. Thus, we have

$$\frac{(V_X - V_Y)_{Due to V_{in1}}}{(V_X - V_Y)_{Due to V_{in2}}} = \frac{V_{in1}}{V_{in2}} = -g_mR_0$$
Differential and common-mode components

\[ V_{in1} = \frac{V_{in1} - V_{in2}}{2} + \frac{V_{in1} + V_{in2}}{2} \] (a)

\[ V_{in2} = \frac{V_{in2} - V_{in1}}{2} + \frac{V_{in1} + V_{in2}}{2} \] (b)

Superposition for differential and common-mode signals

\[ V_{in1} = \frac{V_{in1} - V_{in2}}{2} + \frac{V_{in1} + V_{in2}}{2} \] (a)

\[ V_{in2} = \frac{V_{in2} - V_{in1}}{2} + \frac{V_{in1} + V_{in2}}{2} \] (b)
Differential and common-mode components (cont’d)

- $\lambda \neq 0$
  - Differential-mode operation
  - Common-mode operation

\[
V_x = -g_m(R_D)_{\lambda}(V_{m1} - V_{m2})/2 \\
V_y = -g_m(R_D)_{\lambda}(V_{m2} - V_{m1})/2 \\
V_x - V_y = -g_m(R_D)_{\lambda}
\]

If the circuit is fully symmetric and $I_{SS}$ an ideal current source, the current drawn by $M_1$ and $M_2$ from $R_{D1}$ and $R_{D2}$ is exactly equal to $I_{SS}/2$ and independent of $V_{in,CM}$. Thus, $V_x$ and $V_y$ experience no change as $V_{in,CM}$ varies.

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Common-mode response

- Differential pair sensing CM input

\[
R_{SS} : \text{the output impedance of current source.}
\]

\[
A_{v,CM} = \frac{V_{out}}{V_{in,CM}} = -\frac{R_D/2}{1 + R_{SS}} \quad (\lambda = \gamma = 0)
\]
Common-mode response with mismatch

- Resistor mismatch

\[ \Delta V_X = - \Delta V_{in,CM} \frac{g_m}{1 + 2g_m R_{SS}} R_D \]
\[ \Delta V_Y = - \Delta V_{in,CM} \frac{g_m}{1 + 2g_m R_{SS}} (R_D + \Delta R_D) \]

A CM change at the input introduces a differential component at the output.

- Effect of CM noise

Common-mode response with finite tail cap.

\[ \Delta + = \Delta - = \Delta \]

Thus, the circuit converts input CM variations to a differential error by a factor equal to

\[ A_{CM-DM} = - \frac{\Delta g_m R_D}{(g_{m1} + g_{m2}) R_{SS} + 1} \]

\[ A_{CM-DM} \]: CM to DM conversion

\[ \Delta g_m = g_{m1} - g_{m2} \]
Common-mode rejection ratio (CMRR)

- **Definition** \( \text{CMRR} = \frac{A_{CM}}{A_{CM-DIFF}} \)
- If only \( g_m \) mismatch is considered
  
  - Differential mode (assume \( V_{in1} = -V_{in2} \))
    \[
    |A_{CM}| = \frac{R_D}{2} \frac{g_{m1} + g_{m2} + 4g_m R_{os}}{1 + (g_{m1} + g_{m2}) R_{os}}
    \]
  
  - Common-mode to differential-mode conversion
    \[
    A_{CM-DIFF} = -\frac{\Delta g_m R_D}{(g_{m1} + g_{m2}) R_{os} + 1}
    \]
  
  - **CMRR**
    \[
    \text{CMRR} = \frac{g_{m1} + g_{m2} + 4g_m R_{os}}{2\Delta g_m}
    = \frac{g_m}{\Delta g_m} \left[ 1 + 2g_m R_{os} \right]
    \]

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Differential pair with MOS loads

- **Diode-connected load**
  \[
  A_v = -g_{mN} \left( g_{mP} \left[ V_{dd} \right] \right)
  \approx \frac{g_{mN}}{g_{mP}}
  = \left[ \frac{\mu_p (W/L)_N}{\mu_p (W/L)_P} \right]
  \]

- **Current-source load**
  \[
  A_v = -g_{mN} \left( r_{on} \left[ V_{dd} \right] \right)
  \]
Differential pair with MOS loads (cont’d)

- Diode-connected + current source loads

- Cascode differential pair

\[
|A_v| \approx g_{m1}(g_{m3}r_{o3}r_{o7})(g_{m5}r_{o5}r_{o7})
\]

Half circuit

Variable-gain amplifier (VGA)

- Simple VGA

  \[ A_v = \frac{V_{out}}{V_{in}} \text{ varies from zero (if } I_{D3} = 0 \text{) to a maximum value given by voltage headroom limitations and device dimensions.} \]

  \[ \text{VGAs find application in systems where the signal amplitude may experience large variations and hence requires inverse change in the gain.} \]

- Two stages providing variable gain

Consider two differential pairs that amplify the input by opposite gain. We now have \( V_{out1}/V_{in} = -g_{m}R_{D1} \) and \( V_{out2}/V_{in} = g_{m}R_{D2} \), where \( g_{m} \) denotes the transconductance of each transistor in equilibrium. If \( I_1 \) and \( I_2 \) vary in opposite directions, so do \( |V_{out1}/V_{in}| \) and \( |V_{out2}/V_{in}| \).
Gilbert cell

- $V_{out} = V_{out1} + V_{out2} = A_1V_{in} + A_2V_{in}$

- If $I_1 = 0$, then $V_{out} = +g_mR_DV_{in}$
  - If $I_2 = 0$, then $V_{out} = -g_mR_DV_{in}$
  - For $I_1 = I_2$, the gain drops to zero.

- $V_{cont1}$ and $V_{cont2}$ vary $I_1$ and $I_2$ in opposite directions such that the gain of the amplifier changes monotonically. For $V_{cont1} = V_{cont2}$, the gain is zero.

- For $M_{5,6}$ to operate in saturation, the CM level of $V_{cont}$ must be such that $V_{CM,cont} ≤ V_{CM,in} - V_{GS1} + V_{TH5,6}$.

Gilbert cell (cont’d)

- Gilbert cell sensing the input voltage by the bottom differential pair

- For very positive $V_{cont}$, $V_{out} = g_{m5,6}R_DV_{in}$.
  - For very negative $V_{cont}$, $V_{out} = -g_{m5,6}R_DV_{in}$.