Phase-Locked Loops

Fundamentals of PLLs (II)

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Block diagram of PLL

- **Open-loop transfer function**
  \[ G(s) = \frac{\theta_o(s)}{\theta_e(s)} = \frac{K_d K_o F(s)}{s} = \frac{KF(s)}{s} \]  
  (loop gain)

- **System transfer function**
  \[ H(s) = \frac{\theta_o(s)}{\theta_i(s)} = \frac{G(s)}{1 + G(s)} \]

- **Error transfer function**
  \[ E(s) = \frac{\theta_e(s)}{\theta_i(s)} = 1 - H(s) \]
Second-order PLL with a simple RC filter

\[ R \quad C \]

\[ \tau_1 = RC \]

\[ F(s) = \frac{1}{1 + sRC} = \frac{1}{1 + s\tau_1} \]

- Open-loop transfer function
  \[ G(s) = \frac{K}{s(1 + s\tau_1)} \] (loop gain)
  \[ G(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_ns + \omega_n^2} \]

- System transfer function
  \[ H(s) = \frac{K / \tau_1}{s^2 + s/\tau_1 + K / \tau_1} \] \[\Rightarrow H(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_ns + \omega_n^2} \]

- Error transfer function
  \[ E(s) = \frac{s(s\tau_1 + 1)}{s^2 + s/\tau_1 + K / \tau_1} \] \[ E(s) = \frac{s^2 + 2\zeta\omega_ns}{s^2 + 2\zeta\omega_ns + \omega_n^2} \]

- Theory of servomechanism (dynamic motion equation)
  - natural frequency \( \omega_n = \sqrt\frac{K}{\tau_1} \)
  - damping factor \( \zeta = \frac{\omega_n}{2K} = \frac{1}{2\sqrt{K\tau_1}} = \frac{1}{2\omega_n\tau_1} \)
• Plots of 2\textsuperscript{nd}-order PLL ($\zeta = 0.7$)

\begin{align*}
20\log |H(jx)| & \quad \text{Phase of } G(jx) \\
20\log |E(jx)| &
\end{align*}

PLL ICs

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• Transfer functions for different damping factors $\zeta$
2nd-order PLL with a phase lag-lead RRC or RCC filter

- Open-loop gain
  \[ G(s) = \frac{K(1 + s\tau_2)}{s(1 + s\tau_1)} \]

- Transfer function
  \[ H(s) = \frac{(K / \tau_1)(1 + s\tau_2)}{s^2 + s(1 + K\tau_2) / \tau_1 + K / \tau_1} \]

- Natural frequency & damping factor
  \[ \omega_n = \sqrt{\frac{K}{\tau_1}} \quad \zeta = \frac{\omega_n}{2}\left(\frac{\tau_2 + 1}{K}\right) \]

\[ G(s) = \frac{s(2\zeta\omega_n - \omega_n^2 / K) + \omega_n^2}{s(s + \omega_n^2 / K)} \]
\[ H(s) = \frac{s(2\zeta\omega_n - \omega_n^2 / K) + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \]
\[ E(s) = \frac{s^2 + s\omega_n^2 / K}{s^2 + 2\zeta\omega_n s + \omega_n^2} \]
Type-2 2\textsuperscript{nd}-order PLL with voltage output PD

\[ F(s) = -\frac{1 + s\tau_2}{s\tau_1 + 1/A} \approx -\frac{1 + s\tau_2}{s\tau_1} \quad (A \gg 1) \]

where
\[ \tau_1 = \left( R_1 + \frac{R_1 + R_2}{A} \right) C \approx R_1C \quad \tau_2 = R_2C \]

- Loop gain \( K = K_dK_AK_o \), DC gain \( K_{DC} = K_dK_AK_oF(0) = K_dK_AK_oA \)
- Open-loop gain
\[ G(s) = \frac{K(1 + s\tau_2)}{s[s\tau_1 + 1/A]} \approx \frac{K(1 + s\tau_2)}{s^2\tau_1} \]
- Transfer function
\[ H(s) = \frac{K(s\tau_2 + 1)}{s^2\tau_1 + s(K\tau_2 + 1/A) + K} \]
a zero located at \( s = -\frac{1}{\tau_2} \)
- Natural frequency & damping factor
\[ \omega_n = \sqrt{\frac{K}{\tau_1}} \quad \zeta = \omega_n \frac{\tau_2}{2} \]
\[ \Rightarrow G(s) = 2\zeta\omega_n s + \omega_n^2 \quad H(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad E(s) = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \]
Loop filter for a 2\textsuperscript{nd}-order type-2 PLL

1. Single-path circuit with Opamp

\[
F(s) = -\frac{1 + s\tau_2}{s\tau_1 + 1/A} \approx -\frac{1 + s\tau_2}{s\tau_1} = -\left(\frac{\tau_2}{\tau_1} + \frac{1}{s\tau_1}\right) \quad (A \gg 1)
\]

where \(\tau_1 = \left(R_1 + \frac{R_1 + R_2}{A}\right)C \approx R_1C\) \(\tau_2 = R_2C\)

2. Two-path proportional-plus-integral configuration

\[
F(s) = K_1 + \frac{K_2}{s} \quad \text{where} \quad K_1 = \frac{\tau_2}{\tau_1}, \quad K_2 = \frac{1}{\tau_1}
\]

- Note that these example are not low-pass filters. A better name might have been loop controller. The main purpose is to establish dynamics of the feedback loop and to deliver a suitable signal to the VCO. Any filtering of unwanted signals is a secondary task.
Plots of type-2 2\textsuperscript{nd}-order PLL with voltage output PD

20\log|H(jx)| \quad \text{Phae of } G(jx) \quad 20\log|E(jx)|

- Normalized forms:
  \[ G(\sigma) = \frac{1+2\sigma \zeta}{\sigma^2} \quad \text{or} \quad G(jx) = \frac{1+2j\zeta x}{-x^2} \]
  \[ H(jx) = \frac{1+2j\zeta x}{-x^2 + 2j\zeta x + 1} \quad E(jx) = \frac{-x^2}{-x^2 + 2j\zeta x + 1} \]
Plots of type-2 2\textsuperscript{nd}-order PLL for different damping factor $\zeta$
Type-2 2\textsuperscript{nd}-order PLL with current output PD

2\textsuperscript{nd}-order PLL with a passive integrating RC filter

\[ i_d = \frac{I_p \phi_e}{2\pi} = K_{di} \phi_e \]

where \( K_{di} = \frac{I_p}{2\pi} \)

\[ V_c(s) = I_d(s)Z(s) \]

\[ Z(s) = \frac{1 + sRC}{sC} = \frac{1 + s\tau_2}{sC} \]

where \( \tau_2 = RC \)

- Open-loop gain \( G(s) = K_{di} K_o \frac{1 + s\tau_2}{s^2C} \)

- Natural frequency & damping factor \( \omega_n = \sqrt{\frac{K_{di} K_o}{C_1}} \)
\( \zeta = \omega_n \frac{\tau_2}{2} \)

- Transfer function

\[ G(s) = \frac{2 \zeta \omega_n s + \omega_n^2}{s^2} \]
\[ H(s) = \frac{2 \zeta \omega_n s + \omega_n^2}{s^2 + 2 \zeta \omega_n s + \omega_n^2} \]
\[ E(s) = \frac{s^2}{s^2 + 2 \zeta \omega_n s + \omega_n^2} \]
Characteristics of 2\textsuperscript{nd}-order type-2 PLL

- **Transfer function**

  \[ H(s) = \frac{K_d K_o (s \tau_2 + 1) / \tau_1}{s^2 + sK_d K_o \tau_2 / \tau_1 + K_d K_o / \tau_1} = \frac{K_d K_o (K_1 s + K_2)}{s^2 + sK_d K_o K_1 + K_d K_o K_2} = \frac{2\zeta \omega_n s + \omega_n^2}{s^2 + 2\zeta \omega_n s + \omega_n^2} \]

- The denominator polynomial (characteristic polynomial) is of second degree. ⇒ *second order.*

- A zero is located at \( s = -1/\tau_2 = -K_2/K_1 \). It is essential for loop stability.

- Type 2 ⇒ refer to two integrators within the loop.
  (one in the filter and the other in the VCO)

- **Natural frequency & damping**

  \[
  \omega_n = \sqrt{\frac{K_d K_o}{\tau_1}} = \sqrt{K_d K_o K_2} \\
  \zeta = \frac{\tau_2}{2} \sqrt{\frac{K_d K_o}{\tau_1}} = \frac{\tau_2 \omega_n}{2} = \frac{K_1}{2} \sqrt{\frac{K_d K_o}{K_2}}
  \]
Loop parameters of 2\textsuperscript{nd}-order type-2 PLL

System transfer function

\[ H(s) = \frac{2\zeta \omega_n s + \omega_n^2}{s^2 + 2\zeta \omega_n s + \omega_n^2} \]

- \( \zeta < 1 \): the poles are a complex-conjugate pair
  Geometry of the complex pole:
  (illustrating \( \omega_n \) and \( \zeta \))

- \( \zeta = 1 \): the poles are real and coincident
- \( \zeta > 1 \): the geometric mean of the pole locations is equal to \( \omega_n \), and
  \[
  \frac{\omega_{p1}}{\omega_{p2}} = 2\zeta^2 + 2\zeta \sqrt{\zeta^2 - 1} - 1
  \]

- Values of \( \zeta \) typically lie between 0.5 and 2, with 0.707 often a preferred value.
- \( \zeta < 0.5 \), loops have excessive overshoot in transient responses and so are dynamically unsatisfactory.
• Loop gain:  
\[ K_T = K_d K_o K_1 = \frac{K_d K_0 \tau_2}{\tau_1} \text{ [rad/sec]} \]

\[ K_T = 2\zeta \omega_n \quad \omega_n = \sqrt{\frac{K_T}{\tau_2}} \]

\[ K_T \tau_2 = 4\zeta^2 \quad \zeta = \frac{1}{2} \sqrt{K_T \tau_2} \]

\[ H(s) = \frac{K_T (s + K_T / 4\zeta^2)}{s^2 + sK_T + K_T^2 / 4\zeta^2} = \frac{K_T (s + 1/ \tau_2)}{s^2 + K_T s + K_T / \tau_2} \]

\[ E(s) = \frac{s^2}{s^2 + sK_T + K_T^2 / 4\zeta^2} = \frac{s^2}{s^2 + K_T s + K_T / \tau_2} \]

• DC gain:  
\[ K_{DC} = \left| \lim_{s \to 0} sG(s) \right| = K_d K_0 |F(0)| \text{ [rad/sec]} \]

For a type 1 loop, $F(0)$ is finite, whereas integrators in $F(s)$ make it infinite for loops of type 2 or higher.
Frequency response of 2\textsuperscript{nd}-order type-2 PLL

- Phase-filtering properties (frequency normalized to natural frequency $\omega_n$)
  
  $$H(s) \Rightarrow \text{low-pass filtering}$$
Frequency response of 2\textsuperscript{nd}-order type-2 PLL

- Phase-filtering properties (frequency normalized to natural frequency $\omega_n$)
  
  $E(s) \Rightarrow$ high-pass filtering
Frequency response of 2\textsuperscript{nd}-order type-2 PLL

1. Phase-filtering properties (frequency normalized to loop gain $K_T$)
   $$H(s) \Rightarrow \text{low-pass filtering}$$
Frequency response of 2\textsuperscript{nd}-order type-2 PLL

- Phase-filtering properties (frequency normalized to loop gain $K_T$)
  
  $E(s)$ $\Rightarrow$ high-pass filtering
Frequency response of 2\textsuperscript{nd}-order type-2 PLL

\section*{Asymptotic response}

\begin{equation*}
|H(j\omega)| \approx \begin{cases} 
1 & \omega \ll K_T \\
\frac{K_T}{\omega} & \omega \gg K_T
\end{cases}
\end{equation*}

\begin{equation*}
|E(j\omega)| \approx \begin{cases} 
\frac{\omega^2}{\omega_n^2} & \omega \ll \omega_n \\
1 & \omega \gg \omega_n
\end{cases}
\end{equation*}

- The high-frequency asymptote of $|H(j\omega)|$ rolls off at $-6$ dB/oct, and the low-frequency asymptote of $|E(j\omega)|$ rises at $+12$ dB/oct. The asymptotes are independent of damping $\zeta$.
- Different asymptotic slopes of $|H(j\omega)|$ are produced in PLLs of different orders.
- Different slopes of $|E(j\omega)|$ are produced in PLLs of different types.
Basic PLL topology

- Two waveforms with a skew

\[ V_{\text{CK}} \]

\[ V_{\text{VCO}} \]

\[ \Delta t \]

- Change of VCO frequency to eliminate the skew

\[ V_{\text{CK}} \]

\[ V_{\text{VCO}} \]

\[ V_{\text{cont}} \]

\[ t_1 \]

\[ t_2 \]
• Discussion

- To vary the phase, we must vary the frequency and allow the integration

\[ \phi = \int (\omega_0 + K_{V_{CO}} V_{cont}) dt \]

- Phase alignment can be achieved only by a (temporary) frequency change.

- The output phase of a VCO can be aligned with the phase of a reference if
  - the frequency of the VCO is changed momentarily,
  - a phase detector is used to determine when the VCO and reference signals are aligned.

- Phase locking is a task of aligning the output phase of the VCO with the phase of the reference.
Basic PLL topology (cont’d)

- Feedback loop comparing input and output phases

The PD compares the phases of $V_{out}$ and $V_{in}$, generating an error that varies the VCO frequency until the phases are aligned, i.e., the loop is locked.

The topology must be modified because

- the PD output, $V_{PD}$, consists of a dc component (desirable) and high frequency components (undesirable),
- the control voltage of the oscillator must remain quiet in the steady state, i.e., the PD output must be filtered.
Simple PLL

- A low-pass filter is interposed between the PD and the VCO, suppressing the high-frequency components of the PD output and presenting the dc level to the oscillator.
- The feedback loop compares the phases of the input and output. If the loop gain is large enough, the difference between the input phase, $\phi_{in}$, and the output phase, $\phi_{out}$, falls to a small value in the steady state, providing phase alignment.
- Phase lock condition: $\phi_{out} - \phi_{in}$ is constant and preferably small.

$$\frac{d\phi_{out}}{dt} - \frac{d\phi_{in}}{dt} = 0 \quad \Rightarrow \quad \omega_{out} = \omega_{in}$$

When locked, a PLL produces an output that has a small phase error with respect to the input but exactly the same frequency.
Response of a PLL to a phase step

After the loop returns to lock, all of the parameters, \( \phi_{in} - \phi_{out}, V_{cont}, \) and \( \omega_{out} \) remain their original values.
Response of a PLL to a frequency step

\[ V_{in} \rightarrow PD \rightarrow V_{PD} \rightarrow \text{Loop Filter} \rightarrow V_{cont} \rightarrow \text{VCO} \rightarrow V_{out} \]

\[ \omega_{in} \rightarrow \phi_{in} \rightarrow \omega_{in} \rightarrow \phi_{in} \rightarrow \omega_{out} \rightarrow \phi_{out} \]

\[ V_{in}, \omega_{1}, \phi_{in}, \omega_{2} = \omega_{1} + \Delta \omega, V_{out}, V_{PD}, V_{cont}, \omega_{out} \]

 PLL ICs
Example of phase step response

The control voltage of the oscillator can serve as a suitable test point in analysis of PLLs. While it is difficult to measure the time variations of phase and frequency, $V_{\text{cont}} = V_{\text{LPF}}$ can be readily monitored in simulations and measurements.

The state of the loop:

- At $t = t_2$, the output frequency is equal to its final value but the loop continues the transient because the phase error deviates from the required value.

- At $t = t_3$, the phase error is equal to its final value but the output frequency is not.

For the loop to settle, both the phase and the frequency must settle to proper values.
Conceptual operation of a phase-frequency detector (PFD)

\[ A \rightarrow \text{PFD} \rightarrow Q_A \]
\[ B \rightarrow \text{PFD} \rightarrow Q_B \]

\[ \phi_A \neq \phi_B \]

\[ A \]
\[ B \]
\[ Q_A \]
\[ Q_B \]

\[ \omega_A \neq \omega_B \]

\[ A \]
\[ B \]
\[ Q_A \]
\[ Q_B \]
Charge-pump PLL

Why charge pump PLL?

- Advantages
  - No active component for zero steady state phase error
  - Large frequency and phase capture range
  - Digital output (full CMOS swing)
  - Simple and robust design
  - Discrete time analysis

- Disadvantages
  - Slow comparing with analog PLL
  - May create dead zone problem
  - Noisy
PFD with charge pump

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Simple charge-pump PLL (Type II PLL)

Operation

1. When the loop is turned on, $\omega_{out}$ may be far from $\omega_{in}$, and the PFD and the charge pump vary the control voltage such that $\omega_{out}$ approaches to $\omega_{in}$.

2. When $\omega_{out}$ and $\omega_{in}$ are sufficiently close, the PFD operates as a phase detector, performing phase lock.

3. The loop locks when the phase difference drops to zero and the charge pump remains relatively idle.
   - If $V_{cont}$ remains constant for a long time, the VCO frequency and phase begin to drift. The PFD then detects the phase difference, producing a corrective pulse on up and dn that adjusts the VCO frequency through the charge pump and the filter.
   - Since phase comparison is performed in every cycle, the VCO phase and frequency cannot drift substantially.

- In locked condition, the gain of the PFD/CP combination is infinite, i.e., a nonzero (deterministic) difference between $\phi_{in}$ and $\phi_{out}$ leads to indefinite charge buildup on $C_1$. Therefore, the input phase error must be exactly zero.
**Linearity of PFD/CP/LPF combination**

- The system is not linear in the strict sense.
  - We approximate a discrete-time system by a continuous-time model.
- Approximated by a ramp, $\Delta \phi = \phi_0 u(t)$
  - $V_{cont}(t) = \frac{I_P}{2\pi C_1} t \cdot \phi_0 u(t)$
  - $V_{cont}(s) = \frac{I_P}{2\pi C_1} \cdot \frac{1}{s}$
- It contains a pole at the origin.

**Step response:**

- Approximated by a ramp, $\Delta \phi = \phi_0 u(t)$
  - $V_{cont}(t) = \frac{I_P}{2\pi C_1} t \cdot \phi_0 u(t)$
  - $V_{cont}(s) = \frac{I_P}{2\pi C_1} \cdot \frac{1}{s}$
- It contains a pole at the origin.
Linear model of simple charge-pump PLL

- Open-loop transfer function
  \[ \frac{\phi_{\text{out}}}{\phi_{\text{in}}} \bigg|_{\text{open}} = \frac{I_P K_{VCO}}{2\pi C_1 s^2} \]

Since the loop gain has two poles at the origin, this topology is called a “type II” PLL.

- Closed-loop transfer function
  \[ H(s) = \frac{I_P K_{VCO}}{2\pi C_1 s^2 + I_P K_{VCO}} \]

It contains two imaginary poles at \( s_{1,2} = \pm j \sqrt{\frac{I_P K_{VCO}}{2\pi C_1}} \) and is unstable.
Addition of zero to charge-pump PLL

- **Open-loop transfer function**
  \[ \phi_{out}(s)_{\text{open}} = \frac{I_P}{2\pi} \left( R_1 + \frac{1}{C_1 s} \right) \frac{K_{VCO}}{s} \]
  \( \Rightarrow \) a zero at \( s_z = -1/(R_1 C_1) \).

- **Closed-loop transfer function**
  \[ H(s) = \frac{I_P K_{VCO}}{2\pi C_1} \left( R_1 C_1 s + 1 \right) \]
  \[ s^2 + \frac{I_P}{2\pi} K_{VCO} R_1 s + \frac{I_P}{2\pi C_1} K_{VCO} \]
  \( \Rightarrow \omega_n = \sqrt{\frac{I_P K_{VCO}}{2\pi C_1}} \), \( \zeta = \frac{R_1}{2} \sqrt{\frac{I_P C_1 K_{VCO}}{2\pi}} \) and decay time constant
  \[ \frac{1}{\zeta \omega_n} = \frac{4\pi}{R_1 I_1 K_{VCO}} \]
Stability degradation of charge-pump PLL

\[ \angle H_{open} \]

\[ 20 \log |H_{open}| \]

-40 dB/dec

-20 dB/dec

Lower \( I_p K_{vco} \)

\[ \omega_z \]

\[ \log(\omega) \]

\[ \log(\omega) \]

-90°

-180°

\[ \varphi \]

- \( \frac{2}{R_1 C_1} \)

- \( \frac{1}{R_1 C_1} \)

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Critical drawback:
- Since the charge pump drives the series combination of $R_P$ and $C_P$, each time a current is injected into the loop filter, the control voltage experiences a large jump.
- In lock condition, the mismatches between $I_1$ and $I_2$ and charge injection and clock feedthrough of $S_1$ and $S_2$ introduce voltage jumps in $V_{cont}$.

$\Rightarrow$ The resulting ripple severely disturbs the VCO, corrupting the output phase.
Design flow of 2nd-order PLLs

1. Determine $K_{\text{VCO}}$.
2. Choose the natural frequency $\omega_n$ to be about or less than one-tenth of the input frequency.
3. Select $I_p$, to meet the reasonable trade-off between the value the filter components (i.e., chip area) and the pump current.
4. Set the damping factor $\zeta$ to be 0.707.
5. Calculate $R_1$ and $C_1$. 