DESIGN AND DESIGN METHODOLOGY OF CMOS
GIGAHERTZ FREQUENCY RANGE PRESCALERS

by

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A thesis submitted to the Faculty of Graduate Studies and Research
in partial fulfillment of the requirements for the degree of

Master of Engineering

Department of Electronics

Carleton University

Ottawa, Ontario

June, 1998

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Abstract

This thesis presents the design and design methodology of high speed CMOS dual-modulus frequency prescalers. The prescaler circuits have an application in Fractional-N Division frequency synthesizers for portable and mobile communication systems. The thesis document provides a literature review, reports the design process and formulates a design methodology. This has been done by illustrating a complete design process for a divide-by-31/32 dual-modulus prescaler from logic level design to transistor level design and its actual fabrication. The prescaler is designed completely with dynamic CMOS circuits to achieve high frequency operation as well as low power consumption. The layout related considerations are also reported. The design has been fabricated in Northern Telecom's 0.8µm BiCMOS technology using only MOS devices. The circuit operates from 900MHz to 1880MHz while consuming 17mW at 1880MHz and 5 Volts supply.
Acknowledgments

I wish to thank my supervisor Professor Tad Kwasniewski for his guidance, support and patience during my studies at the Department of Electronics, Carleton University. I also wish to thank Eric Mass and Barry Heim of Motorola for supporting the joint project between Motorola and Carleton University. I would also like to thank the members of the faculty, staff and my fellow students who make the excellent learning environment in the department. Special thanks are due to Sergiy Uhanov whose fine skills made many testing problems easier and also to Anna Kim whose help made many administrative tasks transparent for the research group.

Financial support of Carleton University, the Telecommunication Research Institute of Ontario and Motorola is also gratefully acknowledged. The technical support from Canadian Microelectronics Consortium proved to be a great asset and is also acknowledged.

Finally I would like to dedicate this thesis to my parents whose kindness and love greatly facilitated the motivation for my studies.
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List of Symbols and Abbreviations

- **Power supply**
- **Circuit reference point or ground**
- **NMOS**
- **PMOS**
- **Inverter**
- **AND gate**
- **OR gate**
- **NAND gate**
- **Buffer or amplifier**
- **Resistor**
- **Trimming resistor**
- **Capacitor**
- **Inductor**
- **Diode**
- **NPN BJT**
- **50 \( \Omega \) SMA connector**
A/D .................. Analog to Digital Converter.
BiCMOS ............... Bipolar Complementary Metal Oxide Semiconductor.
BJT ................. Bipolar Junction Transistor.
CMOS ................ Complementary Metal Oxide Semiconductor.
D/A .................. Digital to Analog Converter.
ESD .................. Electrostatic Discharge.
ETDFFF ............. Edge Triggered D Flip-Flop.
FSM .................. Finite State Machine.
HSPICE ............... Circuit Simulator.
IC .................. Integrated Circuit.
LSB .................. Least Significant Bit.
LO .................. Local Oscillator.
MSB ............... Most Significant Bit.
PCS ................ Public Communication Services.
PLL ................ Phase Locked-Loop.
PPM ................ Parts Per Million.
Q ...................... Quality factor of a reactive element or oscillator.
RF ..................... Radio Frequency.
ROM ................... Read Only Memory.
SF ..................... Speed Figure (of a flip-flop).
SOI ..................... Silicon on Insulator.
TSPC ................... True Single Phase Clock.
VCO ..................... Voltage Controlled Oscillator.
VLSI .................... Very large Scale Integration.
CHAPTER 1

Introduction

1.1 Introduction

The exponential growth of the PCS services in the last decade poses a strong technological challenge for the telecommunication industry to reduce the cost while satisfying the standards requirements relating to the frequency of operation and performance. It is still not clear which I.C. fabrication technology or technologies will dominate the PCS devices manufacturing in the near future but there are strong indications that CMOS technology will successfully compete with high performance technologies such as high-speed Bipolar, GaAs, SOI and SiGe. CMOS technology in the past has been taken as a slow technology fit for low-frequency baseband signal processing. However, recent advances in this technology into deep sub-micron geometries have pushed the maximum frequencies of the device to well above fifty gigahertz as has been demonstrated for the 0.1μm CMOS devices. Therefore such advances have induced renewed efforts to design RF circuits in CMOS and several research institutions as well as the telecommunication industry are endeavoring to build all CMOS single chip transceivers [1,2].

The application of CMOS technology in RF design is fairly new and literature on
design methodology has only started to address the related issues. The trade-offs for the specific building blocks for the RF front end of a radio transceiver have not been fully examined [3]. One of the basic components of a transceiver front end is the frequency synthesizer, most commonly a PLL frequency synthesizer. This thesis focuses on the frequency divider which is one of the most critical circuits in a PLL synthesizer. It is critical because it is one of the two components in the phase-locked loop which operates at highest frequencies and consumes more power as compared to the rest of the loop components. Therefore efforts to reduce power consumption while maintaining high frequency operation are worthwhile.

1.2 Thesis Motivation

Present day wireless communication applications are aiming towards higher frequencies because of problems such as channel congestion to accommodate the need of increased bandwidth for higher data rates and more users. This calls for fast circuits but at the same time they must be inexpensive and dissipate less power. These are somewhat contradictory requirements since faster circuits tend to consume more power and high performance microelectronics technologies are not cost-effective. Therefore in determining the performance criteria for frequency prescalers the factors of cost, power dissipation and operating frequency are the primary ones. With the advancements in CMOS technology, it is becoming possible to design high speed circuits for RF applications better than before. Hence integrating most of the RF circuits on the same chip as the one with baseband processing circuits has a definite advantage to avail and, that too in the cost-effective CMOS technology.
Frequency synthesizers in wireless systems differ in requirements depending on a specific application. PLL frequency synthesizers are commonly used in modern communication systems. These applications frequently switch channels during operation and systems such as CDMA require fast switching times between different frequencies. Of several frequency synthesizers, Fractional-N synthesis technique has become common for such systems. This technique allows simple dual-modulus frequency prescalers to be used in the PLL for frequency synthesis whereas programmable or multi-modulus prescalers are slow and more complex. In Fractional-N PLL frequency synthesizers, the dual-modulus prescaler divides the incoming frequency from the oscillator by an integer N or N+1 depending on a single control bit. By appropriately switching the division ratios, any frequency multiple of a real number lying in the range of N and N+1, can be theoretically generated. Dual-modulus prescalers are simpler and smaller in physical size than their programmable counterparts. Simpler and smaller circuits, as a consequence, also consume less power and are cheaper. Fast operation both in terms of high operating frequency and frequency switching, simple circuits and small silicon size, are the key requirements for frequency prescaler design for high speed frequency synthesizers.

Next, a dual-modulus prescaler must satisfy the requirement that switching from one division ratio to the other and vice versa, be smooth between output cycles i.e. phase coherency must be observed. If this condition is not met, any unnecessary pulse generated at the output can cause a large phase error and may even throw the loop out of lock. This has to be avoided through careful circuit design.

With the above mentioned criteria, the design of dual-modulus prescaler circuit
Introduction

poses a challenging task. Further, the choice of the technology for integrating the circuit is critical and directly affects the factors mentioned above. In consideration of these criteria, this thesis deals with the problem of dual-modulus frequency prescaler circuit design and satisfies the following:

- high operating frequency,
- wide operating frequency range,
- CMOS implementation,
- switchable between two ratios keeping phase coherency,
- reduction in power dissipation by using true single phase clock dynamic CMOS circuits.

In addition to above, a design methodology is described which allows to examine a dual-modulus architecture using conventional logic design methods because digital frequency dividers are essentially sequential logic circuits. Once an architecture is chosen, it can either be exported directly to a specific technology using IC synthesis tools such as Synopsys for general applications, or the designer can customize the needed flip-flop circuits under certain specifications by optimizing them for speed or power requirements. The architecture used in the design is taken further for implementation in state-of-the-art CMOS technologies. For this purpose an optimization methodology for the chosen CMOS circuits, i.e. dynamic circuits, is also proposed. The proposed methodology takes its idea from event-driven simulation algorithms and allows to optimize a circuit for the given requirements.

This thesis shows that conventional frequency divider architectures can be implemented using dynamic CMOS circuits to cut down power and can be designed to operate
at frequencies as high as 1.9 GHz while maintaining a wide frequency range of operation and consuming only 17 mW @ 1.9 GHz with a supply voltage of 5 Volts and at 3 Volts supply, takes only 3.5 mW with a maximum operating frequency of 1200 MHz.

1.3 Contributions

The thesis contribution is in the formulation of design guidelines for CMOS prescalers. The application of the design methodology resulted in construction and laboratory performance evaluation of prescaler circuits in two distinct CMOS technologies. Significant improvements over previously reported performance figures have been achieved.

1.4 Thesis Outline

The thesis is organized in the following manner.

Chapter 2 presents some aspects of frequency synthesis including synthesis techniques. Chapter 3 provides a background of selected frequency division techniques, both analog and digital. Then it goes on to describe the logic design of the frequency divider or prescaler for this work. The logic design forms the base architecture for implementing the design. Various flip-flop circuits which can be used to implement the design are presented in chapter 4, which also describes timing issues related to the flip-flops. It also explains the transistor level design and speed-optimization of the D flip-flop circuits used for the two-stage frequency divider. Chapter 5 then presents the implementation of the design in two different CMOS technologies and performance evaluation of the circuits. Chapter 6 then outlines the conclusions drawn from the research, some important issues and proposes related future research.

Design and Design Methodology of CMOS Gigahertz Frequency Range Prescalers
2.1 Introduction

The last decade has witnessed a rapid growth of wireless communications products both in consumer market as well as in commercial sector where the major stimulation has come from the consumer side. Fast advancements in sophistication of wireless circuit design and technology as well as reduced costs have led to a remarkable miniaturization of wireless products resulting in their increased acceptance in society. The explosive growth has put a considerable demand on the already congested frequency band allocations. To accommodate an ever increasing number of users, several solutions have been proposed. The basic techniques being an efficient use of bandwidth, reducing the channel spacing and/or to move towards higher frequencies [4]. Modern digital modulation schemes make an efficient use of bandwidth while employing frequency reuse plans however, channel spacing cannot be reduced beyond a certain limit.

As mentioned before, an obvious solution to the channel congestion problem is to move towards higher frequencies. There are more than one reasons that interest and activity in wireless communications systems is occurring at frequencies below 2 GHz [4, 5]
although, higher frequencies are also being investigated. For one reason it is noted that at higher frequencies RF signals attenuate rapidly in the atmosphere as well as in the buildings. Secondly, advancements in IC technology has pushed the transistor operating speeds, \( i.e. f_T \)'s, well above 10 GHz. Perhaps the deciding factor is more economical than technological. While signal attenuation can be overcome by increasing signal power, this is only at the cost of a rapidly drained portable unit battery to which consumers happen to be quite sensitive. Moreover, today’s RF and microwave technologies for frequencies above 2 GHz are both sophisticated and relatively expensive, leaving more mature silicon bipolar, CMOS or BiCMOS technologies as the major choices for portable units.

The CMOS technology has proved itself to be excellent for baseband signal processing being mature and cost-effective, while bipolar devices, being inherently faster, have been the choice for RF circuit design. BiCMOS was seen as one answer to integrate RF and baseband circuits on the same substrate. However, increased speeds of CMOS transistors due to reduced geometries is now allowing the most mature and inexpensive CMOS technology to be explored as a candidate for RF circuits in the range of 2 GHz [5, 6].

2.2 Frequency Synthesizer Characterization

Frequency synthesizers are the essential building blocks in all wireless communication systems. Communication standards impose strict requirements to control the radiation in the channels. With channel spacing as small as 30 kHz, not only narrow-bandwidth bandpass filters are needed but the spectral purity of the synthesizers is also crucial [7]. Ideally a signal source produces a pure sinusoidal signal. Under different operating condi-
tions of load, bias or temperature, the phase, frequency or amplitude of the source should not change [8]. However, practical frequency synthesizers deviate from the ideal behavior. Therefore, a number of performance criteria have been defined over the years to characterize frequency synthesizers. Details of which can be found in the literature and will be summarized here [8, 9].

2.2.1 Phase Noise

Phase noise is a measure of short term stability of frequency sources. Short term stability in turn, is a measure of frequency variations about the nominal frequency that occur over time periods of a few seconds or less. It can be divided into two types: non-random and random type of variations. The non-random frequency variations are periodic or discrete signals which can be observed on an RF spectrum analyzer and are commonly known as spurious signals. The sources of spurious signals are usually known. On the other hand, the second type of short term stability is random in nature and is generally known as phase noise. The sources of phase noise include thermal noise, flicker and shot noise of active and passive devices [10].

An ideal sinusoidal signal in the time domain can be mathematically described by the Equation 2.1 below,

\[ S(t) = A \cos(\omega_0 t) \]  

Where \( A \) is the amplitude and \( \omega_0 \) is the carrier frequency in rad/s. In frequency domain this signal appears as a single spectral line. In the real world however, unwanted amplitude and frequency fluctuations can cause the signal to deviate from its ideal form [8]. The signal then no longer remains a single spectral line but becomes distributed above
and below the carrier frequency in the form of sidebands as shown in Figure 2.1. Such a signal can be represented as [11, 12],

\[ S(t) = [A + a(t)]\cos(\omega_c t + \phi(t)) \]  

where \( a(t) \) is the amplitude fluctuation function and \( \Phi(t) \) denotes the phase fluctuations. For negligible amplitude variations, which is usually the case for high quality oscillators, \( a(t) \) can be ignored and the amplitude of \( S(t) \) can be considered to be constant. Then, all the noise is due to phase fluctuations and mathematically can be represented as below,

\[ S(t) = A \cos(\omega_c t + \Delta f - \sin \omega_m t) = A \cos(\omega_c t + \theta_p \sin \omega_m t) \]  

where \( \Delta f \) is the frequency deviation, \( f_m \) is the offset frequency from the carrier and \( \theta_p \) is the peak phase deviation. For \( \theta_p \ll 1 \), \( S(t) \) can be expressed as Equation 2.4 below.

\[ S(t) = A \cos(\omega_c t - \frac{\theta_p}{2} \cos(\omega_p + \omega_m)t + \frac{\theta_p}{2} \cos(\omega_p - \omega_m)t) \]  

The above relation shows that when peak phase deviation is small, signal \( S(t) \) has frequency components on each side of the carrier with an amplitude of \( \theta_p/2 \). The phase noise is commonly viewed in terms of spectral power density which is the power contained in 1 Hz bandwidth at a particular offset frequency. Due to symmetry in distribution around the carrier frequency, only one side is usually shown in phase noise specifications of frequency synthesizers and is known as single sideband phase noise or SSB noise. Specifications of signal sources usually give sideband noise in 1 Hz bandwidth as \( L(f_m) \) dBc/Hz, which is the ratio of the signal sideband noise power in 1 Hz bandwidth to the total signal power at an offset of \( f_m \) Hertz from the carrier. Magnitude of \( L(f_m) \) is given by
Phase noise of a signal source is one of the most important and often the limiting factor for an application. Different applications according to their performance level, require different phase noise specifications [10, 13]. For a doppler radar, for example, phase noise specification is very important from only a few hertz from the carrier whereas for mobile communications, it is important at a few kHz from the carrier. Therefore the selection of a signal source is very much application driven. Figure 2.2 shows the regions where phase noise is important for different classes of RF and wireless applications.

2.2.2 Power Output and Stability

This figure of merit is usually given as a power output range in dBm at a given frequency and over a temperature range.

2.2.3 Tuning Range

The tuning range of a signal source specifies the change in the output frequency with the change in the control voltage or current and is given by its tuning curve depicting...
output frequency variations versus input control voltage or current. For a VCO the slope of
the tuning curve is expressed in MHz/V as the gain constant $K_{vco}$ of the VCO. The tuning
curve of a VCO is usually nonlinear over its entire range and the VCOs are usually
designed so that the slope of the tuning curve is linear over the required range of operation
which might be about only 10%-20% of the total range. The VCO gain constant is also a
contributor to phase noise in the synthesizer, a higher $K_{vco}$ usually would mean a higher
phase noise.

2.2.4 Frequency Stability

This parameter expresses the frequency drift of the oscillators with temperature
and is usually specified in ±PPM/°C. Frequency stability is more important in a free run-
ning system, whereas in a PLL, a drifty oscillator can be locked to a more stable low fre-
quency oscillator. Frequency drift in oscillators is also caused by supply voltage changes,
process variations, aging and environmental factors.
2.2.5 Harmonics and Spurious Outputs

Nonlinearity of the active devices produce harmonics in the output of the synthesizers or oscillators. Harmonics can be minimized by proper biasing of the active devices, through filtering and matching networks. Other output signals present at the output of the synthesizer and not harmonically related to the fundamental frequencies are called spurious outputs and their presence is a major limitation in direct digital synthesis. Power spectral density of harmonics and spurious outputs relative to the carrier power is typically specified as dBc/Hz at an offset frequency from the carrier frequency.

2.3 Types of Frequency Synthesizers

Generally, synthesizers can be divided into two categories, direct or indirect frequency synthesizers. Direct frequency synthesizers do not use feedback and are further subdivided into Direct Analog or Direct Digital Synthesizers. Indirect Frequency Synthesizers generally use feedback in the form of PLL. These can be either Linear PLLs, Digital PLLs or Software PLLs. Selected types are described here briefly while their detailed description can be found in several references [7, 8, 9, 12, 14].

2.3.1 Direct Analog Synthesizers (DAS)

Using analog techniques, direct analog frequency synthesis technique generally utilizes fixed, precise frequency sources to generate the required output signal frequency. The approach uses frequency multiplication, division, switching, mixing and filtering to generate the output frequencies [9]. Although this method is conceptually straightforward and provides high performance in terms of output frequency switching time, resolution etc., it has a number of drawbacks if a fine output frequency control with multiple output
frequencies is required. The major drawback is that the physical size and complexity of the circuits becomes daunting. Also, the nonlinear circuits generate spurious responses which must be filtered out, thus requiring more circuitry. Such drawbacks make this technique unsuitable for IC fabrication and thus, for mobile units where not only the physical size is a limitation but power consumption is also critical. A typical form of a DAS is shown in Figure 2.3.

\[
\frac{f_3}{N_2} \times \rightarrow \text{BPF} \rightarrow \frac{1}{N_1} \times \rightarrow \text{BPF} \rightarrow f_0
\]

\[
f_2 = \frac{f_1 + f_3/N_1 + f_3/N_1N_2}{N_1 = N_2 = 10 \text{ typically.}}
\]

Figure 2.3: A form of Analog Frequency Synthesizer

2.3.2 Direct Digital Synthesizers (DDS)

Direct digital frequency synthesizers use digital components to generate a variety of frequencies from a single reference clock. As shown in Figure 2.4, a typical DDS consists of an N-bit phase accumulator, a sine lookup table in a ROM, a digital to analog converter and a bandpass filter. A W-bit frequency word determines the output frequency which is cleaned up by the bandpass filter. This is necessary since the output of the D/A converter is only an approximation of a sine wave.

Figure 2.4: Direct Digital Frequency Synthesis
Due to an all digital approach, high precision is obtainable. Other advantages are that it avoids the use of analog tuning components and there is no frequency drift. The major drawback with this technique is that the output frequencies are always smaller than the clock frequency, typically half of the clock frequency.

### 2.3.3 Indirect Frequency Synthesizers

The indirect frequency synthesis technique uses some form of feedback for the generation of output frequencies. Usually phase-locked loops are employed while frequency-locked loops are also used but are less popular because of the reasons such as more complex design, poorer loop stabilities and noise suppression, and loose locking conditions as compared to the phase-locked loops [9]. A simple PLL block diagram is shown in Figure 2.5. The general operation is as follows. The VCO generates a signal of frequency $f_o$. This frequency is scaled down by the divide-by-$N$ frequency divider and is fed to the phase detector input. The other input to the phase detector comes from a reference source of frequency $f_r$. The phase detector compares the phases of the two signals $f_r$ and $f_o/N$ to generate a phase error signal which is proportional to the difference between the respective frequencies. The output signal of the phase detector is a series of pulses which are filtered by a low pass filter to provide the equivalent dc value to the control or tuning input of the VCO. This closes the loop and depending on the phase error, the VCO is pulled towards the frequency $Nf_r$.

From the above description and Figure 2.5, it can be seen that in order to generate multiple frequencies with fine resolution, one can either change the reference frequency or the division ratio $N$. However, there are a number of considerations which must be kept in
mind. First one is that if \( f_r \) is to be varied, then it must be small, of the order of a few tens or hundreds of kilohertz, depending on the particular communication system channel spacing. Since for portable wireless applications, the VCO would be running at frequencies in the range of 1-2 GHz, the division ratio \( N \) has to be very large. This increases the settling time of the loop beyond practicality. There are two popular techniques which are used for frequency synthesis with fine resolution, namely multi-loop and fractional-\( N \) division frequency synthesis. For several reasons the former is not very suitable for monolithic integration of portable communication components. First, the circuits are complex (more expensive and power consuming) and secondly, isolation is necessary between the individual loops and last but not the least, the presence of spurious spectral components due to non-linear circuit elements such as mixers. The latter technique \textit{i.e.} the fractional-\( N \) division, being simpler and inexpensive, is considered to be more suitable for the purpose and is described next.
2.3.4 Fractional-N Division Frequency Synthesis

The fractional-N division frequency synthesis technique uses a phase-locked loop to generate frequencies which are not only an integral but also fractional multiples of the reference frequency. This is done without resorting to multiple loops. As it is known that if the divide-by-\( N \) counter in the simple PLL is replaced by a programmable divider then frequencies in increments of \( f_r \) can be synthesized. If the divider is made to divide by only two ratios say \( N \) and \( N+1 \), then the VCO can be locked either to a frequency \( Nf_r \) or \( (N+1)f_r \). Fractional-N division technique utilizes this fact and by switching the division ratio between \( N \) and \( N+1 \) every few cycles of reference frequency, the PLL can generate frequencies which are a multiple of a real number between \( N \) and \( N+1 \). However, the fractional relation of the input and output frequencies is only on the basis of time average. This is because the divider, which is essentially a digital device, scales down the input frequency by counting the input signal transitions or edges particularly on either of the rising or falling edge. Therefore only an integer number of periods can be counted. The fractional-N technique uses a divider capable of dividing the input frequency by two ratios \( N \) or \( N+1 \). By switching the modulus for different number of cycles, the average output frequency can be a fractional multiple of the reference frequency [8, 9, 14, 15, 16].

To illustrate the above, with reference to Figure 2.6, note that the divider is controlled by a single bit input. The modulus controller can thus switch the modulus by putting a bit stream at this input as desired. The controller works in such a way that it keeps the divider ratio to \( N \) for \( p \) cycles of \( f_r \) and to \( N+1 \) for \( q \) cycles of \( f_r \). This is done in a
Figure 2.6: Fractional-N Division Frequency Synthesis

sequence and the total number of cycles in the sequence is thus \((p + q)\) \([15]\). Hence the input and output frequencies in Figure 2.6 can be related as,

\[
f_o = \frac{p \cdot N + q \cdot (N+1)}{p + q} f_r = \left( N + \frac{q}{p+q} \right) f_r
\]

It is usual to denote the above fractional relationship as \(N.F\) where \(N\) is the integer part and \(F\) is the fractional part \(i.e. q/(p+q)\). Thus by properly selecting the number of cycles \(p\) and \(q\), any fraction can be generated. As a simple example if \(N = 31\) and \(p = q\), then \(f_o = 31.5 \cdot f_{in}\) or if it is desired to generate a frequency of \(31.496 f_r\), then \(N = 31\) and \(F=0.49\). From this it can be deduced that \(q = 49\) and \(p = 51\). In Figure 2.7, such a sequence is shown with \(p = q = 1\) along with the ideal waveform with a division ratio of \(2.5\) for \(N/(N+1) = 2/3\). It is important to point out that due to modulus controller limi-
tions, not all fractions can be synthesized and typically the range is somewhat restricted between 0.25 to 0.75, i.e. only a 50% part of the full scale [17].

![Diagram of N/(N+1) Division of a Waveform](image)

**Figure 2.7: N/(N+1) Division of a Waveform**

### 2.4 Phase Jitter Reduction Techniques for Fractional-N Synthesizers

The fractional division technique is simple and lends itself quite easily for monolithic integration however, it is not without shortcomings. The most important one is that there is a phase jitter present at the output of the divider which degrades the phase noise performance of the loop [15, 17]. As shown in the Figure 2.7, the ideal waveform has a period of $N \cdot F \times T_o$, while the actual period is $N \times T_o$ when dividing by $N$ and $(N+1) \times T_o$ when dividing by $N+1$. When comparing to the ideal waveform, it can be seen that each deviation from the ideal would produce a phase error step at the output of the phase detector. The time error for both cases is given by,

$$
\Delta t_N = N \cdot F \times T_o - N \cdot T_o = F \times T_o
$$

$$
\Delta t_{N+1} = N \cdot F \times T_o - (N+1) \cdot T_o = (F-1) \times T_o
$$

Assuming that $N.5$ gives a zero phase-error, each division by $N$ introduces a posi-
tive phase error step \((N.F > N)\) and each division by \(N+1\) results in a negative phase error step \((N.F < (N+1))\). This appears as a periodic staircase voltage waveform at the output of the phase detector superimposed on the average phase error voltage as shown in the Figure 2.8. This is an undesirable effect and results in a periodic modulation of the VCO output and degrades its spectral purity since, only the dc voltage is required to keep the VCO at the right frequency. A very narrow bandwidth of the loop filter can minimize this effect but settling time would suffer. Several phase jitter cancellation scheme has been proposed in the literature, for example:

- Digital Phase Accumulator technique,

- Pulse Delay Compensation,

- Level Sampling technique,

- Jitter Injection technique,

- Noise Shaping technique.

Of the above, only the Digital-phase accumulator and Noise shaping methods of phase jitter cancellation or reduction will be described here. Other methods either suffer

![Figure 2.8: Phase Error Voltage due to Phase Jitter](image)
from difficulties in practical implementation or are not very reliable, comprehensive
details of which can be found in the literature [15].

2.4.1 Digital-Phase Accumulator Technique

Before going into the details of digital phase accumulator technique, it is imperative
to know how the dual-modulus divider is controlled. The control block for this pur-
pose consists of an L-bit adder and a register which is clocked by the reference frequency
and is shown in Figure 2.9 in block diagram form. Assuming that the divider divides the
frequency at its input by $N$ when its modulus control bit is at logic ‘0’ and by $N+1$ when at
logic ‘1’. The adder has a carry-out or an overflow output which is used to control the
divider. Whenever the capacity of the adder is exceeded, the current content of the adder is
decreased by an integer equal to the adder capacity. An L-bit word $K$ is input to the adder
and at each reference period the register is incremented by a value $K$. Thus, each time an
overflow occurs the accumulator value increases by $K-M$, where $M = 2^L$. Each overflow
causes a division by $N+1$ and when there is no overflow the division ratio remains at $N$. It
can be seen that the accumulator contents at any time are proportional to the phase error. It
is because of this property that this scheme is known as Digital Phase Accumulator or
Digi-Phase technique.

Since the phase error is known at any time, the contents of the accumulator can
then be used to cancel the staircase (Figure 2.8) waveform which causes the phase jitter. In
its simple form the cancellation scheme is shown in Figure 2.10. It consists of a D-to-A
converter and a summer. The contents of the accumulator are converted to analog form,
properly scaled and phased, and then added to the output of the phase detector. Thus only
the required dc value goes ahead in the loop. The practical limitations of this method include converter and summer inaccuracies and also, the cancellation waveform has to be synchronized with the phase detector output.
2.4.2 Noise Shaping Method

Oversampled Sigma-Delta modulation is well known for its noise shaping properties. The noise transfer function in a linearized model of a sigma-delta modulator has a high pass characteristic while the signal transfer is a low pass response. Thus noise can be transposed far away from the band of interest by oversampling. Also, because of the similarities between the digital phase accumulator and a first order sigma-delta modulator, these modulators can be employed in fractional division PLLs. For further improvement in noise attenuation, higher order sigma-delta modulators can be used. This results in better noise filtering and shaping towards higher frequencies as well as decorrelation of noise from the signal.

2.5 Summary

The discussion in this chapter focussed on some important background information on frequency synthesis. A few frequency synthesis techniques were presented. Useful detail of one popular technique, i.e. Fractional-N Division, was given and its properties were highlighted. This technique is becoming popular because of its simplicity and feasibility of monolithic integration. One drawback of this technique, phase jitter due to modulus switching, was explained and methods for its reduction were also described.
CHAPTER 3

Frequency Dividers, Overview and Design

3.1 Introduction

In the previous chapter an overview of popular frequency synthesis techniques was presented. Of the principles mentioned, indirect synthesis using PLL based fractional division technique was seen to be the most suitable one for the mobile communications systems. As the focus of this thesis is frequency division, this chapter begins with an introduction of various frequency division techniques with an emphasis on digital dividers, then the logic design of dual modulus dividers is described.

In a PLL synthesizer, of all the PLL components, circuit design of the VCO and the frequency divider is very critical. The reason partly comes from the fact that these components operate at the highest frequencies within the PLL and also consume most of the power as compared to the other components. With the PCS channel allocation frequencies approaching microwave regions, the designers of VCOs and dividers for RF IC's face the problem of insufficient knowledge [6]. Several problems are being faced by the PLL designer. One of the major ones is that with rapidly advancing technologies and most of the designs being done through computer simulation, the designer often doesn't have reliable and accurate device models. As an example, if a VCO is designed with a center fre-
frequency of 915 MHz and tuning range of ±30 MHz, an error of 10% can move the centre frequency down to 800 MHz or above 1 GHz. Thus, in such cases either several design iterations must be carried out or several designs must be fabricated simultaneously.

A similar situation exists when design of frequency dividers for PCS applications is undertaken. Divider circuits for very high frequencies using microwave technologies such as GaAs, typically take more power and die area than it is allowable for portable units. Other methods use external or on-chip $L$ and $C$ components. Those are limited in many aspects such as cost, silicon size, range of operation, matching problems etc. The following section reviews different classes of frequency dividers, their advantages and limitations.

### 3.2 Frequency Dividers

The frequency divider is a key component in a PLL synthesizer for the translation from high to low frequencies. There are many types of circuits that can perform frequency division and different applications impose different requirements on the divider, however, none of the circuits meet all the requirements simultaneously. Some of the basic requirements are as listed below [14, 18]:

- high operating frequency,
- wide range of operation,
- high division ratio,
- variable and controllable, manually or electronically, division ratio,
- no RF signal in the absence of input signal,
- low cost.
In the following paragraphs, common types of frequency dividers are described briefly.

### 3.2.1 Regenerative Frequency Dividers

Regenerative frequency dividers use nonlinear circuits like mixers and frequency multipliers to divide the input signal frequency by an integer $N$ [18]. As shown in Figure 3.1, the input signal is fed into the LO input of the mixer and the RF input is fed from the multiplier which multiplies the output by $(N-1)$. Thus the input and output signal frequencies are related by,

$$f_o = f_{in} - f = f_{in} - f_{in} \cdot \left(\frac{N-1}{N}\right) = \frac{f_{in}}{N}$$

For the circuit to work, the loop gain must be greater than unity and the only sustainable output is $f_{in}/N$. Regenerative frequency dividers can operate at very high frequencies and in the absence of input signal $f_{in}$ there is no RF signal at the output. However, there are certain other disadvantages associated with such circuits. The mixer and the multiplier need to be driven hard requiring RF amplifiers. Besides, bandpass filtering is also essential. The structure itself is not self starting and a high transient voltage amplitude is
usually needed to start it. The operating frequency range is narrow and high division ratios are not practical. For such reasons regenerative frequency dividers are not suitable for frequencies below 1 GHz.

### 3.2.2 Frequency Division by Injection Locking

In injection locking frequency division, also called *subharmonic triggering*, [12, 19], a mistuned oscillator is locked to a subharmonic of an injected signal, where the injected signal is an Nth harmonic of the oscillator free-running frequency. The performance of such a divider is usually evaluated in terms of *oscillator mistuning* and *capture range*. The degree of oscillator mistuning is the difference between the free running frequency of the oscillator and the locked frequency. The capture range is the maximum oscillator mistuning at a given injected RF power, division ratio and bandwidth of the tank circuit in the oscillator. Normally higher division ratios and high $Q$ of the tank circuit mean higher injected power into the oscillator.

Locked oscillators do not impose limits on the frequency of operation and may be implemented with relatively low cost. However their disadvantages are that the operating frequency range is narrow and there is always an RF signal with no input signal present resulting in wastage of power. But in a PLL, where the oscillator is stays on all the time, an injection locked oscillator will also stay locked.

### 3.2.3 Carrier Storage and Parametric Frequency Dividers

The carrier storage and parametric frequency dividers [18, 20] are relatively inexpensive and can operate well into GHz region, however it is difficult to obtain division
ratios higher than 2. Both types are similar in nature and are represented by the block diagrams in Figure 3.2, where the input and output networks isolate the signal from the load and vice versa.

![Block diagram of Carrier-Storage divider](image)

![Block diagram of Parametric divider](image)

Figure 3.2: (a) Carrier-Storage divide-by-two frequency divider
(b) Parametric divide-by-two frequency divider

The carrier storage divide-by-2 circuit uses a step recovery diode as a charge controlled switch. It closes when voltage across the diode drives it into forward conduction region and opens during reverse recovery process. During the transition phase, the voltage pulse developed across the diode isolates it on the following cycle of the input by changing the recovery delay. This way division by 2 is obtained.

The parametric divide-by-2 circuit can be described by a negative conductance generator such as a varactor diode. It presents a negative conductance to an external circuit tuned to output frequency whenever an RF voltage at twice the frequency appears across the diode.
It is clear from the block diagram in Figure 3.2 that these type of frequency dividers, which require $L$ and $C$ components, are not feasible for monolithic integration for RF IC's for mobile radio applications.

### 3.2.4 Phase-Locked Loop Frequency Dividers

In a phase-locked loop, the frequency divider block can be visualized as a frequency translator function block [9, 18]. The output of the PLL may then be specified as the inverse of the translator function. If this function is a frequency multiplier, then PLL will produce an output which is an inverse of multiplication function *i.e.* frequency division. However, PLL frequency dividers are not popular because they don't offer any extra advantages over other circuits and are relatively expensive.

### 3.2.5 Digital Frequency Dividers

Digital frequency dividers are the most popular divider structures in use today. The advancements in technology have made it possible to build digital frequency dividers operating up to 15 GHz or more. Not only are the digital logic design methods fairly well established but digital frequency dividers also offer the flexibility of programmability, high division ratios and easier digital control [21, 22].

The fundamental element of a digital frequency divider is a flip-flop, typically composed of two level-sensitive latches in a master-slave configuration to form an edge-triggered flip-flop. The basic principle behind their operation is that of finite state machines. Digital dividers count input clock signal transitions either from high-to-low or vice versa. This is the same as counting the clock periods or in other words, the clock fre-
frequency. Thus by counting specific clock periods, while skipping others on purpose, any function of period-counting may be implemented. Although the terms *frequency divider* or *frequency counter* may refer to the same logic circuit, the difference between the two is that for counting purposes, all the bits from the counter are taken out as the output digital data (in parallel) while in a frequency divider usually a single bit output is taken, typically from the last flip-flop stage. The terms *divider* and *prescaler* will be used interchangeably in this text and their division ratio being fixed or variable will be clear from the context.

Generally, dividers can be classified into two types, synchronous and asynchronous frequency dividers [8, 23]. In synchronous dividers, all the flip-flops evaluate their respective states on the same clock edge. On the other hand, in asynchronous dividers, the clock signal triggers the first flip-flop, the output of the first flip-flop triggers the second flip-flop and the change flows or ripples down the flip-flop chain. Both types of the dividers have their own advantages. Synchronous dividers are inherently faster since the states changes occur almost simultaneously on the same clock edge but the division ratio is relatively low. Whereas asynchronous dividers provide higher division ratios but are slower because the changes from one flip-flop to the next do not reach until the previous one is settled. Also, the output of the asynchronous dividers is not synchronized with the input clock signal and may contribute to the overall phase-noise, therefore, a usual solution is to logically AND the output with the input to bring the output in synchronization with the input [15, 23].

The speed and power performance of a digital divider depends on the technology used, type of the logic involved and circuit topology employed [22]. Silicon Bipolar and GaAs technologies offer higher speed while consuming relatively more power while...
CMOS technology is generally slow but takes much less power. The circuits themselves can be either static or dynamic in CMOS technology. Static circuits are more robust and provide broadband operation but are slow while CMOS dynamic circuits can go to higher frequencies but work only in a limited range of frequencies.

As mentioned earlier, high speed circuits are needed for PCS applications. For fractional-N frequency synthesis the pulse swallowing technique is a widely used one which is not only simple but also suitable for monolithic integration [9, 18, 22]. It is shown in Figure 3.3 and uses a variable ratio prescaler, typically a dual-modulus one, which can divide by two integers $N$ or $N+1$. In addition to this, there are two more counters, a swallow counter and a program or reference counter. The swallow counter can count up to $N_s$ and the program counter counts up to $N_p$ cycles of $f_I$ where $N_p \geq N_s$. Initially both counters are reset to their respective zero states. The operation is described as follows. The dual-modulus prescaler is set to divide by $N+1$. Both counters start counting and after $N_s$ cycles of $f_I$, the swallow counter generates an output which changes the prescaler.
Frequency Dividers, Overview and Design

calor ratio to $N$ and at the same time inhibits the swallow counter to count any further. However, the program counter continues to count and does not stop until it has counted $N_p$ cycles. At this time both counters are reset and the cycle repeats. The output frequency is then given by,

$$f_{in} = (N_S + N_p \cdot N) \cdot f_{out}$$

Thus any division ratio $R \geq N(N-1)$ can be obtained.

### 3.3 Logic Design of Dual-Modulus Frequency Prescalers

In this work, the design, implementation and performance of CMOS dual-modulus prescaler is presented. Several dual-modulus prescaler architectures have been proposed in the literature, most of which aim to achieve high speed and low-power consumption with optimized technologies or innovative design techniques [14, 22, 24, 25, 26, 27]. A conventional architecture, shown in Figure 3.4, consists of two stages which are joined together.

![Figure 3.4: Dual-Modulus Divider Block Diagram](image)

**Figure 3.4: Dual-Modulus Divider Block Diagram**

*Design and Design Methodology of CMOS Gigahertz Frequency Range Prescalers*
by a state-detector logic or glue logic. The glue logic detects specific logic states to force a state transition different from the state to which it would have come otherwise, and thus controls the division ratio depending on the input signal at $MC$. The first stage is usually a synchronous or Johnson counter structure which can divide the input by an integer $P$ or $P+1$. The second stage is an asynchronous one and is a fixed ratio ripple counter. A Johnson counter being inherently faster, is employed as the first stage. It can be designed with minimal logic to divide by two ratios but can only provide a maximum division ratio of $2n$, where $n$ is the number of flip-flop stages. Once the frequency has been scaled down to an appropriate figure, it is further scaled down by the second stage which can provide higher division ratios up to $2^n$ where, once again, $n$ is the number of flip-flop stages.

In this work, the target frequency range was chosen to be 1000 MHz after simulations of the circuit with the selected flip-flops at the schematic level in Northern Telecom's 0.8μm BiCMOS technology using only MOS devices. One aim was the speed optimization of the circuit while sacrificing some power dissipation. A compromise was also reached when deciding on the modulus of the divider since it is difficult to measure high frequency signals from a packaged IC. The frequency can be divided down to an appropriate number but considering testability, if the circuit fails, any errors in the failed circuit are difficult to trace due the complexity of the circuit. Therefore a ratio of $31/32$ was chosen so that the output frequencies lie in the range of 30 MHz which are relatively easy to measure while allowing the circuit to be moderately complex. Although the logic design techniques are well established, design methodology is described here in order to analyze the prescaler architecture. This involves the use of state-diagrams, state-tables and Boolean expressions, followed by logic level simulation of the logic circuit using software tools.
such as Synopsys. Several architectures can be generated and analyzed by writing VHDL code however, only the preselected architecture is presented here.

### 3.3.1 First Stage Design

In a radio front end local oscillator, assuming a PLL frequency synthesizer, the VCO output is capacitively loaded by a mixer and the frequency divider. The divider and the VCO are the two components which operate at the highest frequencies in the PLL synthesizer as mentioned before. The VCO loading becomes very important at very high frequencies. If the first stage of the divider is a long chain of flip-flops, it will present a heavy load to the VCO and a high frequency amplifier might as well be needed to drive the divider. This would result in an increased power consumption. Therefore the first stage must present a small capacitive load to the VCO. At the same time, another purpose of the first stage is to appropriately scale down the frequencies for the second stage. These factors play an important role in the design and optimization of the flip-flops for the first stage and at least for the first flip-flop of the second stage. The first stage, which is a synchronous Johnson counter, does not provide a high division ratio. Hence, for the reasons just mentioned, the ratios were chosen to be \( P/(P+1) = 3/4 \) for the first stage. Since an \( n \)-stage Johnson's counter is capable of dividing the input frequency by \( 2n \), two flip-flop stages are needed to achieve a division ratio of 4. As an example, for a divide-by-2/3 prescaler, two stages are needed or for a division ratio of 4/5, three flip-flop stages are required. Thus two stages can provide division ratios of either 2/3 or 3/4. Therefore the higher division ratio 3/4 can be chosen to maintain least number of stages while utilizing the maximum division ratio available from the two stage circuit.
Frequency Dividers, Overview and Design

A two stage Johnson's configuration is shown in Figure 3.5 in its basic form along with its state table, state diagram and implementation with D-flip-flops. The design can be modified using sequential logic design methods [28, 29]. One internal control input $MC_i$ for division ratio control, $P$ or $(P+1)$, will be added, which will control the division ratio of the first stage by properly directing the sequence of logic states.

Let the states of the first stage divider be represented by a binary number $Q_1Q_0$, where $Q_0$ is the LSB. By adding an input $MC_i$ and letting the counter to skip the state '11' and jump from '01' to '10', when $MC_i = '0'$, the effect will be that of counting three clock periods instead of usual four. When $MC_i = '1'$ the circuit is allowed to follow the regular sequence. The excitation table describing the D-flip-flop inputs is shown in Table 3.2, where the present states with the input $MC_i$ and the necessary next states are listed. Following the procedure given in Figure 3.6, the flip-flop outputs $Q_0(t+1)$ and $Q_1(t+1)$ can be expressed as sum of minterms and minimized by using Karnaugh maps. The flip-flop out-

---

**Figure 3.5: Johnson's Counter, its State Table and State Diagram**

**TABLE 3.1: State Table of a Johnson's Counter**

<table>
<thead>
<tr>
<th>Present State</th>
<th>Next State</th>
</tr>
</thead>
<tbody>
<tr>
<td>$Q_1$</td>
<td>$Q_0$</td>
</tr>
<tr>
<td>0 0</td>
<td>0</td>
</tr>
<tr>
<td>0 1</td>
<td>1</td>
</tr>
<tr>
<td>1 0</td>
<td>0</td>
</tr>
<tr>
<td>1 1</td>
<td>1</td>
</tr>
</tbody>
</table>
puts after minimization are given below in Equations 3.3, resulting in the first stage logic circuit shown in Figure 3.6.

\[ Q_0(t + 1) = Q_1((MC_I) + Q_0) \]
\[ Q_1(t + 1) = Q_0 \]

\[ DQ_0 = Q_1((MC_I) + Q_0') \]
\[ DQ_1 = Q_0 \]

<table>
<thead>
<tr>
<th>Present State</th>
<th>flip-flop inputs</th>
<th>( MC_I )</th>
<th>( Q_1 )</th>
<th>( Q_0 )</th>
<th>( DQ_1 )</th>
<th>( DQ_0 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>'0'</td>
<td>'0'</td>
<td>'0'</td>
<td>'0'</td>
<td>'0'</td>
<td>'1'</td>
<td></td>
</tr>
<tr>
<td>'0'</td>
<td>'0'</td>
<td>'1'</td>
<td>'1'</td>
<td>'0'</td>
<td></td>
<td></td>
</tr>
<tr>
<td>'0'</td>
<td>'1'</td>
<td>'0'</td>
<td>'0'</td>
<td>'0'</td>
<td></td>
<td></td>
</tr>
<tr>
<td>'0'</td>
<td>'1'</td>
<td>'1'</td>
<td>'X'</td>
<td>'X'</td>
<td></td>
<td></td>
</tr>
<tr>
<td>'1'</td>
<td>'0'</td>
<td>'0'</td>
<td>'0'</td>
<td>'1'</td>
<td></td>
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<tr>
<td>'1'</td>
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<td>'1'</td>
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<tr>
<td>'1'</td>
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<td>'0'</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>'1'</td>
<td>'1'</td>
<td>'1'</td>
<td>'0'</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 3.2: Excitation Table

Figure 3.6: First Stage Logic Design Procedure

3.3.2 Second Stage Design

In this section the first stage will be combined with the second stage, which is a ripple counter stage, to increase the overall division ratio to \( N/(N+1) = 31/32 \). The two
stages are connected through a combinational logic block which detects certain states from the second stage and controls the division ratio of the first stage depending on the logic value at the external modulus control input \( MC \).

As mentioned earlier, the second stage is a ripple counter stage which is capable of scaling down the input frequencies by a factor of \( 2^n \) with \( n \) flip-flop stages. Since the clock frequency input to the second stage is one fourth of the clock frequency input to the first stage, three flip-flops are required to obtain an overall division ratio of 32. Each of the flip-flops is a toggle flip-flop which is formed by feeding back the complementary output signal \( \bar{Q} \) to the \( D \)-input of the flip-flop. This is shown in Figure 3.7. The flip-flops used here are positive edge-triggered and such a ripple counter is a down-counter, \( i.e. \) it starts counting down from its maximum binary value to zero where the flip-flop for the LSB receives the clock [28]. To control the modulus of the divider, with the first stage combined with the second stage by the glue logic, it must be understood how the division works. The goal is to count 31 clock periods when \( MC \) is at low logic level and to count 32 clock periods when \( MC \) is high. It is known that the first stage can divide by 4 and the second stage by 8. As the second stage reaches towards the end of the cycle, it passes through the sequence of \('011', '010', '001', '000'\). Up until the state \('001'\), \(4 \times 7 = 28\) clock cycles would have been counted. During its last state \('000'\) the first stage will count four more clock periods. Thus by detecting the previous state \('001'\), and setting the \( MC_i \) input down to '0' at the end of this state but only when \( MC = '0' \), the first stage will be forced to count only three instead of four clock periods during the state \('000'\). Hence the total number of cycles counted will be 31 \( i.e. \ (4 \times 7 + 3) = 31 \). The logic circuit required from this condition, which corresponds to a unique logic state in the complete cycle, can be seen to be a \( NAND \) function.
since it is needed to apply a '0' when \( Q_4Q_3Q_2 = '001' \) to the input \( MC_i \) when \( MC' = '1' \).

As a note, it is mentioned here that each state in the second stage is unique and since it always cycles through all the states, one can also use any other state instead of '001' to remove one clock cycle. The control function \( MC_i \) to be applied to the first stage is then given by,

\[
MC_i = (MC' \cdot Q_4' \cdot Q_3' \cdot Q_2')
\]

Figure 3.7: An n-Stage Ripple Binary Counter

Hence, the two stages can be connected by a four input NAND gate. The complete logic circuit of the divide-by-31/32 dual-modulus frequency divider is shown in Figure 3.8. In order to verify the logic, the design based on positive edge-triggered flip-flops was drawn in Synopsys and selected simulation waveforms are shown in Figures 3.9 and 3.10.

In Figure 3.9 a complete cycle of division by 31 is shown in which the \( Q_0 \) signal is the output from the first stage and \( f_o \) is the divided output signal. At the time mark 1900 ns, it can be seen that three clock periods are counted instead of four when \( MC \) is low. In Figure 3.10 the \( MC \) signal is high and the division by 32 is obvious.

### 3.4 Summary

In this chapter various forms of frequency dividers were presented such as analog frequency dividers, parametric frequency dividers, digital frequency dividers etc. Then the
pulse swallowing technique was described which employs dual-modulus frequency dividers for fractional-N division frequency synthesis. In the end it was shown how a dual-modulus divider of an arbitrary ratio $N/N+1$ can be designed using sequential logic design methods and logic level simulations were also shown to verify the design. Using this design methodology, a dual-modulus frequency prescaler architecture can be analyzed. In the next chapter different types of D-flip-flops will be presented which can be used to implement the design. Particularly, the analysis and design of dynamic CMOS flip-flops will be presented.
Figure 3.9: Division by 31

Figure 3.10: Division by 32
4.1 Introduction

In the last chapter, the logic design of the divide-by-31/32 dual modulus frequency prescaler was described without taking into account any timing parameters. Practical circuits do however, have timing constraints, the simplest of which is the propagation delay of a signal through a circuit. Since the divider design is based on flip-flops, this chapter begins with a brief overview of commonly used clocking schemes for digital systems using flip-flops. Then various timing parameters of latches and flip-flops are described which determine the performance of digital systems. Some of the commonly used flip-flop structures are also mentioned and then functional analysis of dynamic flip-flops used in this particular design is illustrated. An optimization technique is also proposed and is used to illustrate the optimization of the prescaler circuit. The chapter concludes with the simulation results of the complete prescaler circuit.

The circuit simulations shown at various places in this chapter have been performed in HSPICE circuit simulator. The technology used for the circuits is Northern Telecom's 0.8μm gate-length BiCMOS technology from which only MOS devices have been used. Some of the circuits were simulated using minimum size devices permitted in
the BiCMOS technology and for which the circuit layouts were prepared using Cadence IC design tool Virtuoso. The HSPICE netlists were extracted for the circuits including parasitics for simulation.

4.2 Clocking Schemes

In almost all digital VLSI systems some of the states must be stored implying the use of storage or memory elements. In an FSM machine, the output of the system depends on the present state of the system as well as on the inputs. When the outputs change, the new states are sampled and stored in the flip-flops. During the time when the combinational logic is evaluating the output signals, the input signals and the present logic-states must remain stable. When the outputs have been evaluated and are stable, the flip-flops can be loaded with new logical values and stored as the present states. The task of data flow and synchronization is carried by the system clock which serves as the heart of the system. During part of each clock cycle, the storage elements are isolated and typically, are loaded with new data when the clock transition takes place. In a pipe-lined system, where there are no feed back paths, the flip-flops may be loaded at the end of each clock period. The maximum rate at which an FSM or a pipe-lined system can be clocked is determined by various timing parameters of both the memory elements and those of combinational logic.

The choice of the clocking strategy is of utmost importance since it would influence the circuit topology of the flip-flops to be used, the loading of the flip-flops and the routing of the clock signals throughout the chip. It also affects the size of the chip and its
power dissipation. The following paragraphs briefly describe the different types of clocking schemes which are available to the designer [22, 30, 31, 32, 33, 34, 35, 36].

### 4.2.1 Single Phase Clocking

Single phase clocking is the simplest form of clocking scheme in which only one clock signal is used to trigger the flip-flops and latches in the system. The flip-flops are typically composed of two latches operating on complementary clock signals. The second phase of the clock may be generated within each flip-flop itself and or it may be distributed globally in the chip. In the latter case the clock skew problems are more severe and must be dealt with by careful design. Because of the complementary clock signal, the scheme may not be regarded as single phase clocking scheme in its true sense.

### 4.2.2 Two Phase Clocking

In this scheme two non-overlapping clock signals are used. An example is shown in Figure 4.1. Ideally, the two signals never overlap and the logical condition ($\Phi_1$ AND $\Phi_2 = 0$) is always true. Due to clock skew, there might be some overlap. However, the use of two phase clocking reduces the skew and clock distribution problems as compared to single phase clocking.

### 4.2.3 Multi-Phase Clocking

Many VLSI systems use multiple non-overlapping clock signals so that multiple clock edges are available on which actions can be taken. However, it increases the complexity of the clock distribution networks. This method is mainly used by high performance systems.
4.2.4 True-Single-Phase Clocking or TSPC

In TSPC clocking technique, there is only one clock signal which is needed to trigger the flip-flops and no extra clock phase is required whatsoever. This technique is mainly used in dynamic CMOS circuits and helps to simplify the design.

![Two Phase Clocking Scheme](image)

**Figure 4.1: Two Phase Clocking Scheme**

4.3 Timing Constraints in a Sequential Logic Circuit

As mentioned before, the type of the flip-flops to be used in a digital circuit generally depends on the clocking scheme to be used. Several types of flip-flops have been reported in the literature and a wide variety of both single and double edge-triggered static as well as dynamic CMOS flip-flops are available. Before looking into different types of flip-flop circuits, it is useful to look at some important timing parameters for both latches and flip-flops so that a fair analysis can be made regarding their performance. To illustrate the timing parameters, a D-type latch and a D-type flip-flop will be used.
4.3.1 Latch Timing Parameters

A D-latch is a device, a memory element, with at least two inputs, a clock signal \( CLK \), a data signal \( D \), and at least one output \( Q \) where the other output may be the complement of \( Q \). The ideal latch behavior is shown in Figure 4.2. The D-latch is transparent during the high clock phase which means that the output \( Q \) follows the input during the time when the clock signal \( CLK \) is high. When the clock signal is low, the output is isolated from any changes in the input signal \( D \) as shown. This kind of latch is also called a positive latch. A negative latch can also be made with a complementary behavior [36].

\[ \begin{array}{c}
\text{CLK} \\
\downarrow \\
\text{D} \\
\downarrow \\
\text{Q}
\end{array} \]

\[ \begin{array}{c}
\text{CLK} \\
\downarrow \\
\text{D} \\
\downarrow \\
\text{Q}
\end{array} \]

**Figure 4.2: Positive D-Latch Behavior**

The latch parameters will be defined here with reference to the leading and trailing clock edges. The clock phase during which the latch is transparent will be called the *transparent phase* while the other phase will be called the *isolation phase*. The clock transition from the isolation phase to the transparent phase will be called the *triggering edge* while its counter part will be called the *isolating edge*. This terminology will make it easier to apply the timing parameters to both positive and negative latches although a positive latch will be used for illustration. To observe the timing constraints, the \( D \) signal for a latch is allowed to change during both the transparent as well as in the isolation phase anywhere but within the vicinity of clock transitions as restrained by the respective timing parameters.
ters, i.e. the setup and hold times. Furthermore, for both latches and flip-flops the timing

![D-Latch Timing Parameters](image)

**Figure 4.3: D-Latch Timing Parameters**

parameters can be different for high and low $D$ signal values and in such cases worst case
values are taken. The timing parameters are described below and are illustrated in Figure
4.3.

**Minimum Clock Pulse-Width, $T_w$:** It is the minimum clock pulse-width which is
necessary for a proper operation of the latch. Any further increase in the pulse-width of the
clock will not affect the other timing parameters such as setup time or hold time. This
definition also holds for an edge-triggered D-flip-flop.

**Setup Time, $\tau_S$:** It is the minimum time between a $D$ signal change and the isolating
(trailing edge for positive latch) edge of the clock such that the $Q$ output would assume the
correct $D$ value even under worst case conditions. Thus for a proper operation the $D$ signal
must be stable for a duration of time prior to the isolating edge of the clock given by $\tau_S$.
Nonobsevance of this condition is called the *setup time violation*. 

Design and Design Methodology of CMOS Gigahertz Frequency Range Prescalers
**Hold Time, $\tau_H$:** It is the minimum duration of time for which the $D$ signal must remain constant or stable after the isolating (trailing for positive latch) clock edge. The observance of this condition means that given that the most recent $D$ signal change was no later than the set-up time $\tau_S$ before the isolating edge, *i.e.* the set-up has been observed, the $Q$ output would assume the new value and remain stable after the isolating edge of the clock signal $CLK$. Failure to observe this condition is called *hold time violation*.

**Clock-to-Q Delay, $\tau_{CQ}$:** It is the propagation delay from the clock terminal $CLK$ to the output terminal $Q$ given that the $D$ signal has already been stable early enough relative to the triggering (leading) edge of the clock. In other words it is the time taken by the signal $D$ to appear at the output terminal $Q$ after the triggering edge of the clock.

**D-to-Q Delay, $\tau_{DQ}$:** It is the propagation delay from the $D$ terminal to the output $Q$ during the transparent phase of the clock given that the transparent phase is turned on early enough with respect to the $D$ signal change.

The affect of timing parameters on the behavior of a D-latch can be observed by comparing the ideal latch behavior in Figure 4.2 with the actual one in Figure 4.3. Even in Figure 4.3, the rise and fall times of the various signals are unaccounted for and these would further slow down the latch action.
4.3.2 Edge-Triggered D-Flip-Flop Timing Parameters

The edge-triggered flip-flop has the same input and output terminals as those of a D-latch however, an edge-triggered flip-flop responds to the changes in the $D$ signal only at one of the two clock edges, i.e. to the rising or the falling edge of the clock. Although the output is not affected by the second, inactive edge, changes do occur in the internal circuitry of the flip-flop. Similar timing parameters as those described for a D-latch may also be defined for the D-flip-flop. As illustrated in Figure 4.4, the flip-flop is shown to be a positive or leading Edge-Triggered D-type Flip-Flop or an ETDFF. Therefore, the parameters would be defined with respect to the leading edge of the clock [36]. The other edge of the clock, which was designated as the isolating edge for the latch, does not perform any function as far as the output $Q$ is concerned. The minimum clock pulse width for a D-flip-flop has the same significance as that for a D-latch. The other timing parameters for an ETDFF are described below.

**Set-up Time, $\tau_S$:** It is the minimum time between a $D$ signal change and the triggering (leading) edge of the clock such that the $Q$ output would assume the correct $D$ value even under worst case conditions. Therefore for a proper operation the $D$ signal must be stable.
Flip-Flops, Divider Circuit Design and Simulation Results

for a duration of time $\tau_S$ seconds, prior to the triggering edge of the clock. Nonobservance of this condition is called the *setup time violation*.

**Hold Time, $\tau_H$:** It is the minimum duration of time for which the $D$ signal must remain constant or stable after the triggering edge. The value of $\tau_H$ can be zero or even negative for some flip-flops. A Failure to observe this condition is called *hold time violation*.

**Clock-to-Q Delay, $\tau_{CQ}$:** It is the propagation delay from the clock terminal $CLK$ to the output terminal $Q$ given that the $D$ signal has already been stable relative to the triggering (leading) edge of the clock i.e. setup time has been observed.

### 4.3.3 Minimum Clock Period

Typically in an FSM, as shown in Figure 4.5, the flip-flops are in the feedback path of the system. It is also necessary to take into account the minimum and maximum delays associated with the combinational logic blocks. The maximum delay in a logic path $\tau_{L,\text{max}}$, also sometimes called the long path delay, determines the maximum speed of the system at which it can be clocked and in turn, is dependent on the number of logic gate stages in a particular signal path, the fan-in and fan-out of the gates and is also a function of the technology used. On the other hand, some of the logic signal paths might have small delays and $\tau_{L,\text{min}}$, or the short path delay, becomes critical in determining the proper functioning of the flip-flops in the sense that, due to short path delays, some of the $D$ signals might be generated so early in time such that hold time specification may be violated. These can also give rise to glitches and false signals. Therefore, it becomes feasible to
Figure 4.5: Finite State Machine Block Diagram

make the short path delays close to the larger delays in the systems by intentionally adding more delays [29, 36].

The minimum clock period, *i.e.* maximum clock frequency, at which a particular flip-flop can operate, may be estimated in terms of the above defined timing parameters. When defining the timing parameters, it was assumed that all the flip-flops in the system receive the clock pulse simultaneously. This implies that the clock pulse-width is the same throughout the system. However, in practice, even similar devices on the same wafer can have different parameters. Therefore, before doing any estimation, it is necessary to refine the estimation by incorporating other affects such as clock skew and clock edge deviation due to unmatched devices as well as the phase noise of the clock source. A parameter $\Delta t$

Figure 4.6: Clock Edge Deviation
will be defined to accommodate the worst case clock edge deviation. With reference to Figure 4.6, let the leading clock edge occur at time $t_l$. An interval of tolerance around $t_l$ can be introduced such that the clock edge is allowed to occur anywhere between $t_l - \Delta t$ and $t_l + \Delta t$. If the $D$ signal is assumed to arrive on time for the first clock cycle then the latest time of arrival of the $D$ signals for the next cycle must meet the following condition [36]:

$$t_{arr} \leq P - (\Delta t + \tau_s) \quad 4.1$$

where $P$ is the clock period. The $D$ signal would arrive at the $D$ terminal at the latest:

$$t_{arr} = \Delta t + \tau_{CQ} + \tau_{L,max} \quad 4.2$$

thus from the above two relations:

$$P \geq 2 \cdot \Delta t + \tau_{CQ} + \tau_s + \tau_{L,max} \quad 4.3$$

Also, to ensure proper functioning against any hold time violations, the $D$ signals must remain stable for $\Delta t + \tau_H$ after the triggering (leading) clock edge. In terms of short path delays, it is clear that the minimum time for the generation of new $D$ signals would be $\tau_{L,min}$, if $t_l = 0$. Thus the minimum delay through the logic must satisfy the following:

$$\tau_{L,min} \geq 2 \cdot \Delta t + \tau_H - \tau_{CQ,min} \quad 4.4$$

Any value less than the one given by the above relation, will cause a hold time violation. The above relations can now be used to compare different flip-flops in terms of speed performance and robustness against clock edge deviation from ideal. It should be noted that the tolerance interval $2\Delta t$ can be defined to take into account different types of clock edge deviations from an ideally placed clock edge in time, examples of which may be;
1. edge deviation when a given clock edge does not appear at all the flip-flops at the same time,

2. rise and fall times of the clock,

3. phase noise of the clock source.

Regarding the phase noise, the period of the clock may vary from cycle to cycle due to phase noise of the clock source. This gives rise to a changing clock pulse width and hence may be accounted for in the tolerance interval.

### 4.4 Speed Figure of Flip-Flops

An alternative method to measure the speed performance of a flip-flop is shown in Figure 4.7 [35]. It is basically a divide-by-2 counter formed by connecting the $Q$ output to an odd number of inverters and fed back to the $D$ input. The circuit is clocked and the clock frequency is progressively increased until the divide-by-2 operation fails. This corresponds to the maximum operating frequency of the circuit configuration in Figure 4.7.

![Speed Figure of Flip-Flops](image)

Figure 4.7: Speed Figure of D Flip-Flops

The speed figure of the flip-flop is then defined as the sum of setup time $\tau_s$ and the clock-to-$Q$ delay $\tau_{CD}$. In the case when the setup time is different for high and low $D$ inputs,
worst case value is taken. Since the inverter chain delay $\tau_{\text{inv}}$ is known, the following relations can be derived for a positive edge-triggered D-type flip-flop:

\[
\begin{align*}
\tau_d &= \tau_{\text{cd}} - \tau_{\text{inv}} \\
\tau_s &= T - \tau_{\text{cd}} \\
SF &= \tau_s + \tau_d = T - \tau_{\text{inv}}
\end{align*}
\]

Where $\tau_d$ is the delay through the flip-flop itself, $\tau_{\text{cd}}$ is the delay from the rising edge of the clock and time when the inverted output reaches back at the $D$ input. $T$ is the clock period and $SF$ is the speed figure, usually expressed in nanoseconds.

### 4.5 D-Flip-Flop Circuits

A wide variety of D-flip-flop circuits has been reported in the literature [14, 21, 22, 25, 37, 38]. As compared to the other types such as SR (set-reset) or JK type flip-flop, the D-flip-flop is the simplest in its form and operation. The behavior of the D-flip-flop has already been presented in section 4.3. In this section, a selection of static and dynamic CMOS D-flip-flops will be presented in order to first illustrate the multitude of choices available and secondly to select one or more circuit topologies to find a suitable circuit for the dual-modulus prescaler design. The main characteristics to be looked for are simplicity of design, low power consumption and high frequency operation with a wide operating frequency range.
4.5.1 Static Flip-Flops

The static flip-flops store or keep their logic states if the clock is stopped and power is maintained. A conventional static D-flip-flop can be made with logic gates, or in CMOS, with transmission gates and inverters. Typically the flip-flop circuits are composed of complementary latches connected in a master-slave configuration [28, 29]. A static latch with logic gates is shown in Figure 4.8 [32]. The form shown here uses a single clock but as can be seen, the device count is high, 14 for the logic-gate based latch and 8 for the transmission gate latch shown in Figure 4.9 [32]. The circuit complexity makes these unsuitable for the intended design for this work in terms of speed and power consumption.

![Static D-Latch Block with Logic Gates](image)

Figure 4.8: Static D-Latch Block with Logic Gates

A faster flip-flop circuit is shown in Figure 4.10 where two complementary latches are cascaded to form a static D-flip-flop. This circuit also uses a single clock but has reduced noise margin [24] and due to the regenerative transistor pair in each latch, it
requires careful design. It can be very fast because of small size and absence of feedback from the output to input.

![Diagram of a static D flip-flop with transmission gates and inverters]

**Figure 4.9:** A Static D Flip-Flop with Transmission Gates and Inverters

Another class of flip-flops worth mentioning here is the double edge-triggered flip-flop [22, 40, 41, 42]. Typically a flip-flop will trigger at either rising or falling edge of the clock signal. Therefore most of the time after settling it is inactive thus wasting time. By making a flip-flop trigger at both clock edges, the overall system efficiency and speed can be improved by a factor of two. An example of such a flip-flop is shown in Figure 4.11.

Digital systems which use double edge-triggered flip-flops require careful consideration of signal timing. For prescaler circuits these flip-flops do not offer any advantage since the

![Diagram of a fast static D-Flip-Flop]

**Figure 4.10:** A Fast Static D-Flip-Flop
overall division ratio is reduced to half of that offered by the corresponding circuit built with single edge-triggered flip-flops [22]. Another disadvantage is higher, typically double, device count. The conclusion being that double edge-triggered flip-flops do not give an overall speed improvement for the prescaler circuits.

![Diagram of a Double Edge-Triggered Flip-Flop](image)

**Figure 4.11: A Double Edge-Triggered Flip-Flop**

### 4.5.2 Dynamic Flip-Flops

Dynamic flip-flops are another class of storage elements which have become popular in the design of high speed digital systems in CMOS [22, 25, 26, 30, 31, 32]. These circuits store the logic state on the node capacitance which is mainly composed of gate capacitance of the MOS devices. When the clock is stopped and the power is maintained, the node capacitance starts to lose it’s charge due to leakage currents and thus the logic state may be lost after a certain duration of time and the charge must be refreshed regularly. Therefore clock signals for dynamic CMOS circuits consist of a precharge phase and an evaluation phase, at least refreshing the present state in each clock cycle if there is not going to be any change in the current state. Figure 4.12 shows two dynamic flip-flop structures. The flip-flop in Figure 4.12(a) with clocked inverters, uses a two phase clock to
function. It operates as follows. The clock signals $\Phi_1$ and $\Phi_2$ are out of phase clocks. When the clock $\Phi_1$ is high, the node $X$ takes the inverted value of $D$ signal while the output node $Q$ is in high impedance state and isolated from node $X$. When the clock $\Phi_1$ goes low, the node $X$ becomes isolated from the input $D$ and the output $Q$ takes the inverted value of $X$ (the true value of $D$), which is latched at the output. It should be noted that the voltages at the nodes are stored on the node capacitances composed of gate, drain and other parasitic capacitances.

Another dynamic latch structure shown in Figure 4.12(b) is based on what can be described as the true single phase clock or TSPC scheme [22, 31]. The circuits using TSPC scheme require only one clock signal and no other phase or complementary clock signal is needed. This scheme is quite popular in circuit design of high speed digital systems, especially for pipelined computational systems.

4.6 Circuit Design and Analysis

The dual modulus prescaler design described in this thesis is based on the TSPC dynamic D-type flip-flop circuit [22, 30, 31] shown in Figure 4.13. The structure itself is
quite simple and has only 9 MOS transistors, an additional inverter is required to obtain the true logic value of the latched $D$ input. This circuit forms the base of both the first and second stage of the circuit in Figure 3.8. Since the circuit is a dynamic structure, i.e. it stores or latches data on the node capacitances, it has a lower frequency limit as well as some charge sharing problems as will be evident in the following discussion of the circuit. These two problems can be overcome by careful design. The design goals can be stated as follows:

- to optimize the speed performance of the prescaler,
- to enhance the speed performance by avoiding conventional logic in the modulus control part of the first stage,
- to extend the operating frequency range of the prescaler using only dynamic circuits,
- to use simple circuits so that the power consumption can be kept low.

The objectives can be stated as follows. By careful design methodology and optimization, the dynamic circuits can be made to function at high frequencies as well as can be designed to operate in a wide frequency range. The reason behind the latter part of the last statement being that due to their inherent problems, dynamic circuits are generally known to work only in a narrow range of frequencies.

The logic design at the register level of the divide-by-31/32 dual-modulus frequency prescaler was described in section 3.3. The complete logic circuit is shown in Figure 3.8.
4.7 Consideration of Operating Frequency Range for Each Stage

As stated earlier, the dynamic flip-flops have a lower bound on the operating frequency to which they can operate without malfunctioning. When the divider architecture is considered, it can be seen that the lowest output frequency of the first stage is $f_{\text{clk, min}}/4$. Similarly, the lower bounds of the following flip-flops of the second stage are $f_{\text{clk, min}}/8$ at $Q_2$, $f_{\text{clk, min}}/16$ at $Q_3$, and $f_{\text{clk, min}}/32$ at the output $f_o$. Hence after the frequency has been divided by 4 by the first stage, each subsequent stage in the second stage reduces the frequency by another factor of 2. If this is not taken into account in the design of the dynamic flip-flops for the two stages, the circuit might fail to work.

The intended solution to take care of the above problem is to either optimize each occurrence of a flip-flop by taking into account the possible range of frequencies, or to modify the flip-flop circuit itself to make it work in a wider range of frequencies. Another approach is to use static flip-flops for the later stages. However, one of the objectives in this work is to use simple structures in order to minimize silicon area as well as to maintain low power consumption. Therefore, for all the flip-flops, dynamic circuits will be used.

In the following paragraphs, the transistor level design and speed optimization of the divider circuit will be presented.

4.8 Analysis of the First Stage Flip-Flop

The dynamic flip-flop used for the first stage design is shown in Figure 4.13. The operation of the flip-flop can be understood by considering eight cases which constitute
different combinations of input signals namely the clock and the data. For the illustration purposes, minimum transistor sizes are used in the flip-flop circuit. In the cases considered, the first four are related to changes in the clock signal with a steady data signal and the last four are related to the changes in the data signal when the clock signal is steady.

![Flip-Flop Diagram](image)

**Figure 4.13: Dynamic Flip-Flop for the First Stage**

**CASE 1: D = '0', Clock goes from low to high (CLK '0' → '1').**

Assuming that $Q_b$ is initially low, the transistors $M_1$ and $M_2$ are on while $M_3$ is off in this condition. Therefore the node $N_2$ is high keeping $M_5$ on. With clock being low $M_4$ is on thus $N_3$ is also high. This condition keeps $M_7$ and $M_8$ off while $M_9$ stays on. However, $Q_b$ is isolated from $N_3$ since $M_7$ and $M_8$ are off. Thus the voltage at the node $Q_b$ remains latched. When the clock signal goes high, $M_2$ turns off, isolating $N_2$ from input $D$ and keeping it high. Now the transistor $M_4$ turns off, $M_6$ turns on while $M_5$ is already on. This discharges the node $N_3$ turning $M_7$ on, $M_9$ off whereas $M_8$ is turned on. Since $M_7$ is turned on with the node $Q_b$ disconnected from ground, the node $Q_b$ goes high. The circuit
Thus acts as a positive edge-triggered D flip-flop latching the complement of $D$ at $Q_b$ when the clock goes from low to high. The true value of the latched signal is provided by the output inverter. The simulation of this case is shown in Figure 4.14.

Figure 4.14: Case 1

CASE 2: $D = '0'$, Clock goes from high to low (CLK ‘1’ → ‘0’).

When $D$ is low and clock is high, the following conditions prevail. Transistor $M_1$ is on but $M_2$ and $M_3$ are off. Hence $N_2$ is isolated from the input. The clocked transistors $M_6$ and $M_8$ are on and $M_4$ is off. The voltage on node $N_3$ now depends on voltage on $N_2$. If $N_2$ was low, $M_5$ would be off. Hence $N_3$ is also isolated. This condition is shown in Figure 4.15 as Case 2a before the falling edge of the clock. However if $N_2$ was high initially, $N_3$ would be low thus making $Q_b$ high by turning $M_7$ on and $M_9$ off. This latter condition is shown in Figure 4.16 as Case 2b.
When the clock goes from high to low, the node $N_2$ is charged to the supply voltage through $M_1$ and $M_2$. The node $N_3$ goes high since $M_6$ will be cut off and $M_4$ will be turned on. The voltage at $N_3$ will isolate $Q_b$ from $N_3$ because $M_7$ will be turned off, with $M_9$ on but $M_8$ going off as clock goes low. Thus in this case the $D$ signal is sampled and stored at the node $N_2$ when clock goes from high to low. The HSPICE simulation of this case with the two possibilities is shown in Figures 4.15 and 4.16.

**CASE 3: $D = '1'$, Clock goes from high to low (CLK ‘1’ $\rightarrow$ ‘0’).**

When $D$ and clock are both high, the node $N_2$ is low since $M_3$ is on with $M_1$ & $M_2$ both cut off. In the second branch, $M_4$ and $M_5$ are off while $M_6$ is on thus isolating the node $N_3$. The transistor $M_8$ is on but the present voltage on $Q_b$ will depend on the voltage on $N_3$. If $N_3$ was high $Q_b$ would be high since $M_9$ would be on (Case 3a, Figure 4.17). On
the other hand, a low at the node $N_3$ will charge $Q_b$ to supply voltage. This can be seen as Case 3b in Figure 4.18.
As the clock signal goes low, following events take place. The node $N_2$ which was low, still stays low but may rise a little as $M_2$ turns on and the charge on $N_I$ is being dumped to ground. Thus $M_5$ stays off but $M_4$ now charges the node $N_3$ towards supply voltage turning $M_7$ and $M_9$ off, while the clock signal turns $M_8$ off. The results is that the node $Q_b$ is now isolated from $N_3$. The simulation of these conditions is shown in Figures 4.17 and 4.18.

Figure 4.18: Case 3b

CASE 4: $D = '1'$, Clock goes from low to high ($CLK \ '0' \rightarrow \ '1'$).

When $D$ is high the node $N_I$ and $N_2$ are already low since the transistor $M_1$ is off while $M_2$ and $M_3$ are both on. The node $N_3$ is high since $M_4$ is on and both $M_4$ and $M_5$ are off, hence isolating $Q_b$ from $N_3$. When the clock goes high, $M_2$ is turned off which now brings $N_2$ into tristate condition and becomes isolated from any input changes. Since the clock is rising, turning $M_4$ off, the node $N_3$ is also isolated from $N_2$ as $M_5$ is already off.
because \( N_2 \) is low. As \( N_3 \) was initially high, the high going clock turns \( M_8 \) on. With \( M_9 \) already on the output \( Q_b \) goes low.

![Graph]

**Figure 4.19: Case 4**

Thus in this case the output is latched at the rising edge of the clock. The HSPICE simulation of this condition is shown in Figure 4.19.

The next four cases will describe the flip-flop behavior when the clock signal is steady but changes occur at the input signal \( D \).

**CASE 5: CLK = '0', D goes from low to high (D '0' \( \rightarrow \) '1').**

When both the clock signal and the \( D \) signal are low, the node \( N_2 \) is high because the transistors \( M_1, M_2 \) are on and \( M_3 \) is off. The node \( N_3 \) is also high because \( M_6 \) is off while \( M_4 \) and \( M_5 \) are on. However \( Q_b \) is isolated from \( N_3 \) as both \( M_7 \) and \( M_8 \) are off. When \( D \) rises, the nodes \( N_1 \) and \( N_2 \) are driven low cutting \( M_5 \) off and further isolating \( N_3 \). Thus a \( D \) signal change from low to high with a low clock signal does not affect the output and...
the change is transferred only to the node $N_2$. The HSPICE simulation of these events is depicted in Figure 4.20.

![Graph showing CLK, D, Qb, and N2]  

Figure 4.20: Case 5

**CASE 6:** Case 6: CLK = '0', D goes from high to low (D '1' $\rightarrow$ '0').

In this case the node $N_2$ is initially low because $M_1$ is off while $M_2$ and $M_3$ are on. The node $N_3$ is isolated. When $D$ goes low, $M_1$ turns on but $M_3$ turns off which cause $N_2$ to go high turning $M_5$ on but, since $M_4$ is on with $M_6$ off, $N_3$ is hardly affected. This can be seen in Figure 4.21 where a simulation of this case is shown.

**CASE 7:** CLK = '1', D goes from low to high (D '0' $\rightarrow$ '1').

In this case the node $N_2$ is initially isolated from the input as both $M_2$ and $M_3$ are off. The node $N_1$ is precharged to the supply voltage. The voltage at node $N_3$ depends on the initial voltage on node $N_2$. If $N_2$ was high, $N_3$ would be low since both the transistors $M_5$ and $M_6$ are on while $M_4$ is off. This isolates $Q_b$ from the rest of the circuit. On the
other hand if node $N_2$ was low, $N_3$ is isolated and the voltage on $Q_b$ will depend on the voltage on $N_3$. The first condition is shown in Figure 4.22 as Case 7a while the second condition when $Q_b$ depends on $N_3$, is illustrated in Figure 4.23. The node voltages are unpredictable as these may be partially charged and give rise to a metastable condition. However, any subsequent rising clock edge will cause $Q_b$ to go low as shown by the simulation.

![Figure 4.21: Case 6](image)

CASE 8: CLK = '1', D goes from high to low (D '1' → '0').

When both the $D$ signal and the clock signal are high, the node $N_2$ is discharged to ground. This makes $M_5$ to be in cut off, thus isolating the node $N_3$ as can be seen in the simulation shown in Figure 4.23 for the previous case. Again, in this case also the voltage on the node $Q_b$ will depend on the initial voltage on the node $N_3$. If it is high $Q_b$ will be obviously low but if $N_3$ is low then $Q_b$ will be high. When the $D$ signal goes low, the node
Figure 4.22: Case 7a

$N_2$ becomes isolated too and thus further isolates the circuit from the input changes. A simulation of this case is shown in Figure 4.24.

4.8.1 Timing Parameters

The first stage flip-flop circuit in the previous section consisted of minimum sized MOS transistors for the mentioned BiCMOS technology. The basic circuit was simulated using HSPICE prior to any speed optimization. Several timing parameters obtained from simulation of this circuit are listed in Table 4.1. Later on, the same parameters for the optimized circuit will be given. It can be seen from Table 4.1 that the circuit for first stage has an operating window from approximately 127 MHz to 1110 MHz for a divide-by-2 configuration before having functional problems, while this window reduces to 127 MHz -890 MHz for a two stage divide-by-4 Johnson configuration. This configuration was selected
Figure 4.23: Case 7b

Figure 4.24: Case 8
to compare it with the optimized first stage which has a divide-by-3/4 configuration shown in Figure 3.6.

### 4.9 Analysis of the Second Stage Flip-Flop

The second stage of the dual-modulus prescaler is an asynchronous chain of three flip-flops or a divide-by-8 configuration. If the circuit in the previous section is taken as an example, the output frequency of the first stage lies between 65 MHz to 220 MHz. Obviously the same flip-flop circuit cannot be used for the second stage because it will not function in this range. The circuit has to be modified so that it works within the required frequency range. The modified version is capable of working from low frequencies to higher ones as will be seen in the following paragraphs. The circuit used in the second stage is shown in Figure 4.25. To illustrate the problem which the first stage flip-flop has working at lower frequencies, a simulation of the divide-by-4 configuration at 180 MHz is shown. It can be observed that this circuit cannot work at this or lower frequencies. The circuit is dividing by 3 instead of 4 and also, there are the metastability problems as it is

<table>
<thead>
<tr>
<th>Parameter</th>
<th>For</th>
<th>Value</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\tau_{CQ}$</td>
<td>0</td>
<td>0.557 ns</td>
<td>Clock-to-Q delay</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>0.317 ns</td>
<td></td>
</tr>
<tr>
<td>$\tau_S$</td>
<td>0</td>
<td>0.188 ns</td>
<td>Set-up time</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>-0.113 ns</td>
<td></td>
</tr>
<tr>
<td>$\tau_H$</td>
<td>0</td>
<td>0.162 ns</td>
<td>Hold time</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>-0.103 ns</td>
<td></td>
</tr>
<tr>
<td>Speed Figure</td>
<td></td>
<td>0.673 ns</td>
<td>Worst case</td>
</tr>
<tr>
<td>$f_{min}$</td>
<td></td>
<td>127 MHz</td>
<td>Divide-by-2 configuration, with sinusoidal clock signal.</td>
</tr>
<tr>
<td>$f_{max}$</td>
<td></td>
<td>1110 MHz</td>
<td></td>
</tr>
<tr>
<td>$P_{ave}$</td>
<td>$f_{max}$</td>
<td>1.35 mW</td>
<td>Average Power @ 5V</td>
</tr>
<tr>
<td></td>
<td>900MHz</td>
<td>1.13 mW</td>
<td>Divide-by-2 configuration</td>
</tr>
</tbody>
</table>
clear from Figure 4.26.

At low frequencies there is an inherent problem in the dynamic flip-flop [22, 25, 26]. When a low data signal \( D \) is being sampled, the node \( N_2 \) is high keeping the transistor \( M_5 \) on. The node \( N_3 \) is then an inverted version of the clock signal and when the clock goes low, the node \( N_3 \) becomes high thus turning \( M_9 \) on. In this state when the next rising clock edge comes, it turns \( M_9 \) on before affecting the node \( N_3 \) so that when it goes low, \( M_9 \) turns off late. The result is that the node \( Q_b \) momentarily discharges because of the delay which exists between \( M_8 \) turning on and \( M_9 \) turning off. The glitch is significant at low frequencies and can affect the circuits which are connected at the output. This situation is shown in Figures 4.26 and 4.27. In order to remove the glitch, another transistor, \( M_{8a} \), can be added as shown in the Figure 4.25, that is driven by an inverter which in turn, is being driven from the node \( N_2 \). When the node \( N_2 \) is high, the inverter switches the transistor \( M_{8a} \) off so that the node \( Q_b \) cannot discharge thus preventing the glitch. Furthermore, at lower frequencies the output node can discharge due to leakage currents and to

![Figure 4.25: Second Stage Flip-Flop](image-url)
check that, a small feedback P device can be added which is driven from the output node $Q$ and when the output is low, this transistor helps to keep the node $Q_{lb}$ high.

The modifications described above are shown in Figure 4.25 and HSPICE simulation in the Figure 4.28 show that the problems are eliminated. The basic operation of the flip-flop is the same as that of the first stage flip-flop.

4.9.1 Timing Parameters

The same set of timing parameters as those for the first stage flip-flop can be determined for the flip-flop used in the second stage. This set of extracted timing parameters is given in Table 4.2.

4.10 Modulus Control Circuit

The first stage of the dual-modulus divider has a divide-by-3/4 synchronous con-
Figure 4.27: Glitch in the Dynamic Flip-Flop at Low Frequencies

Figure 4.28: Operation of the Modified Dynamic Flip-Flop
figuration. The division ratio is controlled by the modulus control circuit which is inserted between the two first stage flip-flops. If the signal $MC_i$ in Figure 3.6 is high then the OR gate is closed and the circuit performs division by four which is the normal operation. However, if this signal $MC_i$ is low, then the circuit skips one clock cycle out of every four cycles and a division by three results. Ordinarily the control can be implemented using logic gates as shown in Figure 3.6 or the function can be implemented into the flip-flops themselves [22]. Both of these schemes suffer from the drawback that they reduce the operating speed of the circuit. In this design, a different scheme is used to change the modulus of the divider at the proper instant. The circuit which achieves this is shown in Figure 4.29 and is connected in parallel to the path of the output signals of the two flip-flops of the first stage. The operation, with reference to the state diagram in Figure 4.29, is as follows. Normally the circuit goes through the states following the sequence ‘00’, ‘01’, ‘11’ and ‘10’. In order to skip one input clock cycle out of every four, a control signal $MC_i$ is introduced which when low, forces the circuit to skip the state ‘11’ and it goes from state ‘10’ to state ‘10’. This happens as follows. If the signal $MC_i$ is low, transistor $M_c$ pulls the

<table>
<thead>
<tr>
<th>TABLE 4.2: Simulated Timing Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parameter</td>
</tr>
<tr>
<td>---------------</td>
</tr>
<tr>
<td>$\tau_{eq}$</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>$\tau_s$</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>$\tau_h$</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>Speed Figure</td>
</tr>
<tr>
<td>$f_{min}$</td>
</tr>
<tr>
<td>$f_{max}$</td>
</tr>
<tr>
<td>$P_{ave}$</td>
</tr>
<tr>
<td></td>
</tr>
</tbody>
</table>
node $S$ to a voltage less than the $V_t$ of the NMOS transistor to keep $M_e$ off. When $MC_i$ is low, transistor $M_c$ does not affect the node $S$ whereas the signals $Q_{0b}$ and $Q_{1b}$ do. The transistors $M_a$, $M_c$ and $M_e$ along with the inverter $I_2$ perform the logic function given by Boolean equation 3.3. Therefore when the circuit is in state '01' and $MC_i$ is low, $Q_{0b}$ is also low keeping $M_a$ off. Since $Q_l$ is low too, node $S$ does not affect $M_e$. When the next rising clock edge arrives, the circuit momentarily goes into state '11' which is the next state in the normal divide-by-4 operation. Since $M_c$ is off, the signals can affect the node $S$. Signal $Q_l$ goes high and turns on the transistor $M_e$ on. Although $Q_{0b}$ is low which means that $Q_o$ should be high, a high $Q_l$ forces the transistor $M_e$ to pull down the node $Q_o$ immediately. Therefore the circuit is forced to go into the state '10' before the next clock cycle. The next clock edge causes the circuit to go into the initial state '00'. This cycle is repeated as long as $MC_i$ is kept low. The operation of this circuit depends on careful sizing of the transistors $M_a$, $M_c$ and $M_e$.

The above action which performs division by 3 can be seen in Figure 4.32 where at approximately 46.7ns, $Q_0$ and $Q_l$ are both high and $S$ is rising, forcing $Q_o$ to go low. $Q_o$ must be pulled down below the threshold voltage before the next rising clock edge. The circuit fails to divide by 3 when this cannot be done anymore when the input clock frequency is increased.

The rest of the control logic, the NAND gate, for the complete divider is not that critical because after the first stage the frequency is already reduced by a factor of at least three. Therefore a NAND gate from the standard cell library of the technology can be used.
to generate the $MC_i$ control signal for the first stage ratio by detecting logic states from the second stage output bits.

![Diagram](image)

Figure 4.29: Modulus Control Circuit for First Stage

### 4.11 Circuit Optimization

The prescaler circuit uses CMOS flip-flops which are composed of several transistors. The operating frequency of the circuit can be increased by optimizing the sizes of the transistors. The optimization process is not a straightforward process because changing the transistor sizes connected to a particular node influences the switching speed of both the driven and the driving node. Further, the feedbacks signals in a sequential circuit are also effected. In CMOS circuits, tapered transistors connected in series in a branch [43] help to reduce the gate capacitance of the innermost transistors however, this does not
guaranty the required performance e.g. maximum operating frequency. The optimization can either be carried out in a manual, iterative simulation process or stochastic methods of optimization can be utilized. Such approaches may not provide an insight into the circuit behavior. Here, an optimization method for transistor sizing is proposed which employs the idea behind the event-driven simulation algorithms. In an event-driven simulation of a system, the simulation time is not advanced until an event happens to which the state of the system is subject to change. Based on the changes, activities are carried out, new events are scheduled and the simulation time is advanced. This is in contrast to the usual methods of simulation in which simulation time is advanced in fixed increments and for each time step, small or large, the required calculations are performed.

The method used to optimize the MOS device sizes for the prescaler circuit exploits the above concept by applying it to time domain simulations of the flip-flop circuits. This can be illustrated as follows. In the circuit of Figure 4.13, there are seven nodes including the nodes $Q_b$ and $Q$. These nodes are influenced by the signals on $D$ and $CLK$ terminals. When a change in these signals happens i.e. an event occurs, it causes different node voltages to change and these are updated accordingly. The circuit conditions after the event continue to settle down and after some time the circuit is said to be in its relaxed state, ready to take a new event. In the presence of feedback paths e.g. if $Q_b$ is connected back to $D$ forming a toggle flip-flop, the circuit will not relax until the feedback signal reaches back at $D$.

A circuit can be optimized by first breaking it into smaller circuits e.g. one flip-flop only, and then putting it into certain initial conditions to simulate different possibilities of events at its inputs. The cause and effect relationship between the event and the variable to
Flip-Flops, Divider Circuit Design and Simulation Results

be optimized, can be studied and changes in the circuit can then be made accordingly. For example, in Figure 4.13, \( N_1, N_2 \) are the nodes connecting the left and middle branch. In order to observe the impact of the transistor size of \( M_I \) on node \( N_I \), an event is caused to simulate a particular condition, which can be one of the cases discussed in section 4.8. In the simulation, the size of \( M_I \) is varied in steps and for each step, a simulation is performed involving a time duration starting from the start of the event and ending when the circuit is relaxed. Various node voltages and device currents are then plotted together which show the said relationship graphically. A suitable size for the device \( M_I \) is selected and that size is assigned to the transistor. The same event is simulated again but this time the size of \( M_2 \) is varied to observe its influence on the nodes. The remaining nodes \( N_2, N_3 \) etc. are processed in a similar manner until the last node is reached. The process can be repeated until the desired criteria, e.g. a certain propagation delay, is met. This is then the stopping point of the optimization process.

As stated earlier, the goal was to optimize the prescaler circuit to achieve maximum operating frequency. Since speed and power optimization may not be achieved at the same time, power dissipation was kept low by choosing CMOS dynamic circuits using true single phase clocking scheme (TSPC).

An example of the procedure outlined above is shown in Figure 4.30 which represents the Case 1 in section 4.8. Here the device under consideration is the transistor \( M_3 \). The width of the transistor is being varied from 1.4\( \mu \)m to 13\( \mu \)m. The node voltages at \( Q_b \) and \( N_2 \) are plotted for the corresponding sizes which vary as shown on the graph. According to Case 1, when the clock signal rises with a low \( D \) signal, the node \( Q_b \) rises and node...
N₂ stays high. As shown in Figure 4.30, a falling clock signal precharges node N₂ when D is low. When the rising edge clock event occurs, the inverted D signal is transferred to node Q₂. Varying the size of transistor M₃ shows that the delay from node D to N₂ can be reduced by approximately 0.13ns if M₃ is kept small. This is because a small transistor size reduces the node capacitance. This can be seen in the graph of Figure 4.30(a), where a falling D signal causes the node N₂ to charge. For different transistor sizes this node charges at a different rate. The graph in Figure 4.30(b) shows the drain current of M₃. These curves show a considerable change in peak current when the sizes are varied from 1.4μm to 13μm. Considering the reduction of the charging time of N₂ and to keep a small current, a small transistor size is chosen for M₃. The consideration of the delay from rising clock edge to the corresponding change at node N₂ is not considered here as transistors at node N₃ still need to be optimized.

All the flip-flop circuits in the preceding sections were optimized for maximum speed. As a start the first stage with a divide-by-4 configuration was simulated and then the control logic was inserted. Then the second stage flip-flop was optimized to achieve speed compatibility with the first stage. The optimization of the second stage is easier than that for the first stage since only one flip-flop has to be optimized. This is because flip-flops of the second stage can operate at lower frequencies. The next step was to carefully layout the circuit, extract post layout netlists and perform further optimization by iterative time domain analysis.

The flip-flop circuits for both divider stages were layed out and the netlists were extracted that included parasitics. Two instances of the first stage flip-flop and one
instance of the second stage flip-flop was optimized. The simulated timing parameters were extracted with HSPICE and are given in Table 4.3. FF1 and FF2 are the two versions of the first stage flip-flop. TFF is the designation used for the second stage flip-flop since this flip-flop is connected in the toggle configuration. The timing parameter values listed in Table 4.3 indicate an increase in the operating speed of the first stage flip-flops almost by a factor of 1.7 as compared to the non-optimized circuits. The second stage flip-flop has been kept slow keeping two objectives in mind. The first one was to ensure proper function at relatively low frequencies and the second objective was to ensure correct voltage swings of the internal nodes of the flip-flop but with improved timing parameters i.e.
smaller delays and time constraints. The complete prescaler circuit with optimized transistor sizes is given in Appendix B.

Final data for the optimized circuit is given in Table 4.4. Although the TFF is working at low frequencies, it is taking slightly more power which is due to a higher device count as compared to the first stage circuits.

**TABLE 4.3: Timing Parameters of Optimized Flip-Flops**

<table>
<thead>
<tr>
<th>FF</th>
<th>( \tau_{CQ} ) ns</th>
<th>( \tau_{D} ) ns</th>
<th>( \tau_{ID} ) ns</th>
<th>SF</th>
<th>( f_{min} ) MHz</th>
<th>( f_{max} ) MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>FF1</td>
<td>0.2</td>
<td>0.43</td>
<td>0.19</td>
<td>-0.03</td>
<td>0.1</td>
<td>0.17</td>
</tr>
<tr>
<td>FF2</td>
<td>0.46</td>
<td>0.28</td>
<td>0.17</td>
<td>0.22</td>
<td>0.14</td>
<td>-0.13</td>
</tr>
<tr>
<td>TFF</td>
<td>0.49</td>
<td>0.42</td>
<td>0.45</td>
<td>0</td>
<td>0.075</td>
<td>-0.36</td>
</tr>
</tbody>
</table>

### 4.12 Simulation Results

In this section the simulation results of the whole divider will be presented. After optimization the circuits were layed out and a number of post layout simulations were performed. Selected results are presented in the Figure 4.31 to Figure 4.35. These are explained in the following paragraphs.

**TABLE 4.4: Power Figures for Flip-Flops**

<table>
<thead>
<tr>
<th>FF</th>
<th>@ 900 MHz</th>
<th>( @ f_{max} ) MHz</th>
<th>( \mu \text{W/MHz} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>FF1</td>
<td>3.5 mW</td>
<td>5.92 @1756 MHz</td>
<td>2.83</td>
</tr>
<tr>
<td>FF2</td>
<td>3.59 mW</td>
<td>5.49 @1505 MHz</td>
<td>3.14</td>
</tr>
<tr>
<td>TFF</td>
<td>2.8 mW @ 400 MHz</td>
<td>5.5 @910 MHz</td>
<td>5.29</td>
</tr>
</tbody>
</table>

**First Stage: Division by 4**

In Figure 4.31 a simulation of the first stage circuit is shown which has a divide-by-3/4 configuration. The input frequency is 1070 MHz. The modulus control input is kept high and the circuit is dividing the input clock frequency by 4. In the same Figure, the
operation of the modulus control circuit is also illustrated. Since the control signal is high, the node $S$ is kept low so that the transistor $M_e$ does not turn on and the circuit goes through its normal cycle.

**First Stage: Division by 3**

A simulation of the first stage circuit with the modulus control signal set low is shown in Figure 4.32 where the output signal frequency is one third of the clock frequency and the input clock frequency is 1060 MHz. As can be seen in the Figure 4.32, each cycle of $Q_0$ or $Q_1$ contains three cycles of the $CLK$ signal. The Figure also shows the modulus control circuit operation. The control signal is set low and when both $Q_{0b}$ and $Q_{1b}$ go low at the same time, *i.e.* the state is '11', the node $S$ goes high turning the transistor $M_e$ on and thus pulling down the node $Q_0$. This has the effect of bringing the circuit in state '10' when it would have stayed in the state '11'. This happens before the next clock edge. Thus when the next edge of the clock signal arrives, the circuit goes into the initial state '00' and hence can count only three clock periods. Selected performance measures for the first stage circuit are given in Table 4.5.

**Divide by 32 Operation**

The simulation of the complete divider circuit divide-by-32 mode is shown in Figure 4.33 where the input frequency is 1050 MHz. The control signal $MC$ is high (at 5 Volts) which keeps the node $S$ low. This can be seen in the bottom most trace in Figure 4.33. The first stage is performing division by 4 and the second stage by 8 thus giving an overall division ratio of 32.
Divide by 31 Operation

In this case the modulus control signal $MC$ is set low keeping the transistor $M_c$ out of the picture as long as $MC$ is low. The voltage at node $S$ is now a function of $Q_0$ and $Q_I$, which keep it low until the time when the circuit is in the required logic state and at that time, all the NAND gate inputs go low and it gives out a high going pulse which drives the node $S$ high. This pulse turns on the transistor $M_e$ and pulls down the node $Q_I$. The result is that one clock cycle out of each 32 cycles is skipped \textit{i.e.} achieving division by 31. The operation is illustrated in Figure 4.34. The input frequency is 1050 MHz.

<table>
<thead>
<tr>
<th>Div. Ratio</th>
<th>$f_{min}$, MHz</th>
<th>$f_{max}$, MHz</th>
<th>$P_{ave} @ f_{max}$, mW</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>147</td>
<td>1062</td>
<td>8.91</td>
</tr>
<tr>
<td>4</td>
<td>158</td>
<td>1070</td>
<td>8.66</td>
</tr>
<tr>
<td>31</td>
<td>159</td>
<td>1060</td>
<td>13.47</td>
</tr>
<tr>
<td>32</td>
<td>158</td>
<td>1079</td>
<td>13.72</td>
</tr>
</tbody>
</table>

Divide by 31.5 Operation

Figure 4.35 shows an example of fractional division with a ratio of 31.5 and input frequency of 1050 MHz. Each output cycle of 31 input cycles is followed by an output cycle that consists of 32 input cycles, effectively dividing the input clock signal by 31.5. Two output cycles are shown in the Figure and total of 63 clock cycles can be counted for the two output cycles. In this case the output of the prescaler is fed to a toggle flip-flop and the output of this flip-flop goes to the modulus control input of the prescaler. Thus, for one output cycle, the $MC$ signal is set low which makes the prescaler to divide by 31 and for the next output cycle, the modulus control input is set high for a division ratio of 32.
4.13 Summary

This chapter presented simulation results for the optimized, complete frequency prescaler circuit. The dynamic flip-flop circuit for the first stage was optimized for maximum speed and the one for the second stage was optimized for speed in the sense that it could work at high as well as low frequencies. Different timing parameters defined earlier in the chapter, were given for the optimized flip-flops and simulation results of the complete prescaler circuit were presented with one example of fractional division of the input clock frequency.
Figure 4.31: Division by 4, input frequency: 1070 MHz
Figure 4.32: Division by 3, input frequency: 1060 MHz
Figure 4.33: Division by 32, input frequency: 1050 MHz
Figure 4.34: Division by 31, input frequency: 1060 MHz
5.1 Introduction

The dual-modulus frequency prescaler design was fabricated in two different MOS technologies. The first prescaler with division ratios of 31/32 was fabricated in Northern Telecom's 0.8µm gate-length BiCMOS technology through Canadian Microelectronic Consortium (CMC), and was packaged in a 68 pin PGA with I.D.# IBACUKS1. The second design consisting of only the first stage having division ratios of 3/4 was submitted to Motorola, for fabrication in Motorola's GCMOS process. This design was not packaged, testing was done by bonding the die on an RF board. Several tests were carried out to evaluate the performance of the dual-modulus frequency prescalers. These include:

- operating frequency range,

- maximum operating frequency as a function of supply voltage,

- power consumption as a function of frequency,

- input sensitivity of the divider which is the minimum amplitude of the clock signal necessary for proper operation as a function of frequency.
This chapter explains the test set-ups, procedures and measurement results performed on the prescaler circuits. Since the circuits were expected to operate in the range of 1 GHz or above, special care was given to the test beds to reduce unnecessary signal losses and noise coupling.

5.2 0.8μm gate-length BiCMOS Dual-Modulus Frequency Divider

This section describes the measurement results performed on the prescaler chip IBACUKS1 fabricated in 0.8μm BiCMOS technology.

5.2.1 Floor Plan

The partial floor plan of the chip IBACUKS1 is shown in Figure 5.1. In order to measure power characteristics of the divider, separate power supply pads were provided for the divider circuit and for the output buffer. The output buffer is composed of a six stage tapered CMOS inverter chain followed by an emitter follower stage with an open emitter. The BJT is included in the buffer to take the advantage of its higher drive capability as compared to MOS transistors since most RF measurement equipment are 50Ω systems.

There is no ESD protection circuits on any of the pads, therefore extreme care was necessary during the testing. Grounded wrist bands were also used during the testing.

5.2.2 Test Bed

The test bed of IBACUKS1 was built on a breadboard with a ground plane because of the presence of very high frequency signals. The schematic of the test circuit is shown
in Figure 5.2. To built the circuit, surface mount components were used wherever possible and were placed as close to the chip as possible with shortest connections. Separate regulated power supplies were used for all dc requirements which were,

- $V_{MC}$, the modulus control input,
- $V_b$, dc bias for the clock signal,
- $V_{dd}$, dc supply for the divider circuit,
- $V_{bb}$, dc supply for the output buffer.

![Diagram](image)

**Figure 5.1: Partial Floor Plan of IBACUKS1**

As shown in Figure 5.2, the mc_div2 input pin has one resistor connected permanently to ground for ESD protection and a jumper switch is provided to apply 5 Volts to the input through another resistor. These resistors were provided to limit any charging and discharging current through this pin which has one MOS transistor gate as input.
The power supplies for both the divider circuit and the output buffer were decoupled with capacitors to reduce switching noise in the setup. The clock input was provided with a signal generator capable of providing a maximum signal power of +20dBm over 50Ω up to 4 GHz. Two 50Ω resistors connected as a voltage divider at the clock input provide a dc bias of $V_b/2$ so that the peak-to-peak ac-coupled signal from the generator goes

**Figure 5.2: Test Set-Up for IBACUKS1**

![Diagram of the test setup for IBACUKS1](image)
from 0 Volts to $V_b$. A high frequency inductance was inserted in series with the 50Ω resistor from $V_b$ to the clock input pin to provide high impedance path to the supply for the clock signal. The 50Ω matching is provided by the resistor which is connected from the clock input pin to the ground.

The output of the divider was expected to be within a range of 20 MHz to 50 MHz and its matching although important, was not critical. A 200Ω resistor is connected from the output pin to ground and is ac coupled to a SMA connector on the board to take the signal out for observation. The two 50Ω SMA connectors for the clock input and the output signal were soldered close to the chip to reduce signal losses. The output was then taken through a 50Ω coaxial cable either to the spectrum analyzer or to the high frequency oscilloscope for observation.

### 5.2.3 Operating Frequency Range

The operating frequency range was measured using the test setup described in the previous section. Since the output of the divider is a square wave, a spectrum analyzer was used to observe the fundamental component of the output signal. For proper functioning, the fundamental frequency component at the output and the input clock signal must be related by the divider ratio i.e.,

$$f_{clk} = \text{ratio} \cdot f_{out}$$

in which the ratio is either 32 ($mc\_div2='1'$ or 5V) or 31 ($mc\_div2='0'$ or 0V). To find the maximum operating frequency of the circuit at a certain divider supply voltage $V_{dd}$, the bias $V_b$ is set to $V_{dd}$ and the signal generator is set to provide a peak-to-peak signal ampli-
tude of $V_{dd}/2$. The frequency is then increased until the input-output relation in Equation 5.1 is no longer held. Similarly, minimum operating frequency is found by following the same procedure but by decreasing the frequency until the circuit fails to provide correct ratios.

### 5.2.4 Power Characteristics

This section illustrates how the frequency divider consumes power as the frequency is varied over the operating range with the clock signal kept at the maximum amplitude. Figure 5.3 shows the curves obtained at 5V supply, $V_{dd}$ for the two divider ratios. The current taken by the divider was measured by inserting a current meter in the

![Power Consumption at 5V Supply](image)
supply path of the divider. As typical in CMOS circuits, the power consumption varies almost linearly with the frequency. As can be seen in Figure 5.3 that the division by 31 determines the operating frequency range which is 960 MHz to 1.9 GHz. The operating range for divide by 32 operation is wider and goes down to 800 MHz from 1.9 GHz.

Figure 5.4: Input Signal Sensitivity as a Function of Input Frequency

5.2.5 Sensitivity to the Input Signal

Looking at the divider architecture, it can be seen that the first stage includes a feedback loop. The transistors in the circuit switch on and off when the clock signal goes high and low. If the clock signal is kept at a certain dc level, the clocked transistors in the two first stage flip-flops will remain partially on and would provide paths to circuit ground from different nodes of the circuit. The presence of feedback will therefore cause the first
stage to oscillate. The circuit can thus be seen as an injection locked oscillator due to the injected clock signal as described in section 3.2.2. A typical characteristic of such frequency dividers is that at a certain frequency, which is a subharmonic component of the clock signal, resonance will occur and the divider will operate with minimum input signal amplitude. The divider input sensitivity is an important parameter characterizing RF frequency range of prescalers. A set of curves depicting the input sensitivity of the divider circuit obtained for the two ratios 31 and 32 is shown in Figure 5.4. Again, divide by 31 operation determines the operating frequency range. For this test, the peak-to-peak input clock signal was kept to $V_{dd}$ Volts, $V_{dd}$ being the varied supply voltage.

### 5.2.6 Maximum Operating Frequency with Supply Voltage Variations.

The variation of the maximum operating frequency as a function of supply voltage is shown graphically in Figure 5.5. It shows that the circuit slows down as the supply voltage is decreased. Also, as shown in Figure 5.6, the current taken by the divider is shown as a function of supply voltage with the divider operating at maximum frequency for that supply voltage. The graphs in Figure 5.6 correspond to those in Figure 5.5. The vertical lines on the curves show the operating range at different supply voltages.
Figure 5.5: Maximum and Minimum Operating Frequency vs Supply Voltage
Performance Evaluation

Supply Voltage. Volts

Current

at

Maximum
operating
frequency

Current

at

Minimum
operating
frequency

Figure 5.6: Maximum and Minimum Current Consumption vs Supply Voltage
5.2.7 Self Oscillation Characteristics

The divider circuit oscillates without a clock signal when a certain dc voltage $V_b$ is applied to the clock input. This behavior provides useful information when the circuit is incorporated in a system such as a PLL so that the circuit response may be predicted at start-up. Figure 5.7 shows how the divider self oscillation frequency varies as different supply voltages with $V_b$ set at $V_{dd}/2$ for different supply voltages.

Figure 5.7: Self Oscillation Characteristics as a Function of Supply Voltage
5.2.8 Demonstration of Divider Operation

Oscilloscope traces in Figure 5.8(a) demonstrates the prescaler operation at 1486 MHz and Figure 5.8(b) shows its operation at a frequency of 960 MHz while dividing by 31.

Figure 5.8: Oscilloscope Traces Illustrating Division by 31
5.3 Divide-by-3/4 GCMOS Dual-Modulus Frequency Divider

The first stage of the divider circuit, Figure 3.6, was fabricated in Motorola's GCMOS technology. This design was submitted for fabrication as part of a joint research project between Carleton University and Motorola. The design was laid out with the same device sizes as the ones used in 0.8μm BiCMOS process. The circuit was tested and measurements were obtained to record its speed and power characteristics as well as the sensitivity to the input signal.

5.3.1 Floor Plan

Figure 5.9 shows the layout floor plan for the divide-by-3/4 frequency prescaler. On chip decoupling capacitors were used at the dc supply lines close to the circuit and the buffer. Two buffers were provided in order to drive the external 50Ω RF probes. The first one is the Pre-Buffer which is an NMOS inverter with an adjustable bias. The second one is the main RF buffer consisting of multiple inverter stages. During the testing it was found that the main RF buffer did not function properly and the output gets stuck at either of the supply voltages at different frequencies. The cause of this was investigated and it was found that the dc level at different internal nodes of the multistage buffer is different at different frequencies and high dc gain of the buffer makes it unstable in the absence of negative feedback.

5.3.2 Test Bed

The test bed used to measure different characteristics of this implementation of the circuit is shown in Figure 5.10. The dies were fixed on printed circuit board specially
designed for testing at high frequencies. Decoupling was provided both on chip as well as off the chip on the PCB.

As explained in the previous section, there were problems with the RF buffer and the output signal could not be taken out from the designated output pad. An alternate method was provided to take the signal out of the chip. As shown in Figure 5.9, the source of the NMOS transistor in the Pre-Buffer is open. By connecting the circuit as a source follower and providing an external RF amplifier the output of the prescaler was success-

![Diagram of Prescaler Circuit](image)

**Figure 5.9: Layout Floor Plan of the Divide-by-3/4 GCMOS Frequency Prescaler**

fully brought out. The set-up used for this purpose is shown in Figure 5.11. The two variable resistors provide dc biases for the Pre-Buffer while a switch is connected through a resistor to provide the modulus control signal. SMA connectors were fixed on the RF
board for the input and output signal. Since the output signal was taken from the Pre-Buffer, an external LNA was used to further strengthen the signal in order to observe it on the spectrum analyzer or high-frequency oscilloscope. The method used for this purpose is shown in Figure 5.11 where a 200Ω resistor combined with the NMOS transistor of the Pre-Buffer forms the source follower circuit. An external variable resistor was used to adjust the dc level at the drains of the two MOSFETs in the prebuffer. The output signal is then capacitively coupled to the LNA MRF1C1501. The LNA is matched to 50Ω and can

Figure 5.10: Test Set-up for the Divide-by-3/4 GCMOS Frequency Prescaler

Design and Design Methodology of CMOS Gigahertz Frequency Range Prescalers
Performance Evaluation

5.3.3 Operating Frequency Range and Input Signal Sensitivity

Figure 5.11: Method to Take Out the Signal using an external LNA

Figure 5.12 shows the sensitivity of the divide-by-3/4 prescaler to the input signal. From the characteristics the circuit can be seen to have a wide operating range \textit{i.e.} from 220 MHz to 1700 MHz. The range is reduced with decreasing input signal amplitude and for a peak-to-peak signal of 1 Volt, is only about 500 MHz, from 600 MHz to 1110 MHz. The minimum amplitude required for the two ratios is different for each frequency and the notch for each occurs at different frequency as well.
Figure 5.12: Input Sensitivity and Operating Frequency Range for the GCMOS Prescaler

5.3.4 Power Characteristics

The measured power characteristics for the GCMOS prescaler is shown in Figure 5.13. At the maximum frequency the power consumed is seen to be only 6.7 mW at 3 Volts supply voltage. For the entire range of operation the power per MHz is 7.7 \( \mu \text{W/MHz} \).

5.3.5 Demonstration of Prescaler Operation.

Figure 5.14 shows the oscilloscope images of the GCMOS prescaler operating at two different frequencies for the two division ratios.
Performance Evaluation

![Power Consumption vs Frequency Graph]

Figure 5.13: Power Characteristics of the Divide-by-3/4 GCMOS Prescaler

5.4 Summary

This chapter presented the measurement results for the two dual-modulus prescaler circuits. Both circuits were tested to find different characteristics. Important ones include the highest operating frequency, operating frequency range, input sensitivity and power dissipation. All the devices were found to be functional. The results show the successful application of the design and optimization methodology and also illustrate that the CMOS technology is suitable for communications systems operating in the range of 1-2 GHz.
Figure 5.14: Illustration of Divider Operation
6.1 Conclusions

In this thesis, a design methodology for designing high speed dual-modulus prescalers has been approached by an extensive research from the existing literature, followed by simulation and comparison of different structures and circuits. The design methodology allows to optimize the circuit independent of the technology. This is verified by experimental device evaluation by fabricating the design in two CMOS technologies.

The criteria chosen for the dual-modulus prescaler circuit asked for simple architecture as well as simple circuits for implementation of the selected architecture. For this purpose, a two stage architecture was selected. The first stage is composed of two flip-flops to scale down the input clock signal by a factor of 3 or 4 depending on the single bit control signal. Doing so allows a slower second stage with a fixed division ratio to further scale down the frequencies. Although any division ratio can be obtained, a division ratio of 31/32 was chosen to keep the circuit small and simple for testability. The CMOS dynamic logic circuits operating on a single clock (TSPC technique) were used for all the flip-flops of the prescaler to reduce clock loading as well as eliminating clock skew problems. These
decisions resulted in a circuit capable of working at 1.9 GHz with a 5V power supply while consuming only 17.5 mW at that frequency. The circuit was implemented in NT 0.8μm BiCMOS technology. The same circuit at 3V operates at 1200 MHz (maximum operating frequency) while taking only 3.5 mW. The other circuit, a divide-by-3/4 prescaler, fabricated in Motorola’s GCMOS technology uses a 3V supply and operates up to 1.7 GHz while consuming 6.5 mW.

Several monolithic dual-modulus prescalers have been reported in the literature, many of which are implemented in high-performance technologies. Table 6.1 summarizes selected work reported in the past few years. Only CMOS prescalers are listed in the Table. The authors generally report achievements regarding high speed operation.

As can be seen in Table 6.1, in [26] a divide-by-8/9 prescaler was reported. The circuit used dynamic flip-flops and the transistor sizes were optimized to achieve an operating frequency of 1.16 GHz. The same author reports another design in [22] of a 128/129 prescaler with logic functions embedded into the dynamic flip-flops to reduce delays. Speed improvements were also gained by optimizing the transistor sizes. However, the power dissipation is high. A low power divide-by-15/16 prescaler was reported in [24] which uses self-oscillating latches instead of flip-flops to achieve a significant improvement in operating frequency. The drawback of this circuit is its narrow operating frequency range. Another circuit, which uses a novel prescaler architecture was reported in [27]. This circuit uses a phase-select block to switch the modulus. At 3 Volts, it achieves an operating frequency of 1.75 GHz but the circuit needs very careful design approach. In [46] the dual-modulus prescaler circuit was reported which uses a shift-register ring how-
Conclusions

ever, it does not show significant performance improvement. [37] reports a circuit with an even smaller division ratio of 7/8 and consumes a fair amount of power, 31 mW at 5 V. In contrast, in this work a more conventional architecture was implemented by using dynamic CMOS flip-flops. The circuit performance as mentioned earlier, shows significant improvement in comparison to the reported prescaler circuits.

<table>
<thead>
<tr>
<th>Reported by</th>
<th>Year</th>
<th>Ratio</th>
<th>Gate-Length $\mu$m</th>
<th>$f_{\text{max}}$ GHz</th>
<th>Power$^1$, Supply</th>
</tr>
</thead>
<tbody>
<tr>
<td>N. Foroudi, Kwasniewski [24]</td>
<td>1992</td>
<td>15/16</td>
<td>1.2</td>
<td>1.5</td>
<td>13 mW @5V</td>
</tr>
<tr>
<td>R. Rogenmoser [26]</td>
<td>1993</td>
<td>8/9</td>
<td>1.2</td>
<td>1.16</td>
<td>45 mW @5V</td>
</tr>
<tr>
<td>Crainickx, Steyaert [27]</td>
<td>1996</td>
<td>128/129</td>
<td>0.7</td>
<td>1.75</td>
<td>24 mW @3V</td>
</tr>
<tr>
<td>R. Rogenmoser [22]</td>
<td>1996</td>
<td>128/129</td>
<td>1.2</td>
<td>1.61</td>
<td>52.5 mW @5V</td>
</tr>
<tr>
<td>P. Larsson [46]</td>
<td>1996</td>
<td>8/9</td>
<td>0.8</td>
<td>1.75</td>
<td>50 mW @5V</td>
</tr>
<tr>
<td>Chang [45]</td>
<td>1996</td>
<td>128/129</td>
<td>0.8</td>
<td>1.22</td>
<td>25.5 mW @5V</td>
</tr>
<tr>
<td>Seog-Jun [37]</td>
<td>1997</td>
<td>7/8</td>
<td>0.8</td>
<td>1.45</td>
<td>31 mW @5V</td>
</tr>
<tr>
<td>K. Sheikh, T. A. Kwasniewski$^2$</td>
<td>1998</td>
<td>31/32</td>
<td>0.8</td>
<td>1.9</td>
<td>17.5 mW @5V</td>
</tr>
<tr>
<td>K. Sheikh, T. A. Kwasniewski$^2$</td>
<td>1998</td>
<td>31/32</td>
<td>0.8</td>
<td>1.2</td>
<td>3.5 mW @3V</td>
</tr>
</tbody>
</table>

$^1$Power dissipation at $f_{\text{max}}$

$^2$This work.

The results described above show that although it is difficult to optimize a circuit both for power and speed at the same time, power taken by the prescaler can be reduced by clever selection of the flip-flop circuits and clocking technique. Speed improvements can be achieved by systematic approach for optimization and by giving careful attention to reduce the time delays in the control logic. The control-logic block controls the division ratio of the prescaler and reduction of delays in this block is an important factor. For this work, use of conventional logic was avoided for the first stage, which operates at the highest frequencies, and a faster approach was used. A simple NAND gate from the later, slower flip-flop stages then easily served the purpose of controlling the division ratio.
Conclusions

Thus in conclusion, the thesis contributes in outlining design guidelines for dual-modulus CMOS prescaler design. Generally, the current literature does not provide such guidelines in one place. In view of the RF circuit design trends in CMOS technology, this thesis can be seen as one step forward in establishing design practices in this regard. The design and optimization methodologies described in this thesis have been successful in satisfying the performance criteria for the design of dual-modulus prescaler circuits, i.e. dual-modulus operation, a high operating frequency and a wide operating frequency range, low power dissipation and small silicon area. Such a circuit can easily be incorporated into many applications for modern communication systems operating the range of 1-2 GHz.

6.2 Issues

As has been mention earlier, CMOS technology has only started to make its way into circuits for RF applications. But there are some bottlenecks for the designer, the most important one being faced is related to device modeling. As is evident from the text, the HSPICE simulation showed a maximum operating frequency of 1060 MHz whereas the practically achieved maximum frequency was 1900 MHz. Such problems have come into the picture because of the rapid advancements in the microelectronic technologies. There is a lack of understanding of many circuits in modern complex VLSI designs and this can be observed by noting that many of the circuits fail to work in their first runs [44]. Perhaps two of the reasons which can be attributed to this lack of understanding are that: one, almost all of the circuit design is now carried out using computer simulation. Sometimes it is hard to interpret the simulation results and the theory behind it even though the overall
Conclusions

functionality is successfully being achieved. The second factor is that the time constraints on the circuit designers are two fold, first is the tape-out time while the second is the time-to-market for the product. This situation seems to increasingly aggravate the problem as the communication consumer market expands with time.

6.3 Future Research

The prescaler circuit presented in this work has been implemented and evaluated in isolation. In the testing however, phase noise of the prescaler was not measured. Already at Department of Electronics, Carleton University new circuits have been designed for Modulus Controllers [17]. One proposal is to integrate both the prescaler circuit and the modulus control circuit together and evaluate the phase noise and switching characteristics. The second proposal is to explore more technologies which are available now. 0.35μm and 0.25μm gate-length CMOS technologies for commercial purposes are already in the market and these should be explored for RF applications. Such deep sub-micron devices could give unprecedented operating speeds for CMOS circuits which can easily compete the other high performance technologies in price and performance.
Appendix A

BiCMOS Process Parameters

A.1 HSPICE Level 3 Device Parameters

<table>
<thead>
<tr>
<th>Parameter Description</th>
<th>NMOS</th>
<th>PMOS</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>UO (Low-field bulk mobility)</td>
<td>475</td>
<td>154</td>
<td>cm²/Vs</td>
</tr>
<tr>
<td>VTO (Zero-bias threshold voltage)</td>
<td>0.8115</td>
<td>-0.902</td>
<td>V</td>
</tr>
<tr>
<td>TOX (Oxide thickness)</td>
<td>17.52E-9</td>
<td>17.52E-9</td>
<td>m</td>
</tr>
<tr>
<td>DELTA (Narrow width factor for adjusting threshold)</td>
<td>1.0529</td>
<td>0.295</td>
<td>N.A.</td>
</tr>
<tr>
<td>THETA (Mobility degradation factor)</td>
<td>52.45E-3</td>
<td>128.0E-3</td>
<td>I/V</td>
</tr>
<tr>
<td>RS (Source ohmic resistance)</td>
<td>1.076E+3</td>
<td>1.2E+3</td>
<td>Ohms</td>
</tr>
<tr>
<td>RD (Drain ohmic resistance)</td>
<td>1.076E+3</td>
<td>1.2E+3</td>
<td>Ohms</td>
</tr>
<tr>
<td>VMAX (Maximum carrier drift velocity)</td>
<td>146.5E+3</td>
<td>277.3E+3</td>
<td>m/s</td>
</tr>
<tr>
<td>ETA</td>
<td>36.06E-3</td>
<td>79.53E-3</td>
<td></td>
</tr>
<tr>
<td>KAPPA (Saturation field factor)</td>
<td>1E-12</td>
<td>9.56</td>
<td>N.A.</td>
</tr>
<tr>
<td>CJ (Zero-bias bulk junction capacitance)</td>
<td>260.0E-6</td>
<td>450.0E-6</td>
<td>F/m²</td>
</tr>
<tr>
<td>CGBO (Gate-Bulk overlap capacitance)</td>
<td>568.3E-12</td>
<td>568.3E-12</td>
<td>F/m</td>
</tr>
<tr>
<td>CGSO (Gate-source overlap capacitance)</td>
<td>288.4E-12</td>
<td>214.8E-12</td>
<td>F/m</td>
</tr>
<tr>
<td>CGDO (Gate-drain overlap capacitance)</td>
<td>288.4E-12</td>
<td>214.8E-12</td>
<td>F/m</td>
</tr>
<tr>
<td>KF (Flicker noise coefficient)</td>
<td>1.5E-24</td>
<td>250.0E-27</td>
<td>N.A.</td>
</tr>
<tr>
<td>AF (Flicker noise exponent)</td>
<td>0.85</td>
<td>0.95</td>
<td>N.A.</td>
</tr>
</tbody>
</table>
Appendix B

**Physical Design, Circuits, Chip Configuration and Layout Diagrams.**

The following sections illustrate the frequency divider circuits, layout diagrams and chip configurations. The circuits are shown first and are followed by the corresponding layout diagrams. The section B.1 consists of the IBACUKS1 design while the section B.2 describes the design of the GCMOS prescaler. Tables B.1 and B.2 give the signal names and their respective description.

**B.1 Physical Design of IBACUKS1**

This section illustrates the physical design of the divide-by-31/32 prescaler circuit implemented in NT 0.8μm BiCMOS process. Table B.1 gives the signal names and their respective description. Then the circuits or the configurations are given followed by the related layout diagrams.
### TABLE B.1: IBACUKS1 Signal Names and Description

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Description</th>
<th>Signal Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vdd_div1</td>
<td>Power supply input for 31/32 divider no. 1.</td>
<td>Vdd_div1_34</td>
<td>Power supply input for 3/4 divider no. 1.</td>
</tr>
<tr>
<td>mc_div1</td>
<td>Modulus control input for divider 1.</td>
<td>mc_div1_34</td>
<td>Modulus control input for 3/4 divider 1.</td>
</tr>
<tr>
<td>clk_div1</td>
<td>Clock input for divider 1.</td>
<td>clk_div1_34</td>
<td>Clock input for 3/4 divider 1.</td>
</tr>
<tr>
<td>Vdd_buf_div1</td>
<td>Power for buffer.</td>
<td>Vdd_buf_div1_34</td>
<td>Power for buffer.</td>
</tr>
<tr>
<td>op_div1</td>
<td>Output signal from divider 1.</td>
<td>op_div1_3/4</td>
<td>Output signal from 3/4 divider 1.</td>
</tr>
<tr>
<td>Vdd_div2</td>
<td>Power supply input for 31/32 divider no. 2.</td>
<td>Vdd_div2_34</td>
<td>Power supply input for 3/4 divider no. 2.</td>
</tr>
<tr>
<td>mc_div2</td>
<td>Modulus control input for divider 2.</td>
<td>mc_div2_34</td>
<td>Modulus control input for 3/4 divider 2.</td>
</tr>
<tr>
<td>clk_div2</td>
<td>Clock input for divider 2.</td>
<td>clk_div2_34</td>
<td>Clock input for 3/4 divider 2.</td>
</tr>
<tr>
<td>Vdd_buf_div2</td>
<td>Power for buffer.</td>
<td>Vdd_buf_div2_34</td>
<td>Power for buffer.</td>
</tr>
<tr>
<td>op_div2</td>
<td>Output signal from divider 2.</td>
<td>op_div2_3/4</td>
<td>Output signal from 3/4 divider 2.</td>
</tr>
<tr>
<td>VSS1</td>
<td>Substrate ground no. 1.</td>
<td>VSS2</td>
<td>Substrate ground no. 2.</td>
</tr>
</tbody>
</table>
Physicat Design, Circuits, Chip Configuration and Layout Diagrams.

Figure B.1: IBACUKS1 Chip Floor plan
Figure B.2: IBACUKS1 Layout Diagram

Design and Design Methodology of CMOS Gigahertz Frequency Range Prescalers
Figure B.3: Divide-by-31/32 Prescaler Schematic Diagram

- All transistor sizes in μm
- All Gate-Lengths = 0.8μm
Figure B.4: Divide-by-31/32 Prescaler Layout Diagram
Figure B.5: First Stage Circuit, Divide-by-3/4 Prescaler
Figure B.6: First Stage Layout
Figure B.7: First Stage Flip-Flop, FF1 Schematic Diagram
Figure B.8: First Stage Flip-Flop, FF1 Layout Diagram
Figure B.9: First Stage Flip-Flop, FF2 Schematic Diagram
Figure B.10: First Stage Flip-Flop, FF2 Layout Diagram
Figure B.11: Second Stage Flip-Flop, TFF Schematic Diagram
Figure B.12: Second Stage Flip-Flop, TFF Layout Diagram
Figure B.13: Divide-by-31/32 Prescaler Layout Showing Second Stage in the Upper Half of the Layout
Figure B.14: Layout Layers for BiCMOS Process
Physical Design, Circuits, Chip Configuration and Layout Diagrams.

B.2 Physical Design of the Divide-by-3/4 GCMOS Prescaler

This section presents the chip configuration, circuit schematics and the related layout diagrams for the frequency prescaler design implemented in Motorola’s GCMOS process.

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Modulus Control</td>
<td>Modulus control input.</td>
</tr>
<tr>
<td>V_{dd} Prescaler</td>
<td>Power input for prescaler.</td>
</tr>
<tr>
<td>Clock Input</td>
<td>Input for clock signal.</td>
</tr>
<tr>
<td>V_{ss} Prescaler</td>
<td>Ground for prescaler.</td>
</tr>
<tr>
<td>SubGnd1</td>
<td>Substrate ground no. 1.</td>
</tr>
<tr>
<td>V_{ss} Prebuf</td>
<td>Ground for prebuffer.</td>
</tr>
<tr>
<td>SubGnd2</td>
<td>Substrate ground no. 2.</td>
</tr>
<tr>
<td>V_{ss} RFbuf</td>
<td>Ground for RF buffer.</td>
</tr>
<tr>
<td>Output</td>
<td>Output of the prescaler.</td>
</tr>
<tr>
<td>Gnd</td>
<td>Circuit ground.</td>
</tr>
<tr>
<td>V_{dd} RFbuf1</td>
<td>Power input for RF buffer no. 1.</td>
</tr>
<tr>
<td>V_{dd} RFbuf2</td>
<td>Power input for RF buffer no. 2.</td>
</tr>
<tr>
<td>V_{dd} RFbuf3</td>
<td>Power input for RF buffer no. 3.</td>
</tr>
<tr>
<td>Sub. V_{dd}</td>
<td>Substrate tie up to supply.</td>
</tr>
<tr>
<td>V_{dd} Prebuf</td>
<td>Power input for prebuffer.</td>
</tr>
<tr>
<td>Prebuf bias</td>
<td>DC bias input for prebuffer.</td>
</tr>
<tr>
<td>NC</td>
<td>No Connection.</td>
</tr>
</tbody>
</table>
Figure B.15: Floor Plan of Divide-by-3/4 GCMOS Prescaler Chip
Figure B.16: Divide-by-3/4 GCMOS Prescaler Chip Layout Diagram
Figure B.17: Divide-by-34/32 CMOS Prescaler Schematic Diagram

* Transistor sizes in UDR
* All gate lengths L = 4

Design and Design Methodology of CMOS Gigahertz Frequency Range Prescalers
Figure B.18: Divide-by-3/4 GCMOS Prescaler Layout Diagram
References


3. Carleton University VLSI in Communications group research reports, unpublished.


17. Thierry Lepley, "Modulus Controllers for Fractional-N Frequency Synthesizers", Department of Electronics, Carleton University, Ottawa, ON, Canada, 1996.


